Renesas Electronics America Inc - UPD78F1188AGJ-GAE-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	30K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1188agj-gae-ax

3.4.8 Based indexed addressing

[Function]

Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register)

Figure 3-38. Example of [HL+B], [HL+C]

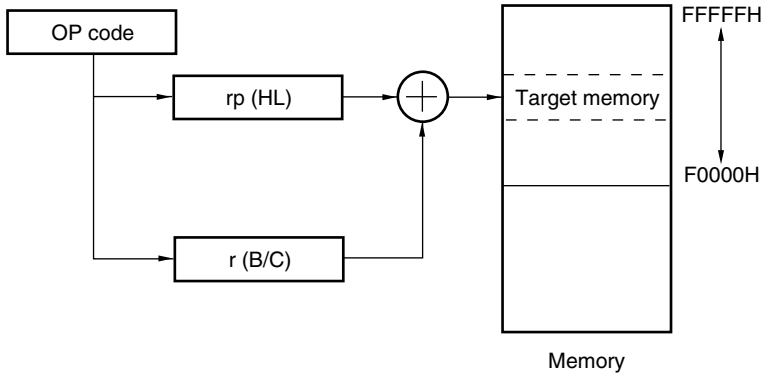
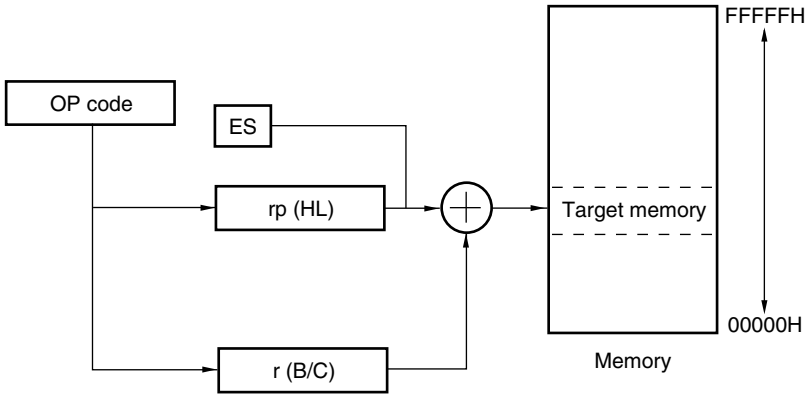


Figure 3-39. Example of ES:[HL+B], ES:[HL+C]



(2) Port registers (P0 to P16)

These registers write the data that is output from the chip when data is output from a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read[Note].

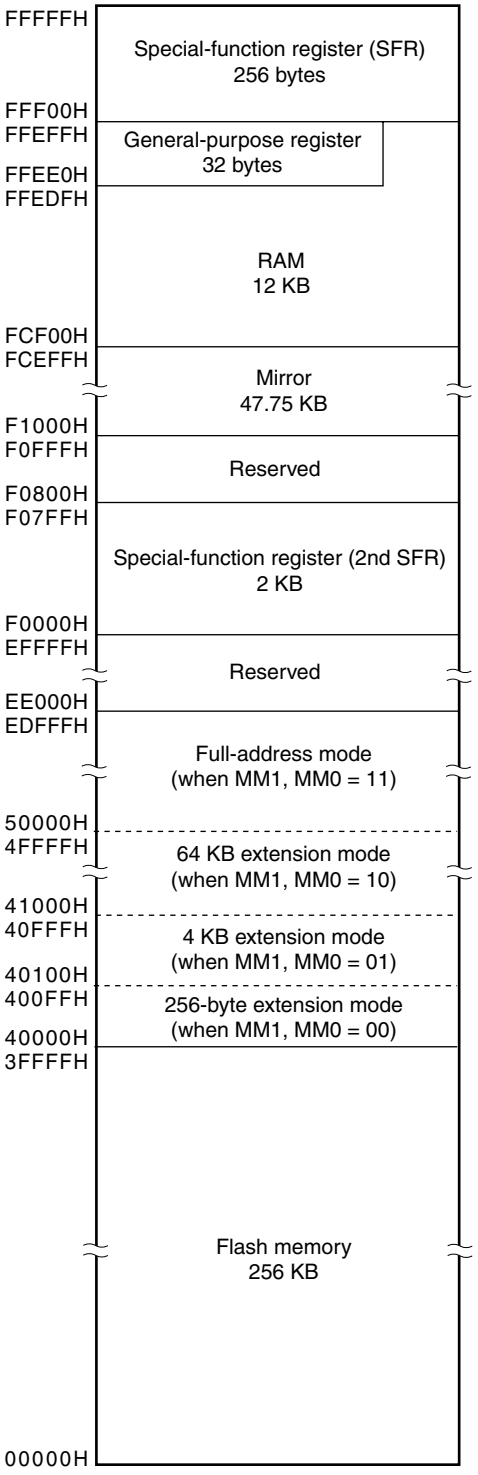
These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

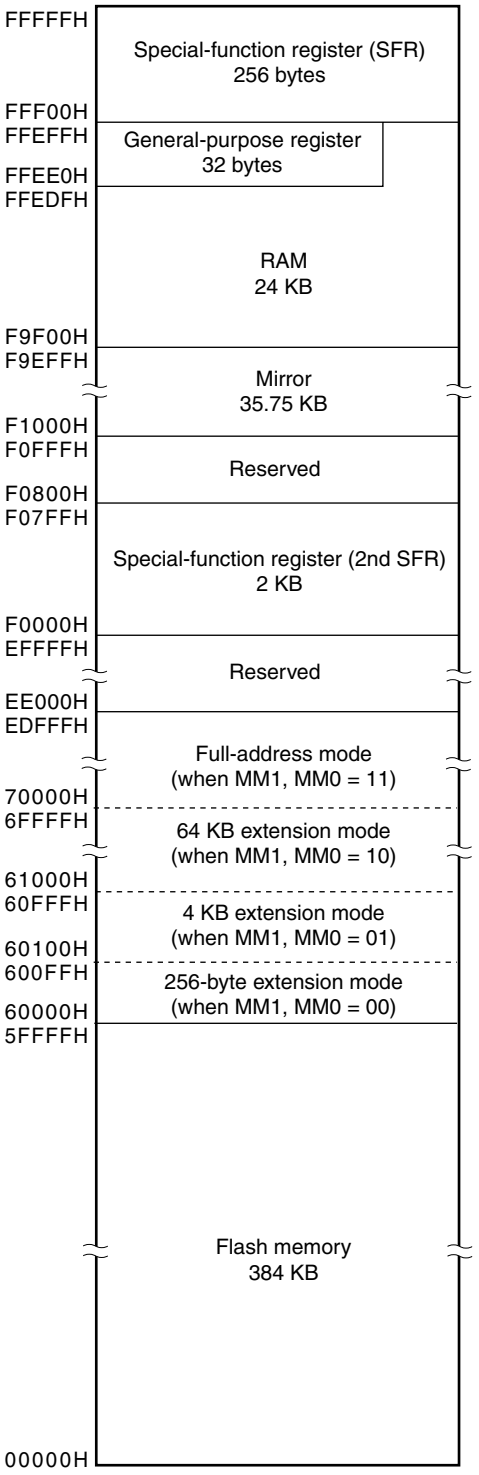
Note It is always 0 and never a pin level that is read out if a port is read during the input mode when P2 and P15 are set to function as an analog input for a A/D converter or P11 is set to function as an analog output for a D/A converter.

Figure 5-1. Memory Map When Using External Bus Interface Function (2/3)

(c) Memory map of μPD78F1186A



(d) Memory map of μPD78F1187A



(7) Operation speed mode control register (OSMC)

This register is used to control the step-up circuit of the flash memory for high-speed operation.

If the microcontroller operates at a low speed with a system clock of 10 MHz or less, the power consumption can be lowered by setting this register to the default value, 00H.

OSMC can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6-8. Format of Operation Speed Mode Control Register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	0	0	0	0	0	0	0	FSEL

FSEL	f_{CLK} frequency selection
0	Operates at a frequency of 10 MHz or less (default).
1	Operates at a frequency higher than 10 MHz.

Cautions 1. OSMC can be written only once after reset release, by an 8-bit memory manipulation instruction.

2. Write "1" to FSEL before the following two operations.

- **Changing the clock prior to dividing f_{CLK} to a clock other than f_{IH}.**
- **Operating the DMA controller.**

3. The CPU waits when "1" is written to the FSEL flag.
Interrupt requests issued during a wait will be suspended.
The wait time is 16.6 μs to 18.5 μs when $f_{CLK} = f_{IH}$, and 33.3 μs to 36.9 μs when $f_{CLK} = f_{IH}/2$.
However, counting the oscillation stabilization time of f_X can continue even while the CPU is waiting.

<R> **4. To increase f_{CLK} to 10 MHz or higher, set FSEL to "1", then change f_{CLK} after two or more clocks have elapsed. Use the external bus interface two clock cycles after setting FSEL to 1.**

<R> **5. Flash memory can be used at a frequency of 10 MHz or lower if FSEL is 1.**

Figure 7-40. Operation Procedure of Interval Timer/Square Wave Output Function (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit, TAU1EN bit of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSm register. Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the TMRmn register (determines operation mode of channel). Sets the TISmn bit to 1 (f_{SUB}/4) when f_{SUB}/4 is selected as the count clock. Sets interval (period) value to the TDRmn register.	Channel stops operating. (Clock is supplied and some power is consumed.)
	To use the TOmn output Clears the TOMmn bit of the TOMm register to 0 (toggle mode). Clears the TOLmn bit to 0. Sets the TOmn bit and determines default level of the TOmn output. →	The TOmn pin goes into Hi-Z output state. The TOmn default setting level is output when the port mode register is in the output mode and the port register is 0.
	Sets TOEmn to 1 and enables operation of TOmn. →	TOmn does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmn pin outputs the TOmn set level.
Operation start	Sets TOEmn to 1 (only when operation is resumed). Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Value of TDRmn is loaded to TCRmn at the count clock input. INTTMmn is generated and TOmn performs toggle operation if the MDmn0 bit of the TMRmn register is 1.
During operation	Set values of TMRmn register, TOMmn, and TOLmn bits cannot be changed. Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TOm and TOEm registers can be changed.	Counter (TCRmn) counts down. When count value reaches 0000H, the value of TDRmn is loaded to TCRmn again and the count operation is continued. By detecting TCRmn = 0000H, INTTMmn is generated and TOmn performs toggle operation. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. TCRmn holds count value and stops. The TOmn output is not initialized but holds current status.
	TOEmn is cleared to 0 and value is set to TOmn bit. →	The TOmn pin outputs the TOmn set level.

Operation is resumed.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

Figure 7-43. Example of Set Contents of Registers in External Event Counter Mode

(a) Timer mode register mn (TMRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKSmn			CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0			MDmn3	MDmn2	MDmn1	MDmn0
	1/0	0	0	1	0	0	0	0	1/0	1/0	0	0	0	1	1	0

Operation mode of channel n
011B: Event count mode

Setting of operation when counting is started
0: Neither generates INTTMmn nor inverts timer output when counting is started.

Selection of TImn pin input edge
00B: Detects falling edge.
01B: Detects rising edge.
10B: Detects both edges.
11B: Setting prohibited

Start trigger selection
000B: Selects only software start.

Slave/master selection
0: Cleared to 0 when single-operation function is selected.

Count clock selection
1: Selects the TImn pin input valid edge.

Operation clock selection
0: Selects CKm0 as operation clock of channel n.
1: Selects CKm1 as operation clock of channel n.

(b) Timer output register m (TOm)

	Bit n
TOm	TOmn
	0

0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n
TOEm	TOEmn
	0

0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n
TOLm	TOLmn
	0

0: Cleared to 0 when TOMmn = 0 (toggle mode).

(e) Timer output mode register m (TOMm)

	Bit n
TOMm	TOMmn
	0

0: Sets toggle mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

Figure 8-4. Format of Real-Time Counter Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RWST	Wait status flag of real-time counter
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of RWAIT is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

RWAIT	Wait control of real-time counter
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. Because RSUBC continues operation, complete reading or writing of it in 1 second, and clear this bit back to 0. When RWAIT = 1, it takes up to 1 clock (32.768 kHz) until the counter value can be read or written. If RSUBC overflows when RWAIT = 1, it counts up after RWAIT = 0. If the second count register is written, however, it does not count up because RSUBC is cleared.	

Caution The RIFG and WAFG flags may be cleared when the RTCC1 register is written by using a 1-bit manipulation instruction. Use, therefore, an 8-bit manipulation instruction in order to write to the RTCC1 register. To prevent the RIFG and WAFG flags from being cleared during writing, disable writing by setting “1” to the corresponding bit. When the value may be rewritten because the RIFG and WAFG flags are not being used, the RTCC1 register may be written by using a 1-bit manipulation instruction.

Remark Fixed-cycle interrupts and alarm match interrupts use the same interrupt source (INTRTC). When using these two types of interrupts at the same time, which interrupt occurred can be judged by checking the fixed-cycle interrupt status flag (RIFG) and the alarm detection status flag (WAFG) upon INTRTC occurrence.

11.4.3 A/D converter operation mode

The operation mode of the A/D converter is the select mode. One channel of analog input is selected from ANI0 to ANI15 by the analog input channel specification register (ADS) and A/D conversion is executed.

(1) A/D conversion operation

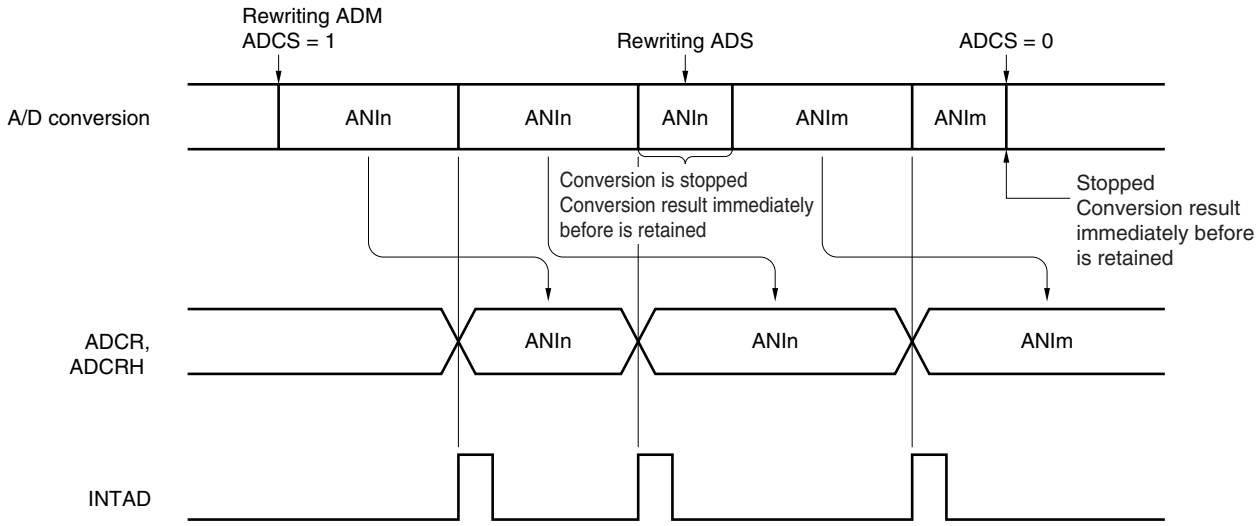
By setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 1, the A/D conversion operation of the voltage, which is applied to the analog input pin specified by the analog input channel specification register (ADS), is started.

When A/D conversion has been completed, the result of the A/D conversion is stored in the A/D conversion result register (ADCR), and an interrupt request signal (INTAD) is generated. When one A/D conversion has been completed, the next A/D conversion operation is immediately started.

If ADS is rewritten during A/D conversion, the A/D conversion operation under execution is stopped and restarted from the beginning.

If 0 is written to ADCS during A/D conversion, A/D conversion is immediately stopped. At this time, the conversion result immediately before is retained.

Figure 11-14. A/D Conversion Operation

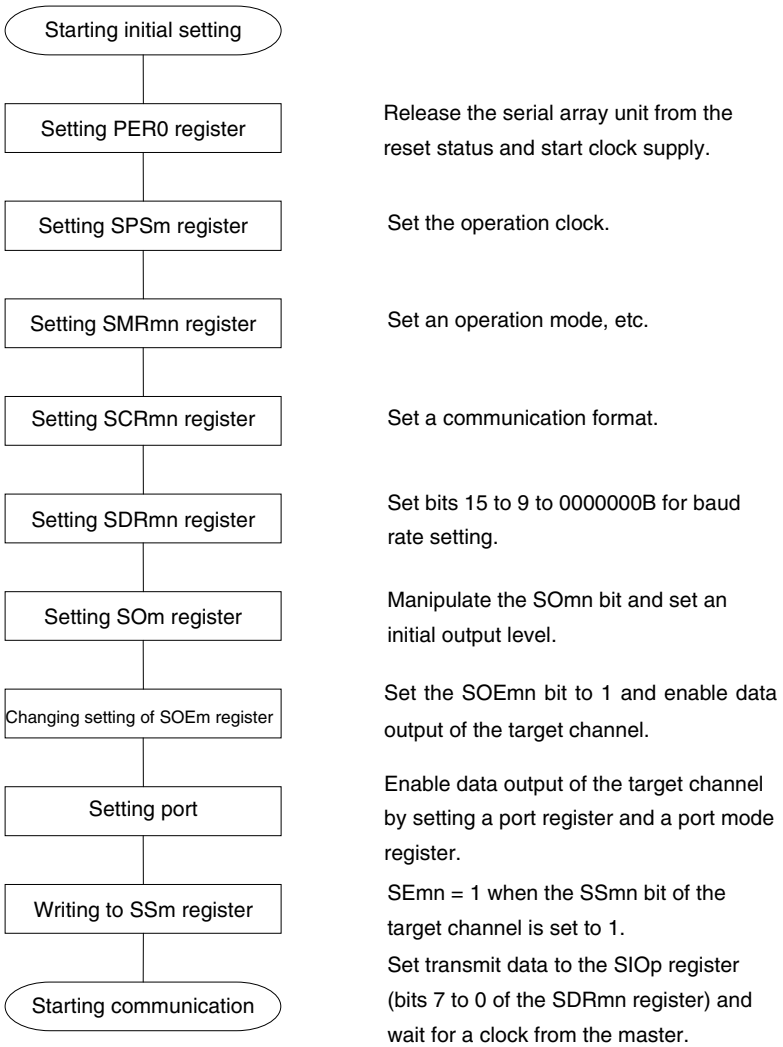


Remarks 1. n = 0 to 15

2. m = 0 to 15

(2) Operation procedure

Figure 13-49. Initial Setting Procedure for Slave Transmission



Caution After setting the PER0 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Notes 1. The SE1 register is a read-only status register which is set using the SS1 and ST1 registers.

2. When channel 1 of unit 1 is set to UART2 reception, this pin becomes an RxD2 function pin. In this case, set channel 0 of unit 1 to operation stop mode or UART2 transmission (refer to **Table 13-9**).
When channel 0 of unit 1 is set to CSI20 or IIC20, this pin cannot be used as an RxD2 function pin. In this case, set channel 2 of unit 1 to operation stop mode or CSI21 or IIC21.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **13.3 (12) Serial output register m (SOm)**.

5. When using UART2 transmission and reception in a pair, set channel 1 of unit 0 to UART2 transmission (refer to **Table 13-9**).

6. The SMR10 register of channel 1 of unit 0 must also be set during UART2 reception. For details, refer to **13.6.2 (1) Register setting**.

7. Set the CKO11 bit to 1 before a start condition is generated. Clear the SO11 bit from 1 to 0 when the start condition is generated.

8. Set the CKO11 bit to 1 before a stop condition is generated. Clear the SO11 bit from 0 to 1 when the stop condition is generated.

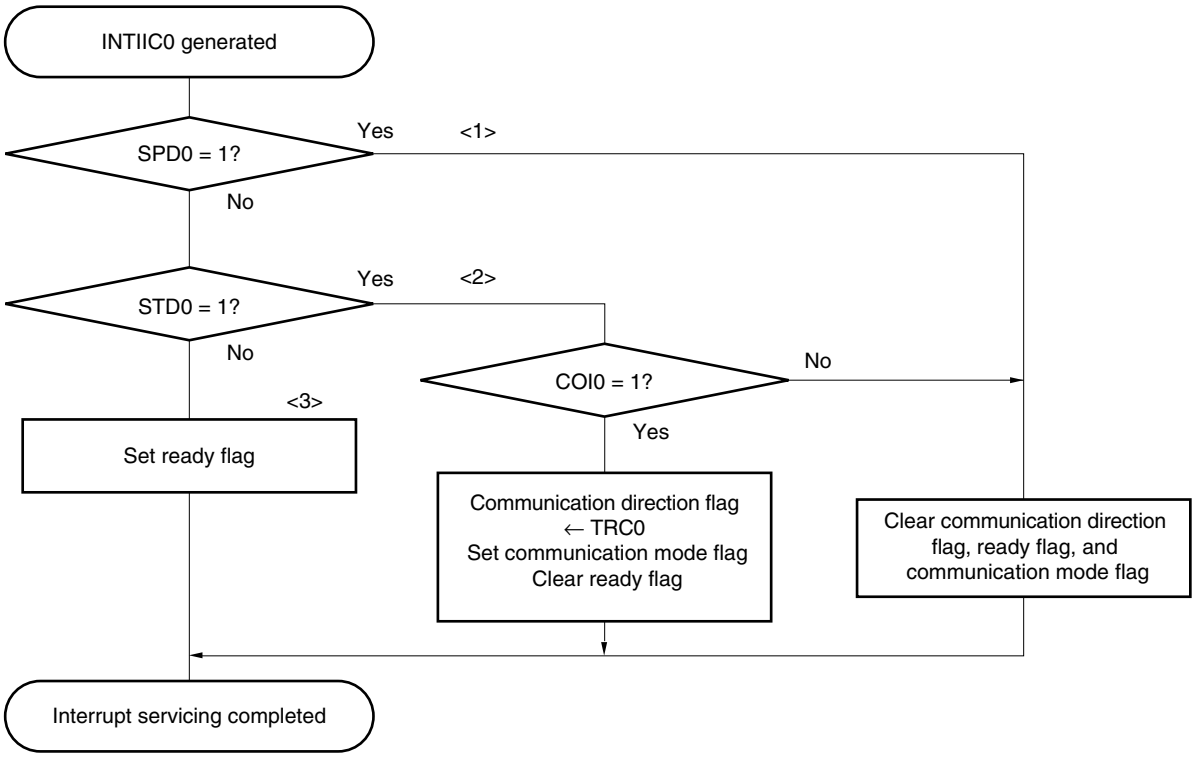
Remark X: Don't care

An example of the processing procedure of the slave with the INTIIC0 interrupt is explained below (processing is performed assuming that no extension code is used). The INTIIC0 interrupt checks the status, and the following operations are performed.

<1> Communication is stopped if the stop condition is issued.
<2> If the start condition is issued, the address is checked and communication is completed if the address does not match. If the address matches, the communication mode is set, wait is cancelled, and processing returns from the interrupt (the ready flag is cleared).
<3> For data transmit/receive, only the ready flag is set. Processing returns from the interrupt with the I^2C bus remaining in the wait state.

Remark <1> to <3> above correspond to <1> to <3> in **Figure 14-27 Slave Operation Flowchart (2)**.

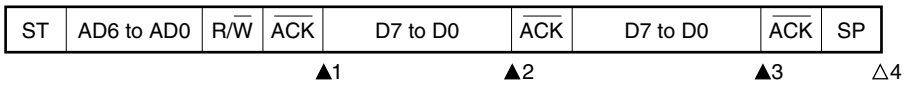
Figure 14-27. Slave Operation Flowchart (2)



(2) Slave device operation (slave address data reception)

(a) Start ~ Address ~ Data ~ Data ~ Stop

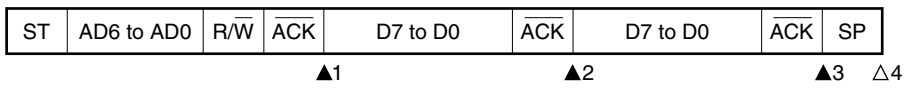
(i) When WTIM0 = 0



▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001×000B
▲3: IICS0 = 0001×000B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1

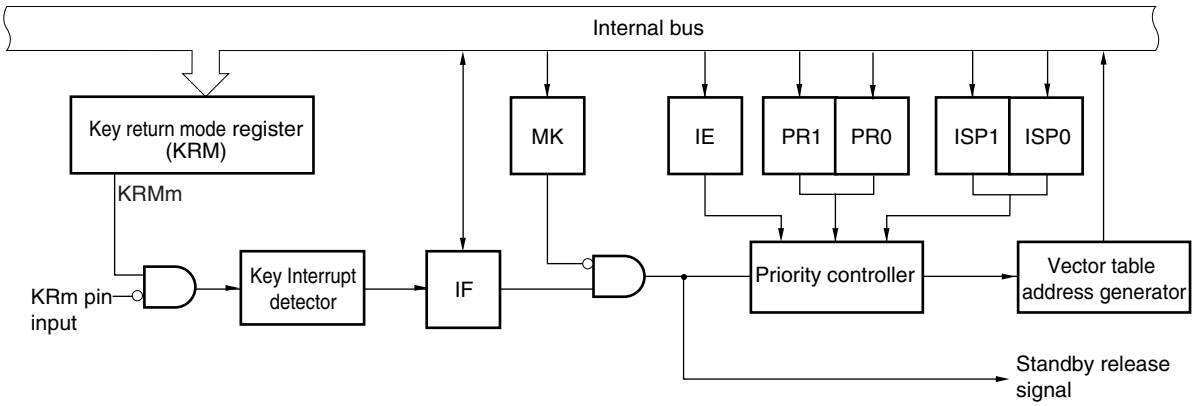


▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001×100B
▲3: IICS0 = 0001××00B
△4: IICS0 = 00000001B

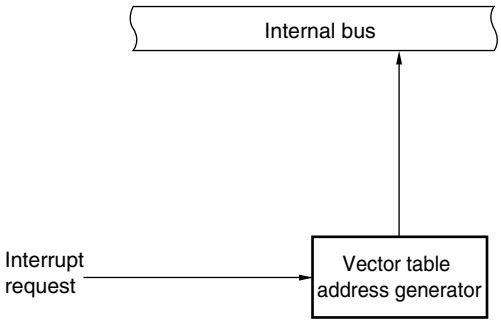
Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 17-1. Basic Configuration of Interrupt Function (2/2)

<R> **(C) External maskable interrupt (INTKR)**



(D) Software interrupt

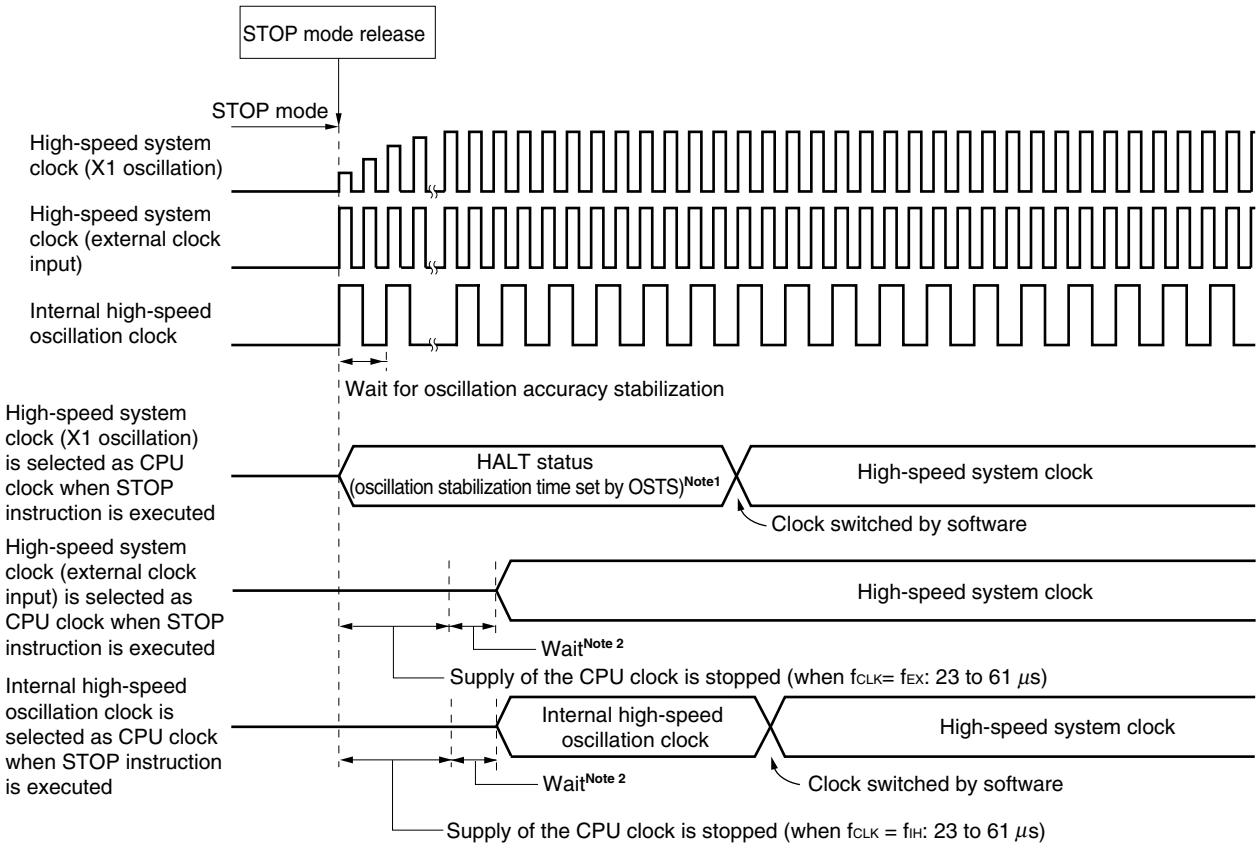


Remarks 1. IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

2. m = 0 to 7

(2) STOP mode release

Figure 19-5. Operation Timing When STOP Mode Is Released (Release by Unmasked Interrupt Request)



Notes 1. When the oscillation stabilization time set by OSTS is equal to or shorter than 61 μs, the HALT status is retained to a maximum of "61μs + wait time."

2. The wait time is as follows:

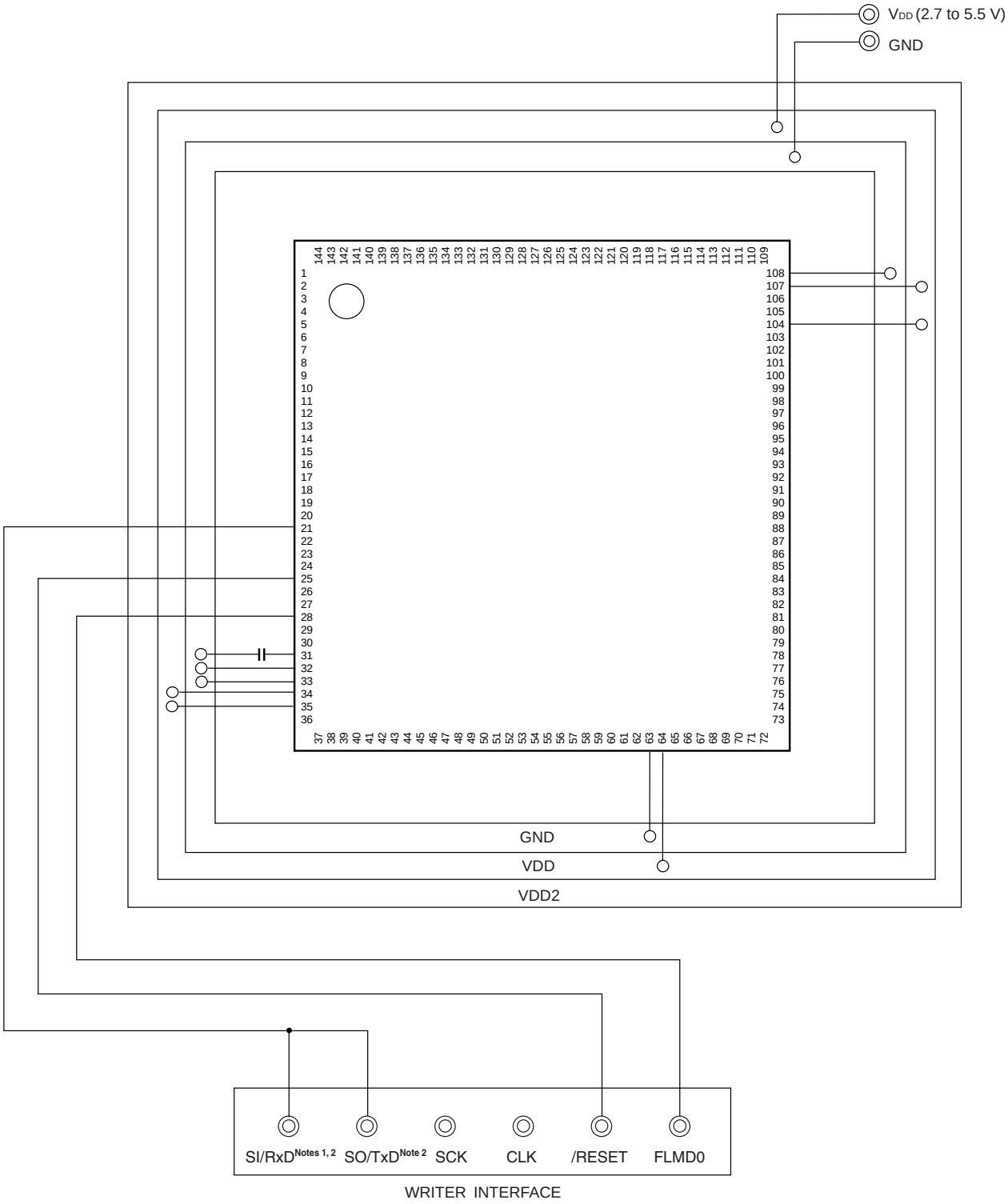
- When vectored interrupt servicing is carried out: 10 to 12 clocks
- When vectored interrupt servicing is not carried out: 5 or 6 clocks

Remark f_{EX}: External main system clock frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

The STOP mode can be released by the following two sources.

Examples of the recommended connection when using the adapter for flash memory writing are shown below.

Figure 25-1. Example of Wiring Adapter for Flash Memory Writing



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

25.9 Flash Memory Programming by Self-Programming

The 78K0R/KJ3 supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the 78K0R/KJ3 self-programming library, it can be used to upgrade the program in the field.

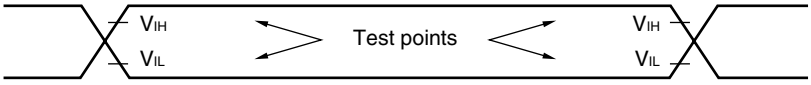
If an interrupt occurs during self-programming, self-programming can be temporarily stopped and interrupt servicing can be executed. If an unmasked interrupt request is generated in the EI state, the request branches directly from the self-programming library to the interrupt routine. After the self-programming mode is later restored, self-programming can be resumed. However, the interrupt response time is different from that of the normal operation mode.

Remark For details of the self-programming function and the 78K0R/KJ3 self-programming library, refer to **78K0R Microcontroller Self Programming Library Type01 User's Manual (U18706E)**.

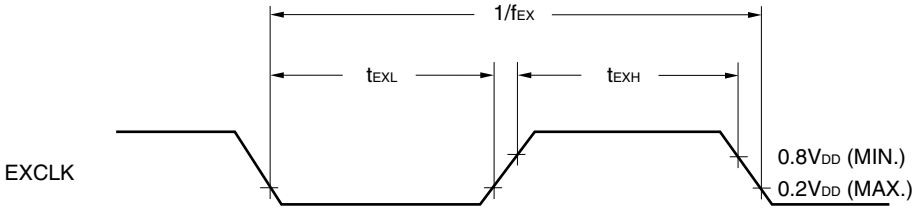
Cautions
1. **The self-programming function cannot be used when the CPU operates with the subsystem clock.**
2. **In the self-programming mode, call the self-programming start library (FlashStart).**
3. **To prohibit an interrupt during self-programming, in the same way as in the normal operation mode, execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self-programming library.**
4. **The self-programming function is disabled in the low consumption current mode. For details of the low consumption current mode, see CHAPTER 23 REGULATOR.**
5. **Disable DMA operation (DENn = 0) during the execution of self programming library functions.**

(1) Basic operation (6/6)

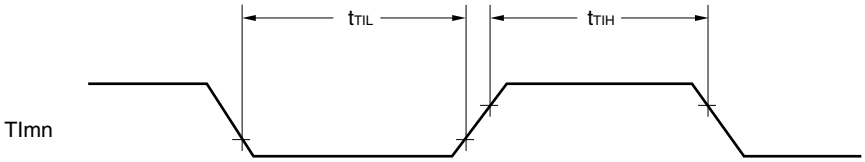
AC Timing Test Points (Excluding External Bus Interface)



External Main System Clock Timing

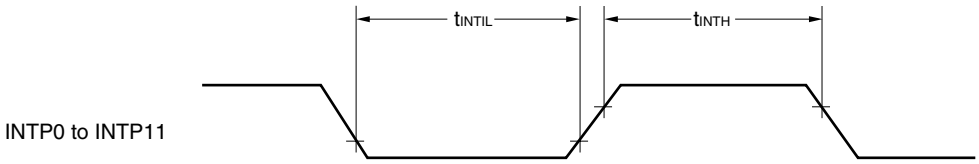


TI Timing

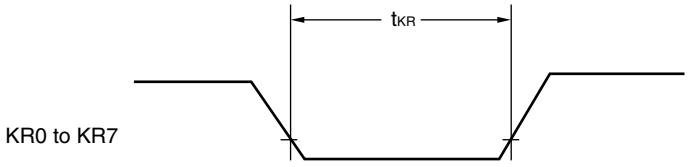


Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7), mn = 00-07, 10-13

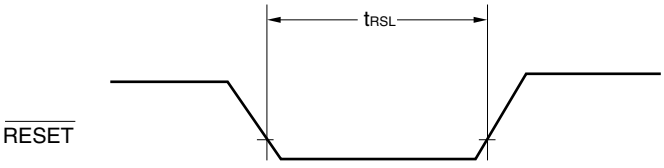
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(4) Serial interface: IIC0

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

(a) IIC0

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{SCL}	6.7 MHz ≤ f_{CLK}	0	100	0	400	kHz
		4.0 MHz ≤ f_{CLK} < 6.7 MHz	0	100	0	340	kHz
		3.2 MHz ≤ f_{CLK} < 4.0 MHz	0	100	–	–	kHz
		2.0 MHz ≤ f_{CLK} < 3.2 MHz	0	85	–	–	kHz
Setup time of restart condition[Note 1]	$t_{SU:STA}$		4.7		0.6		μs
Hold time	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCL0 = "L"	t_{LOW}		4.7		1.3		μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	CL00 = 1 and CL01 = 1	0	3.45[Note 3]	0	0.9[Note 4]	μs
				5.50[Note 5]		1.5[Note 6]	μs
		CL00 = 0 and CL01 = 0, or CL00 = 1 and CL01 = 0	0	3.45	0	0.9[Note 7]	μs
						0.95[Note 8]	μs
		CL00 = 0 and CL01 = 1	0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. When 3.2 MHz ≤ f_{CLK} ≤ 4.19 MHz.

4. When 6.7 MHz ≤ f_{CLK} ≤ 8.38 MHz.

5. When 2.0 MHz ≤ f_{CLK} < 3.2 MHz. At this time, use the SCL0 clock within 85 kHz.

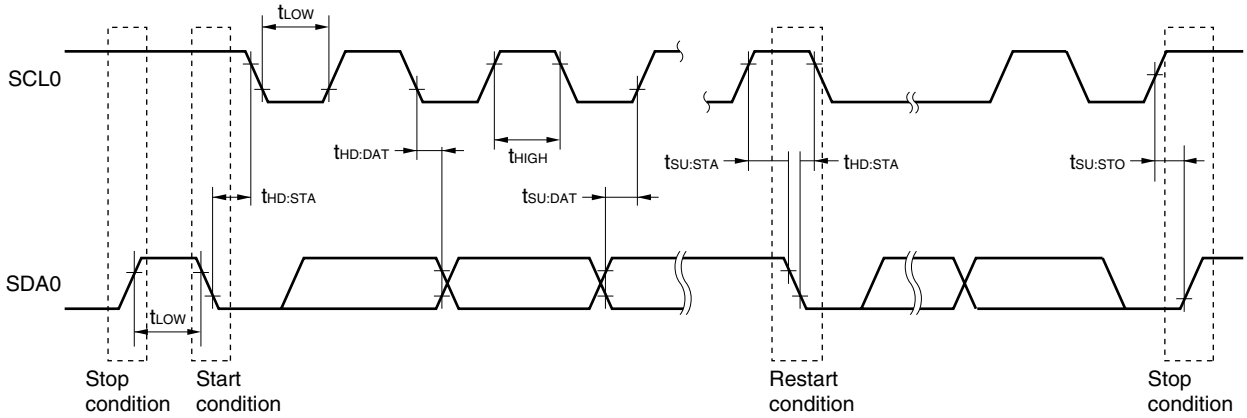
6. When 4.0 MHz ≤ f_{CLK} < 6.7 MHz. At this time, use the SCL0 clock within 340 kHz.

7. When 8.0 MHz ≤ f_{CLK} ≤ 16.76 MHz.

8. When 7.6 MHz ≤ f_{CLK} < 8.0 MHz.

Remark CL00, CL01, DFC0: Bits 0, 1, and 2 of the IIC clock select register 0 (IICCL0)

IIC0 serial transfer timing



A.5 Debugging Tools (Hardware)

A.5.1 When using in-circuit emulator QB-78K0RKX3

QB-78K0KX3[Note] In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0R/Kx3. It supports to the integrated debugger (ID78K0R-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-144-CA-01 Check pin adapter	This check pin adapter is used in waveform monitoring using the oscilloscope, etc.
QB-144-EP-02S Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-144GJ-EA-05T Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector.
QB-144GJ-YS-01T Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator.
QB-144GJ-YQ-01T YQ connector	This YQ connector is used to connect the target connector and exchange adapter.
QB-144GJ-HQ-01T Mount adapter	This mount adapter is used to mount the target device with socket.
QB-144GJ-NQ-01T Target connector	This target connector is used to mount on the target system.

Remarks 1. The QB-78K0RKX3 is supplied with a power supply unit and USB interface cable. As control software, integrated debugger ID78K0R-QB and on-chip debug emulator with programming function QB-MINI2 are supplied.

2. The packed contents differ depending on the part number, as follows.

Packed Contents / Part Number	In-Circuit Emulator	Emulation Probe	Exchange Adapter	YQ Connector	Target Connector
QB-78K0RKX3-ZZZ	QB-78K0RKX3	None			
QB-78K0RKX3-T144GJ		QB-144-EP-02S	QB-144GJ-EA-05T	QB-144GJ-YQ-01T	QB-144GJ-NQ-01T

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 22	Hard	Low-voltage detector	Cautions for low-voltage detector	There is some delay from the time supply voltage (V_{DD}) < LVI detection voltage (V_{LVI}) until the time LVI reset has been generated. In the same way, there is also some delay from the time LVI detection voltage (V_{LVI}) ≤ supply voltage (V_{DD}) until the time LVI reset has been released (see Figure 22-12). See the timing in Figure 21-2 (2) When LVI is ON upon power application (option byte: LVIOFF = 0) for the reset processing time until the normal operation is entered after the LVI reset is released.	p.731 ☐
Chapter 23	Soft	Regulator	RMC: Regulator mode control register	The RMC register can be rewritten only in the low consumption current mode (refer to Table 23-1). In other words, rewrite this register during CPU operation with the subsystem clock (f_{XT}) while the high-speed system clock (f_{MX}) and internal high-speed oscillation clock (f_{IH}) are both stopped.	p.732 ☐
				When using the setting fixed to the low consumption current mode, the RMC register can be used in the following cases. <When X1 clock is selected as the CPU clock> $f_X \leq 5$ MHz and $f_{CLK} \leq 5$ MHz <When the internal high-speed oscillation clock, external input clock, or subsystem clock are selected for the CPU clock> $f_{CLK} \leq 5$ MHz	p.732 ☐
				The self-programming function is disabled in the low consumption current mode.	p.732 ☐
Chapter 24	Soft	Option byte	–	Be sure to set FFH to 000C2H (000C2H/010C2H when the boot swap operation is used).	p.734 ☐
			000C0H/010C0H	Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.	p.734 ☐
			000C1H/010C1H	Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.	p.734 ☐
			000C2H/010C2H	Set FFH to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.	p.734 ☐
			000C3H/010C3H	Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.	p.735 ☐
			000C0H/010C0H	The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.	p.736 ☐
			000C1H/010C1H	Be sure to set bits 7 to 1 to “1”.	p.736 ☐
				Even when the LVI default start function is used, if it is set to LVI operation prohibition by the software, it operates as follows: • Does not perform low-voltage detection during LVION = 0. • If a reset is generated while LVION = 0, LVION will be re-set to 1 when the CPU starts after reset release. There is a period when low-voltage detection cannot be performed normally, however, when a reset occurs due to WDT and illegal instruction execution. This is due to the fact that while the pulse width detected by LVI must be 200 μs max., LVION = 1 is set upon reset occurrence, and the CPU starts operating without waiting for the LVI stabilization time.	p.736 ☐
			000C3H/010C3H	Bits 7 and 0 (OCDENSET and OCDERSD) can only be specified a value. Be sure to set 000010B to bits 6 to 1.	p.737 ☐
			Setting of option byte	To specify the option byte by using assembly language, use OPT_BYTE as the relocation attribute name of the CSEG pseudo instruction. To specify the option byte to 010C0H to 010C3H in order to use the boot swap function, use the relocation attribute AT to specify an absolute address.	p.738 ☐