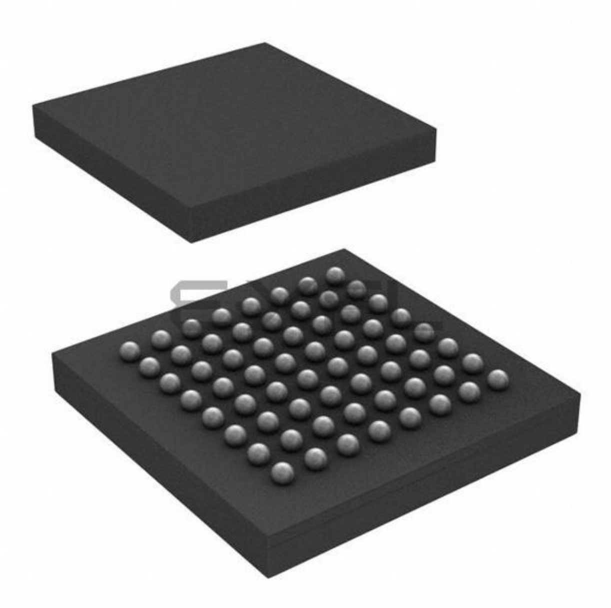

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f078rbh6tr

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3 Functional overview

Figure 1 shows the general block diagram of the STM32F078CB/RB/VB devices.

3.1 ARM®-Cortex®-M0 core

The ARM® Cortex®-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F078CB/RB/VB devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 128 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10 or I²C on pins PB6/PB7 or through the USB DFU interface.

sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 2. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 3. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 25: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F078CB/RB/VB devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 23 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation

Table 5. Number of capacitive sensing channels available on STM32F078CB/RB/VB devices (continued)

Analog I/O group	Number of capacitive sensing channels		
	STM32F078Vx	STM32F078Rx	STM32F078Cx
G5	3	3	3
G6	3	3	3
G7	3	0	0
G8	3	0	0
Number of capacitive sensing channels	23	17	16

3.14 Timers and watchdogs

The STM32F078CB/RB/VB devices include up to six general-purpose timers, two basic timers and an advanced control timer.

Table 6 compares the features of the different timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	integer from 1 to 65536	No	1	-
	TIM15	16-bit	Up	integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	integer from 1 to 65536	Yes	-	-

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Universal serial bus (USB)

The STM32F078CB/RB/VB embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.21 Clock recovery system (CRS)

The STM32F078CB/RB/VB embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.22 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Figure 4. LQFP100 package pinout

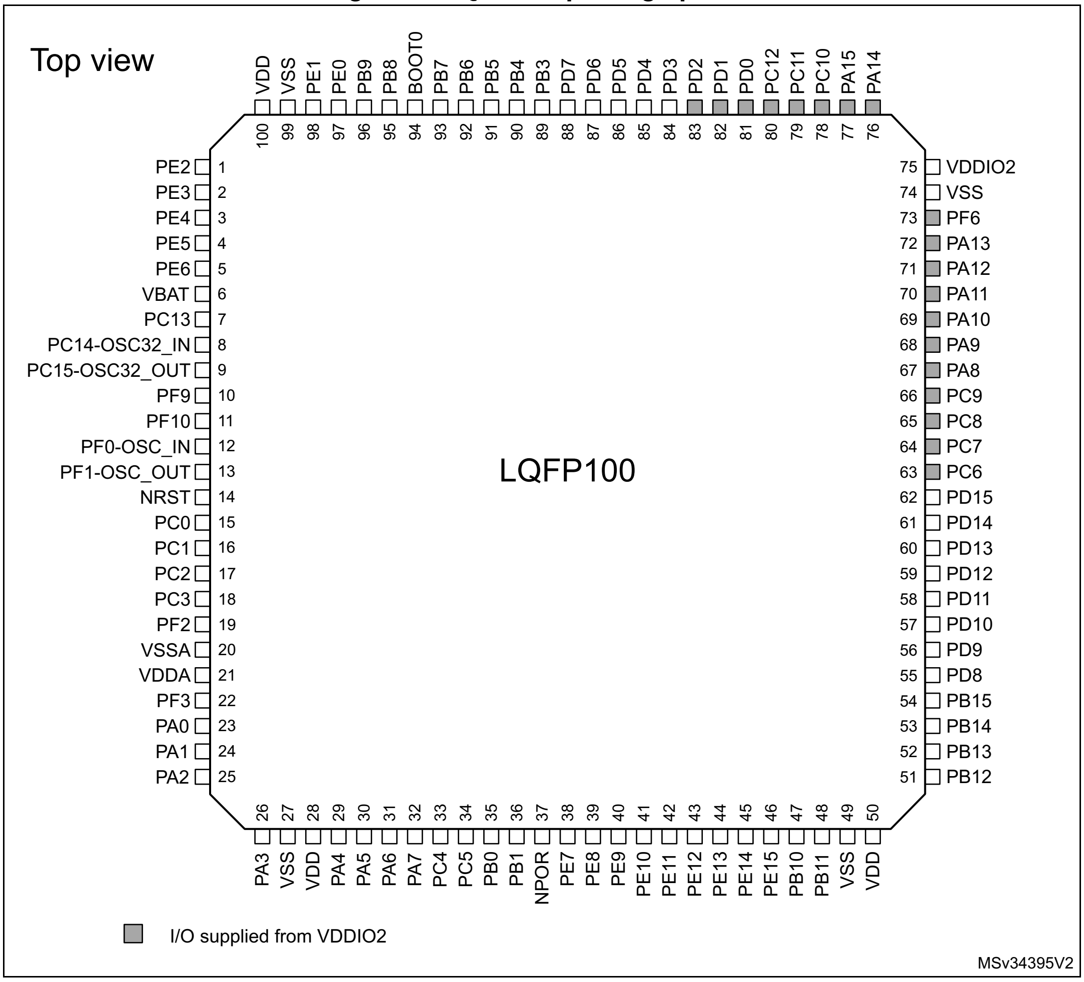


Table 19. STM32F078CB/RB/VB peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6400 - 0x4000 6BFF	2 KB	Reserved
	0x4000 6000 - 0x4000 63FF	1 KB	USB RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics* and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 20. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage	–0.3	1.95	V
$V_{DDIO2}–V_{SS}$	External I/O supply voltage	- 0.3	4.0	V
$V_{DDA}–V_{SS}$	External analog supply voltage	- 0.3	4.0	V
$V_{DD}–V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
$V_{BAT}–V_{SS}$	External backup supply voltage	- 0.3	4.0	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DDIOx} + 4.0 (3)	V
	Input voltage on POR pins	V_{SS} –0.3	4.0	V
	Input voltage on TTa pins	V_{SS} –0.3	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	V_{SS} –0.3	4.0	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 21: Current characteristics*for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 30. Typical and maximum consumption in Stop mode

Symbol	Parameter	Conditions	Typ @ V_{DDA} (V_{DD} = 1.8 V)							Max			Unit
			= 1.8 V	= 2.0 V	= 2.4 V	= 2.7 V	= 3.0 V	= 3.3 V	= 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	All oscillators OFF	0.5							2.1	15.4	37.0	µA
I_{DDA}			1.0	1.0	1.0	1.0	1.1	1.1	1.2	1.6	2.6	3.4	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 50: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 32: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

6.3.5 Wakeup time from low-power mode

The wakeup times given in *Table 33* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode.

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 33. Low-power mode wakeup timings

Symbol	Parameter	Typ @ V_{DDA}		Max	Unit
		= 1.8 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	3.5	2.8	5.3	µs
$t_{WUSLEEP}$	Wakeup from Sleep mode	4 SYSCLK cycles		-	µs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 14: High-speed external clock source AC timing diagram*.

Table 34. High-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	V
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

Table 49. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 and PF1 pins	–0	NA	mA
	Injected current on PC0 pin	–0	+5	
	Injected current on PA11 and PA12 pins with induced leakage current on adjacent pins less than -1 mA	–5	NA	
	Injected current on all other FT and FTf pins, and on POR pin	–5	NA	
	Injected current on all other TTa, TC and RST pins	–5	+5	

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 23: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 50. I/O static characteristics

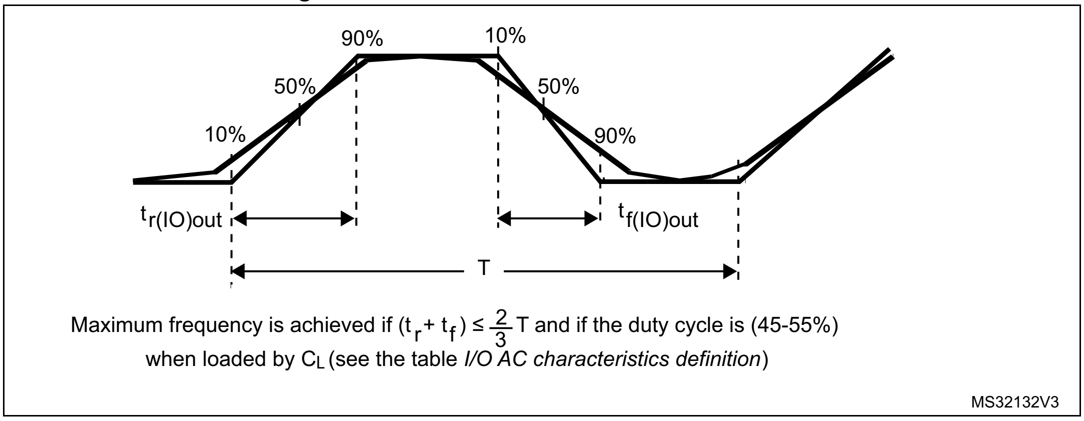
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DDIOx}+0.07(1)	V
		FT and FTf I/O	-	-	0.475 V_{DDIOx}–0.2(1)	
		BOOT0	-	-	0.3 V_{DDIOx}–0.3(1)	
		All I/Os except BOOT0 pin	-	-	0.3 V_{DDIOx}	
V_{IH}	High level input voltage	TC and TTa I/O	0.445 V_{DDIOx}+0.398(1)	-	-	V
		FT and FTf I/O	0.5 V_{DDIOx}+0.2(1)	-	-	
		BOOT0	0.2 V_{DDIOx}+0.95(1)	-	-	
		All I/Os except BOOT0 pin	0.7 V_{DDIOx}	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
		BOOT0	-	300(1)	-	

Table 52. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
Fm+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	12	ns
	$t_{r(IO)out}$	Output rise time		-	34	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	0.5	MHz
	$t_{f(IO)out}$	Output fall time		-	16	ns
	$t_{r(IO)out}$	Output rise time		-	44	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 23*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 23. I/O AC characteristics definition



6.3.14 NRST and NPOR pin characteristics

NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

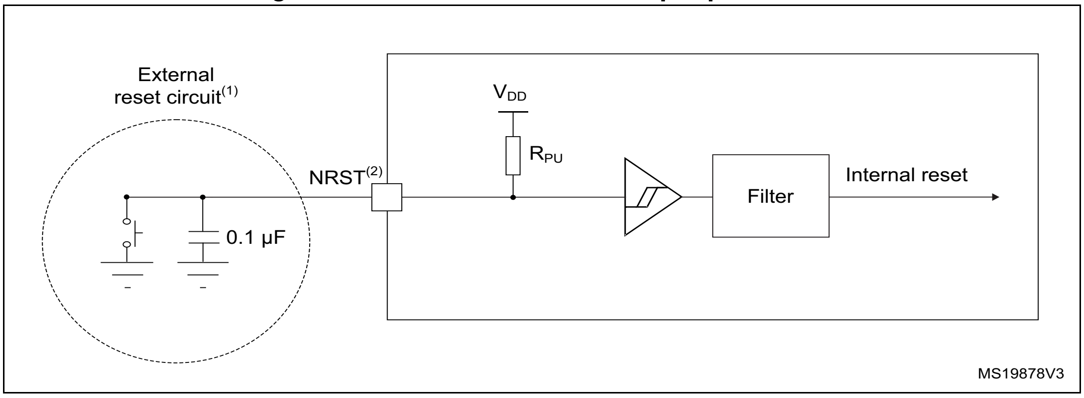
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 V_{DD}+0.07(1)	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.445 V_{DD}+0.398(1)	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	700(1)	-	-	ns

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 24. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

NPOR pin characteristics

The NPOR pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor to the V_{DDA}, R_{PU}.

Unless otherwise specified, the parameters given in *Table 54* below are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

6.3.18 Temperature sensor characteristics

Table 60. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{30}	Voltage at 30 °C (± 5 °C)[2]	1.34	1.43	1.52	V
t_{START}[1]	ADC_IN16 buffer startup time	-	-	10	µs
t_{S_temp}[1]	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 2: Temperature sensor calibration values*.

6.3.19 V_{BAT} monitoring characteristics

Table 61. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	kΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er[1]	Error on Q	–1	-	+1	%
t_{S_vbat}[1]	ADC sampling time when reading the V_{BAT}	4	-	-	µs

1. Guaranteed by design, not tested in production.

6.3.20 Timer characteristics

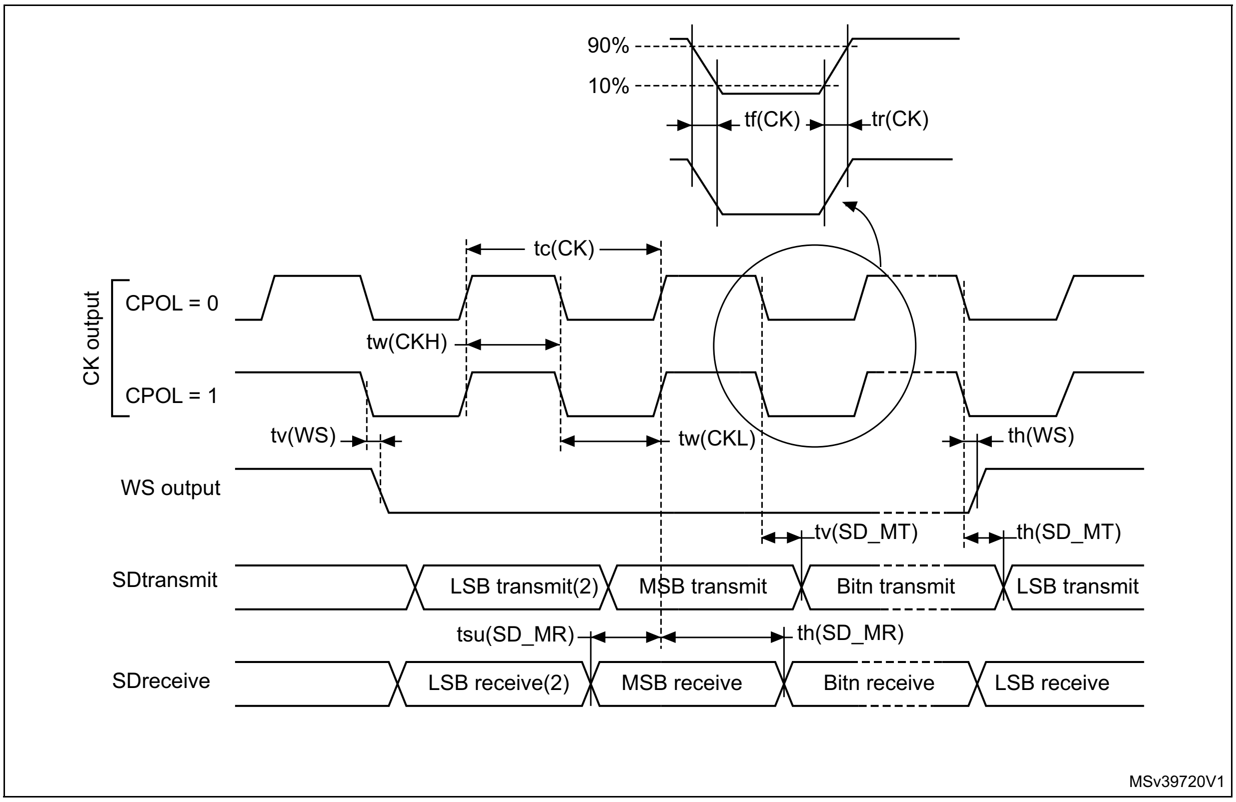
The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 62. TIMx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	1365	-	µs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	-	s

Figure 33. I²S master timing diagram (Philips protocol)



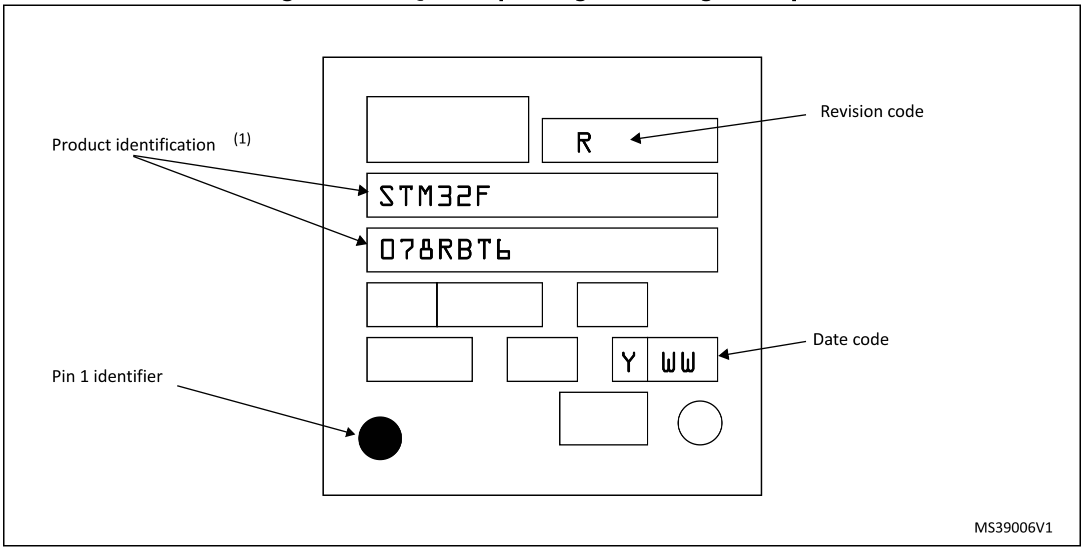
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LQFP64 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 51* to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

Figure 51. LQFP64 P_D max versus T_A