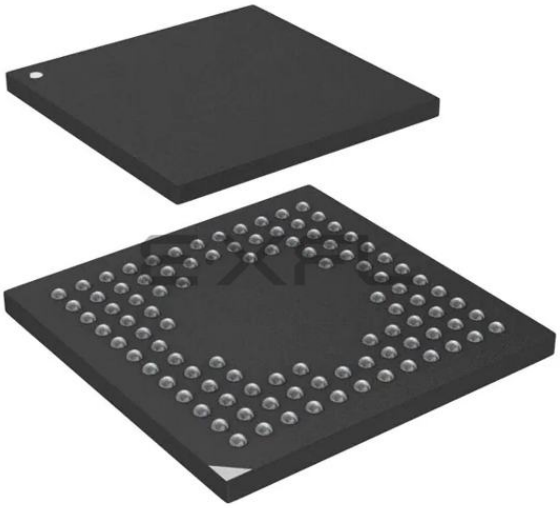


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f078vbh6

List of figures

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion

Six DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 25: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F078CB/RB/VB devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 23 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation

Figure 7. UFQFPN48 package pinout

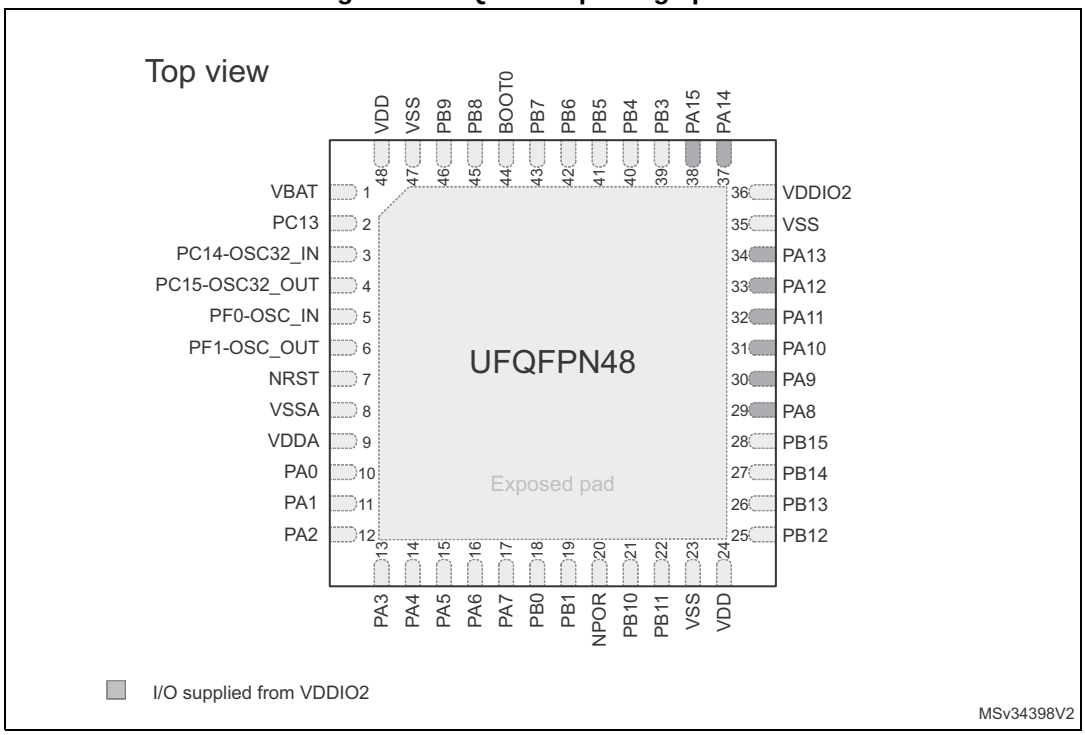
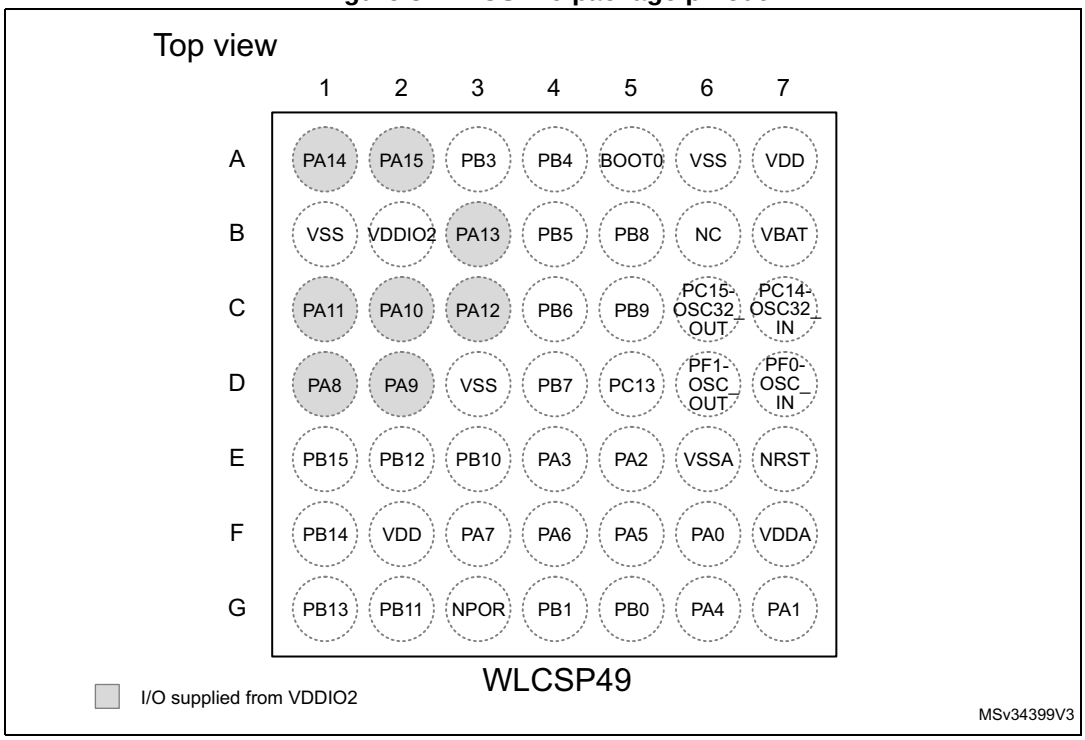


Figure 8. WLCSP49 package pinout



1. The above figure shows the package in top view, changing from bottom view in the previous document versions.

Table 12. STM32F078CB/RB/VB pin definitions (continued)

Pin numbers					Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
UFBGA100	LQFP100	LQFP64	LQFP48/UFQFPN48	WLCSP49					Alternate functions	Additional functions
M2	24	15	11	G7	PA1	I/O	TTa	-	USART2_RTS, TIM2_CH2, TIM15_CH1N, TSC_G1_IO2, USART4_RX, EVENTOUT	ADC_IN1, COMP1_INP
K3	25	16	12	E5	PA2	I/O	TTa	-	USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3	ADC_IN2, COMP2_OUT, COMP2_INM6, WKUP4
L3	26	17	13	E4	PA3	I/O	TTa	-	USART2_RX,TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP
D3	27	18	-	-	VSS	S	-	-	Ground	
H3	28	19	-	-	VDD	S	-	-	Digital power supply	
M3	29	20	14	G6	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT1
K4	30	21	15	F5	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2	COMP1_INM5, COMP2_INM5, ADC_IN5, DAC_OUT2
L4	31	22	16	F4	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT, USART3_CTS	ADC_IN6
M4	32	23	17	F3	PA7	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
K5	33	24	-	-	PC4	I/O	TTa	-	EVENTOUT, USART3_TX	ADC_IN14
L5	34	25	-	-	PC5	I/O	TTa	-	TSC_G3_IO1, USART3_RX	ADC_IN15, WKUP5
M5	35	26	18	G5	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT, USART3_CK	ADC_IN8

Table 17. Alternate functions selected through GPIOE_AFR registers for port E

Pin name	AF0	AF1
PE0	TIM16_CH1	EVENTOUT
PE1	TIM17_CH1	EVENTOUT
PE2	TIM3_ETR	TSC_G7_IO1
PE3	TIM3_CH1	TSC_G7_IO2
PE4	TIM3_CH2	TSC_G7_IO3
PE5	TIM3_CH3	TSC_G7_IO4
PE6	TIM3_CH4	-
PE7	TIM1_ETR	-
PE8	TIM1_CH1N	-
PE9	TIM1_CH1	-
PE10	TIM1_CH2N	-
PE11	TIM1_CH2	-
PE12	TIM1_CH3N	SPI1_NSS, I2S1_WS
PE13	TIM1_CH3	SPI1_SCK, I2S1_CK
PE14	TIM1_CH4	SPI1_MISO, I2S1_MCK
PE15	TIM1_BKIN	SPI1_MOSI, I2S1_SD

Table 18. Alternate functions available on port F

Pin name	AF
PF0	CRS_SYNC
PF1	-
PF2	EVENTOUT
PF3	EVENTOUT
PF6	-
PF9	TIM15_CH1
PF10	TIM15_CH2

Table 19. STM32F078CB/RB/VB peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6400 - 0x4000 6BFF	2 KB	Reserved
	0x4000 6000 - 0x4000 63FF	1 KB	USB RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	2 KB	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics* and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 20. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	–0.3	1.95	V
V_{DDIO2}–V_{SS}	External I/O supply voltage	- 0.3	4.0	V
V_{DDA}–V_{SS}	External analog supply voltage	- 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{BAT}–V_{SS}	External backup supply voltage	- 0.3	4.0	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DDIOx} + 4.0 (3)	V
	Input voltage on POR pins	V_{SS} –0.3	4.0	V
	Input voltage on TTa pins	V_{SS} –0.3	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	V_{SS} –0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 21: Current characteristics*for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 1.8$ V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 29. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	f_{HCLK}	Typical consumption in Run mode		Typical consumption in Sleep mode		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I_{DD}	Current consumption from V_{DD} supply	48 MHz	22.0	12.7	14.2	3.2	mA
		36 MHz	17.1	9.9	10.8	2.5	
		32 MHz	15.4	8.9	9.7	2.2	
		24 MHz	11.9	7.0	7.5	1.8	
		16 MHz	8.3	4.9	5.2	1.3	
		8 MHz	4.4	2.7	2.7	0.7	
		4 MHz	2.7	1.7	1.8	0.6	
		2 MHz	1.6	1.1	1.2	0.6	
		1 MHz	1.1	0.8	0.9	0.5	
		500 kHz	0.9	0.7	0.8	0.5	
I_{DDA}	Current consumption from V_{DDA} supply	48 MHz	143				µA
		36 MHz	112				
		32 MHz	102				
		24 MHz	81				
		16 MHz	59				
		8 MHz	1				
		4 MHz	1				
		2 MHz	1				
		1 MHz	1				
		500 kHz	1				

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 32*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 20: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 32*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 32. Peripheral current consumption

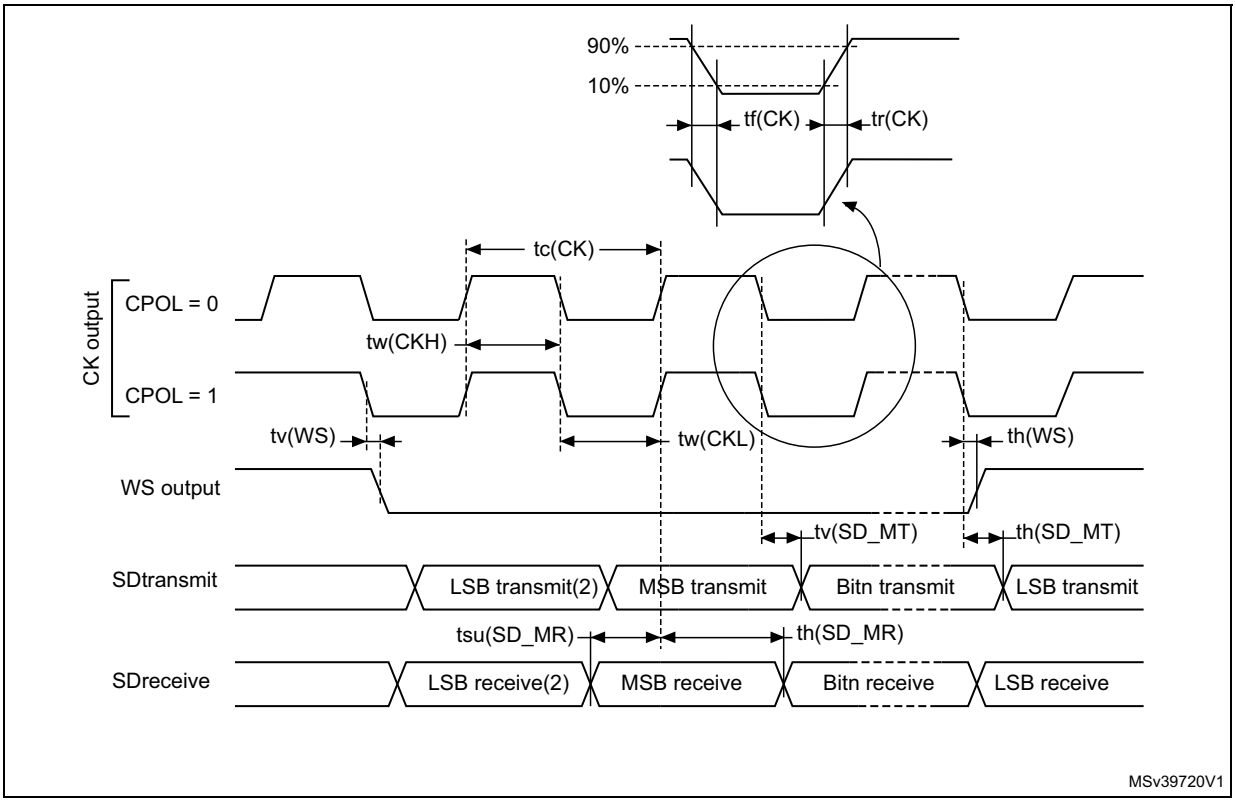
Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix(1)	2.2	µA/MHz
	CRC	1.6	
	DMA	5.7	
	Flash memory interface	13.0	
	GPIOA	8.2	
	GPIOB	8.5	
	GPIOC	2.3	
	GPIOD	1.9	
	GPIOE	2.2	
	GPIOF	1.2	
	SRAM	0.9	
	TSC	5.0	
	All AHB peripherals	**52.6**	

Table 32. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB	APB-Bridge(2)	2.8	µA/MHz
	ADC(3)	4.1	
	CEC	1.5	
	CRS	0.8	
	DAC(3)	4.7	
	DEBUG (MCU debug feature)	0.1	
	I2C1	3.9	
	I2C2	4.0	
	PWR	1.3	
	SPI1	8.7	
	SPI2	8.5	
	SYSCFG & COMP	1.7	
	TIM1	14.9	
	TIM2	15.5	
	TIM3	11.4	
	TIM6	2.5	
	TIM7	2.3	
	TIM14	5.3	
	TIM15	9.1	
	TIM16	6.6	
	TIM17	6.8	
	USART1	17.0	
	USART2	16.7	
	USART3	5.4	
	USART4	5.4	
	USB	7.2	
	WWDG	1.4	
	All APB peripherals	**169.6**	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, is not included. Refer to the tables of characteristics in the subsequent sections.

Figure 33. I²S master timing diagram (Philips protocol)



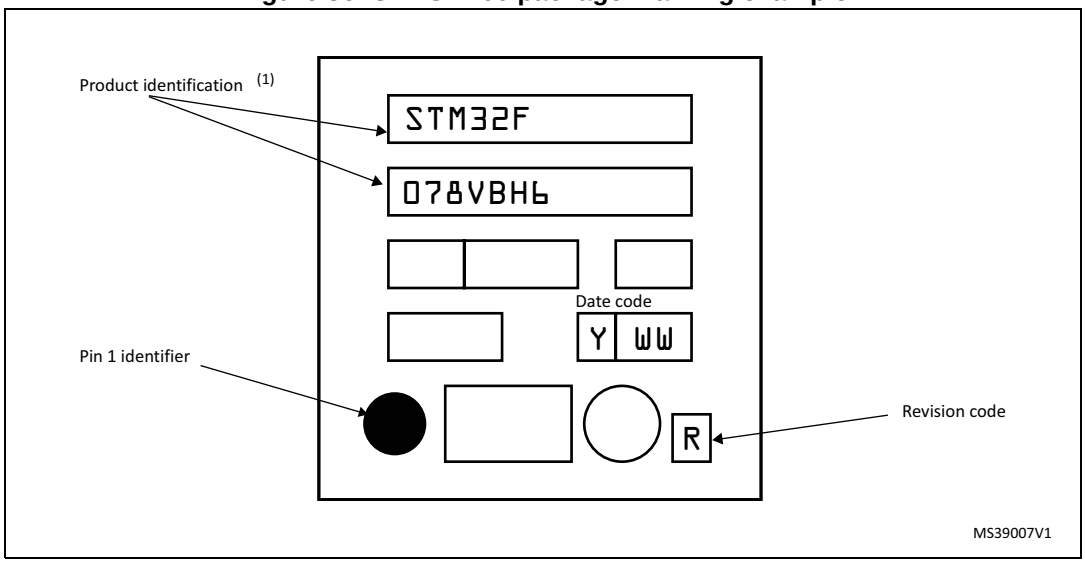
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 36. UFBGA100 package marking example

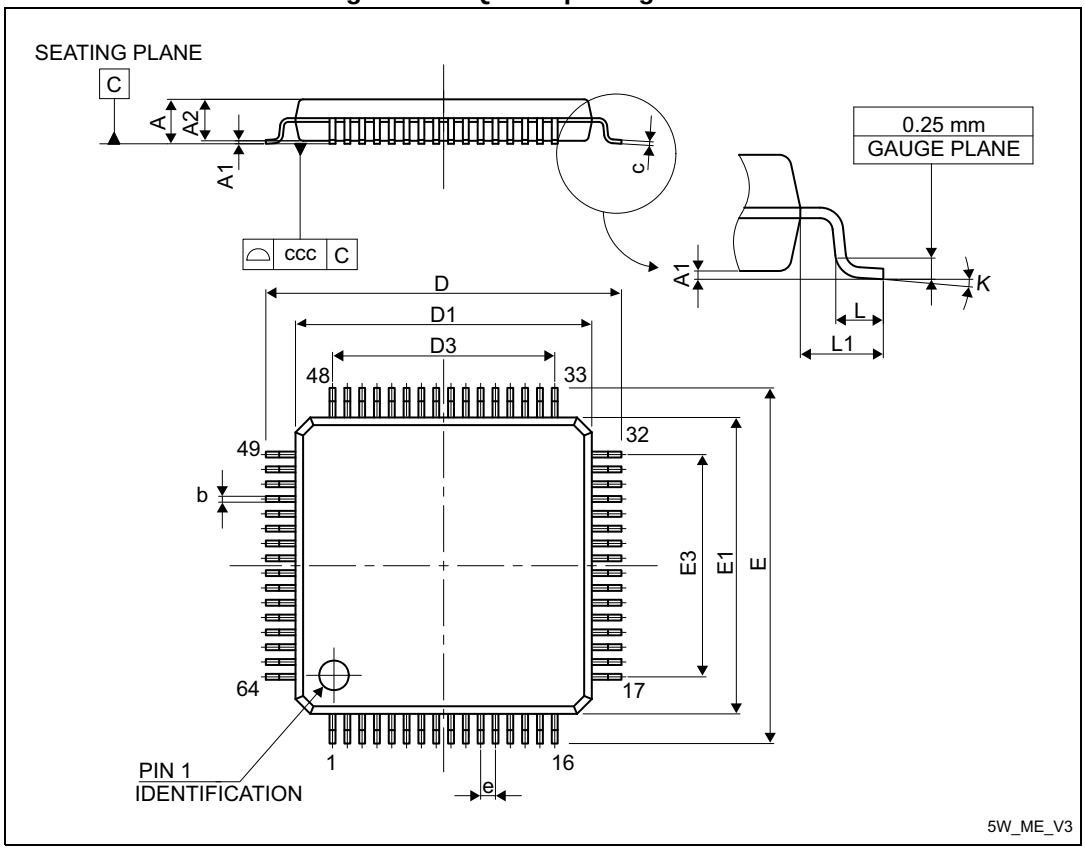


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 40. LQFP64 package outline



1. Drawing is not to scale.

Table 72. LQFP64 package mechanical data

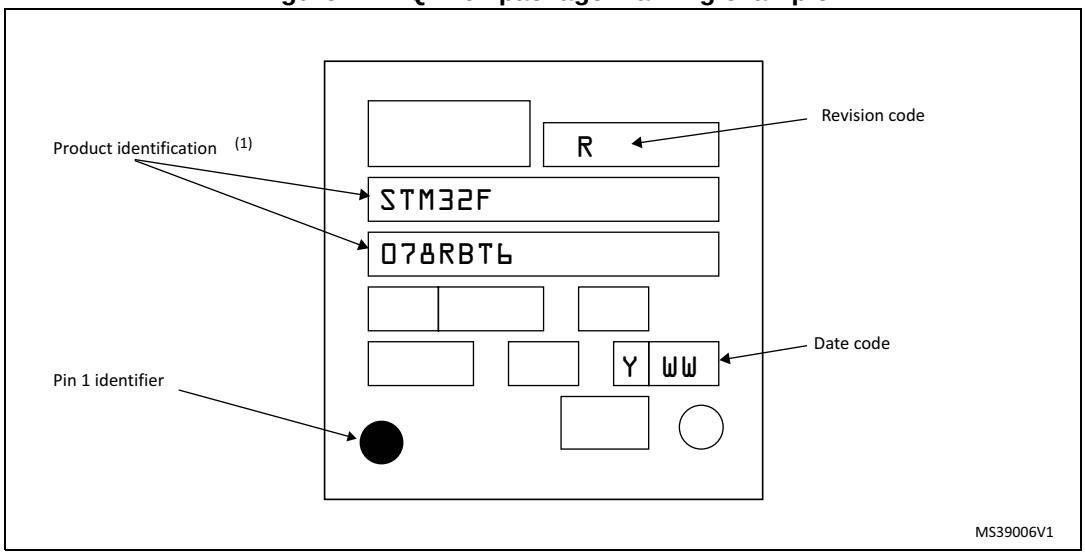
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LQFP64 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 73. WLCSP49 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.242	3.277	3.312	0.1276	0.1290	0.1304
E	3.074	3.109	3.144	0.1210	0.1224	0.1238
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.4385	-	-	0.0173	-
G	-	0.3545	-	-	0.0140	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 23: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 76. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	44	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	54	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	32	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	49	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

9 Revision history

Table 78. Document revision history

Date	Revision	Changes
03-Apr-2014	1	Internal
28-May-2014	2	Initial release
17-Dec-2015	3	**Cover page:** – part numbers moved to title and table of part numbers removed – generic product name updated as STM32F078CB/RB/VB ***Section 2: Description*:** – *Figure 1: Block diagram* updated ***Section 3: Functional overview*:** – *Figure 2: Clock tree* updated – *Section 3.5.3: Low-power modes* - added information on peripherals configurable to operate with HSI ***Section 4: Pinouts and pin descriptions*:** – Package pinout figures updated (look and feel) – *Figure 8: WLCSP49 package pinout* - **now presented in top view** ***Section 5: Memory mapping*:** – *Figure 9: STM32F078CB/RB/VB memory map* updated ***Section 6: Electrical characteristics*:** – *Table 20: Voltage characteristics and Table 21: Current characteristics updated* – *Table 23: General operating conditions - added footnote for V_{IN} of TTa I/O* – *Table 25: Embedded internal reference voltage*: added t_{START} parameter and removed -40°-to-85° condition and associated note for V_{REFINT} – *Merger of tables 33 and 34 into Table 29: Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal* – *Table 38: HSI oscillator characteristics and Figure 18: HSI oscillator accuracy characterization results for soldered parts* updated – *Table 39: HSI14 oscillator characteristics: changed min values for ACC_{HSI14}, added test conditions* – *Table 47: ESD absolute maximum ratings* updated – *Table 50: I/O static characteristics* - note removed – *Table 55: ADC characteristics* - updated some parameter values, test conditions and added footnotes (3) and (4) – *Table 58: DAC characteristics* - I_{DDA} max value (DAC DC current consumption) updated – *Table 59: Comparator characteristics* - min added for V_{DDA} – *Figure 28: Maximum V_{REFINT} scaler startup time from power down* added

Table 78. Document revision history (continued)

Date	Revision	Changes
17-Dec-2015	3 (continued)	– *Table 61: V_{BAT} monitoring characteristics:* changed the typical value for R parameter – *Table 67: I^2S characteristics*: table reorganized, $t_{v(SD\_ST)}$ max value updated ***Section 7: Package information*:** – information on packages generally update ***Section 8: Ordering information*:** – added tray packing to options
10-Jan-2017	4	***Section 6: Electrical characteristics*:** – *Table 37: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* - information on configuring different drive capabilities removed. See the corresponding reference manual. – *Table 25: Embedded internal reference voltage* - V_{REFINT} values – *Table 58: DAC characteristics* - min. R_{LOAD} to V_{DDA} defined – *Figure 29: SPI timing diagram - slave mode and CPHA = 0* and *Figure 30: SPI timing diagram - slave mode and CPHA = 1* enhanced and corrected ***Section 8: Ordering information*:** – The name of the section changed from the previous “Part numbering”