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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, DMA LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	76-XFBGA, WLCSP
Supplier Device Package	76-WLCSP (4.04x3.87)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4248fli-bl583t

More Information

Cypress provides a wealth of data at http://www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the introduction page for Bluetooth® Low Energy (BLE) Products. Following is an abbreviated list for PRoC BLE:

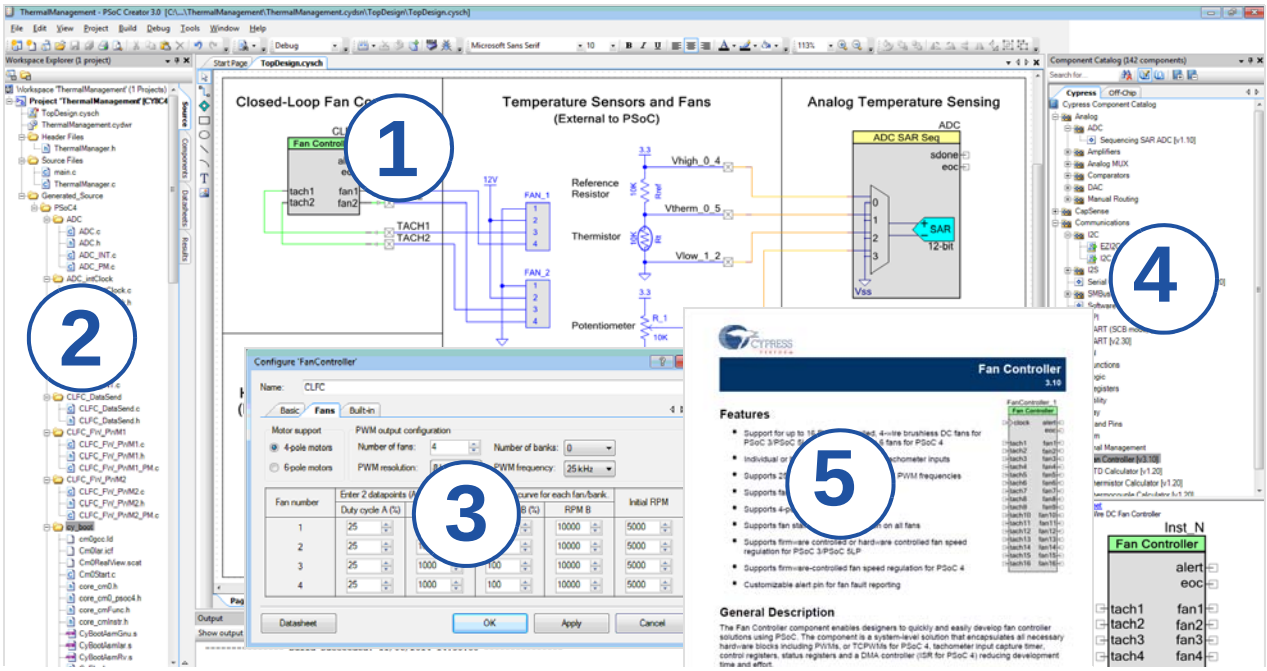
- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PRoC BLE, PSoC 4 BLE, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application Notes: Cypress offers a large number of PSoC application notes coverting a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PRoC BLE are:
  - AN94020: Getting Started with PRoC BLE
  - AN97060: PSoC 4 BLE and PRoC BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91184: PSoC 4 BLE - Designing BLE Applications
  - AN91162: Creating a BLE Custom Profile
  - AN91445: Antenna Design and RF Layout Guidelines
  - AN96841: Getting Started With EZ-BLE Module
  - AN85951: PSoC 4 CapSense Design Guide
  - AN95089: PSoC 4/PRoC BLE Crystal Oscillator Selection and Tuning Techniques
  - AN92584: Designing for Low Power and Estimating Battery Life for BLE Applications
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PRoC BLE functional block
  - Registers TRM describes each of the PRoC BLE registers
- Development Kits:
  - CY8CKIT-042-BLE Pioneer Kit, is a flexible, Arduino-compatible, Bluetooth LE development kit for PSoC 4 BLE and PRoC BLE.
  - CY5676, PRoC BLE 256KB Module, features a PRoC BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-142, PSoC 4 BLE Module, features a PSoC 4 BLE device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - CY8CKIT-143, PSoC 4 BLE 256KB Module, features a PSoC 4 BLE 256KB device, two crystals for the antenna matching network, a PCB antenna and other passives, while providing access to all GPIOs of the device.
  - The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents



Contents

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4XX8 BLE 4.2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher-performance processors such as Cortex-M3 and M4. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to the main processor to be switched off when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a nonmaskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes an SWD interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4XX8 BLE 4.2 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4XX8 BLE 4.2 device has a flash module with either 128 KB or 256 KB of flash memory, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required. Maximum erase and program time is 20 ms per row (256 bytes). This also applies to the emulated EEPROM.

SRAM

SRAM memory is retained during Hibernate.

SROM

The 8-KB supervisory ROM contains a library of executable functions for flash programming. These functions are accessed through supervisory calls (SVC) and enable in-system programming of the flash memory.

DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

The power system is described in detail in the section Power on page 16. It provides an assurance that the voltage levels are as required for the respective modes, and can either delay the mode entry (on power-on reset (POR), for example) until voltage levels are as required or generate resets (brownout detect (BOD)) or interrupts when the power supply reaches a particular programmable level between 1.8 and 4.5 V (low voltage detect (LVD)).

PSoC 4XX8 BLE 4.2 operates with a single external supply (1.71 to 5.5 V without radio, and 1.9 V to 5.5 V with radio). The device has five different power modes; transitions between these modes are managed by the power system. PSoC 4XX8 BLE 4.2 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes. Refer to the *Technical Reference Manual* for more details.

Clock System

The PSoC 4XX8 BLE 4.2 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4XX8 BLE 4.2 consists of the internal main oscillator (IMO), the internal low-speed oscillator (ILO), the 24-MHz external crystal oscillator (ECO) and the 32-kHz watch crystal oscillator (WCO). In addition, an external clock may be supplied from a pin.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 4XX8 BLE 4.2. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low-power oscillator, which is primarily used to generate clocks for the peripheral operation in the Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

External Crystal Oscillator (ECO)

The ECO is used as the active clock for the BLE subsystem to meet the ±50-ppm clock accuracy of the Bluetooth 4.2 Specification. PSoC 4XX8 BLE 4.2 includes a tunable load capacitor to tune the crystal clock frequency by measuring the actual clock frequency. The high-accuracy ECO clock can also be used as a system clock.

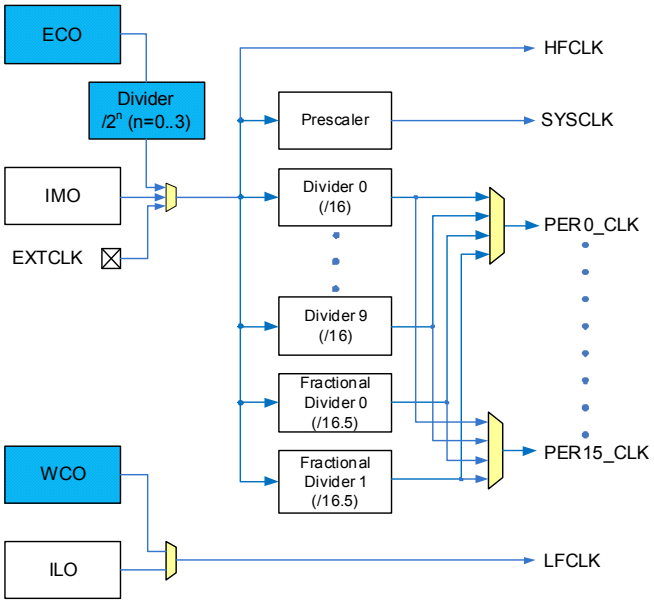
Watch Crystal Oscillator (WCO)

The WCO is used as the sleep clock for the BLE subsystem to meet the ±500-ppm clock accuracy for the Bluetooth 4.2 Specification. The sleep clock provides an accurate sleep timing and enables wakeup at the specified advertisement and connection intervals. The WCO output can be used to realize the real-time clock (RTC) function in firmware.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows the watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register. With the WCO and firmware, an accurate real-time clock (within the bounds of the 32-kHz crystal accuracy) can be realized.

Figure 3. PSoC 4XX8 BLE 4.2 MCU Clocking Architecture



The HFCLK signal can be divided down (see Figure 3) to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4XX8 BLE 4.2: ten with 16-bit divide capability and two with 16.5-bit divide capability. This allows the generation of 16 divided clock signals, which can be used by peripheral blocks. The analog clock leads the digital clocks to allow analog events to occur before the digital clock-related noise is generated. The 16-bit and 16.5-bit dividers allow a lot of flexibility in generating fine-grained frequency values and are fully supported in PSoC Creator.

Reset

PSoC 4XX8 BLE 4.2 device can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through resets and allows the software to determine the cause of the reset. An XRES pin is reserved for an external reset to avoid complications with the configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4XX8 BLE 4.2 reference system generates all internally required references. A one-percent voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or use an external reference for the SAR. Refer to Table 19, “SAR ADC AC Specifications,” on page 26 for details.

BLE Radio and Subsystem

PSoC 4XX8 BLE 4.2 incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded AES-128 security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 1 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 4.2. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

The Bluetooth Smart Radio and Subsystem (BLESS) requires a 1.9-V minimum supply (the range varies from 1.9 V to 5.5 V).

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, 3, and 4
  - Security mode 2: Level 1 and 2
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, Out of Band and Numeric Comparison
  - Authenticated man-in-the-middle (MITM) protection and data signing
  - LE Secure Connections (Bluetooth 4.2 feature)
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Encryption
  - Low-duty cycle advertising
  - LE Ping
  - LE Data Packet Length Extension (Bluetooth 4.2 feature)
  - Link Layer Privacy (with extended scanning filter policy, Bluetooth 4.2 feature)
- Supports all SIG-adopted BLE profiles

Analog Blocks

12-bit SAR ADC

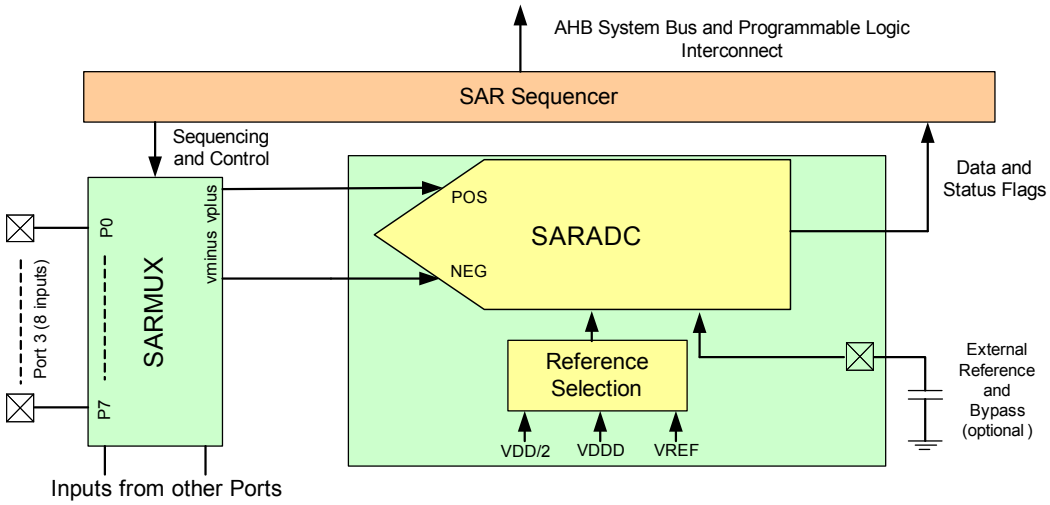
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion (up to 806 Ksps for the PSoC 41X8_BLE derivatives).

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

Figure 4. SAR ADC System Diagram



Opamps (CTBm Block)

PSoC 42X8_BLE has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip, eliminating external components. PGAs, voltage buffers, filters, transimpedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the sample-and-hold circuit of the ADC without requiring external buffering.

Temperature Sensor

PSoC 4XX8 BLE 4.2 has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

Low-Power Comparators

PSoC 4XX8 BLE 4.2 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Special-Function Peripherals

LCD Segment Drive

PSoC 4XX8 BLE 4.2 has an LCD controller, which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

The digital correlation method modulates the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

The PWM method drives the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep mode, refreshing a small display buffer (four bits; one 32-bit register per port).

CapSense

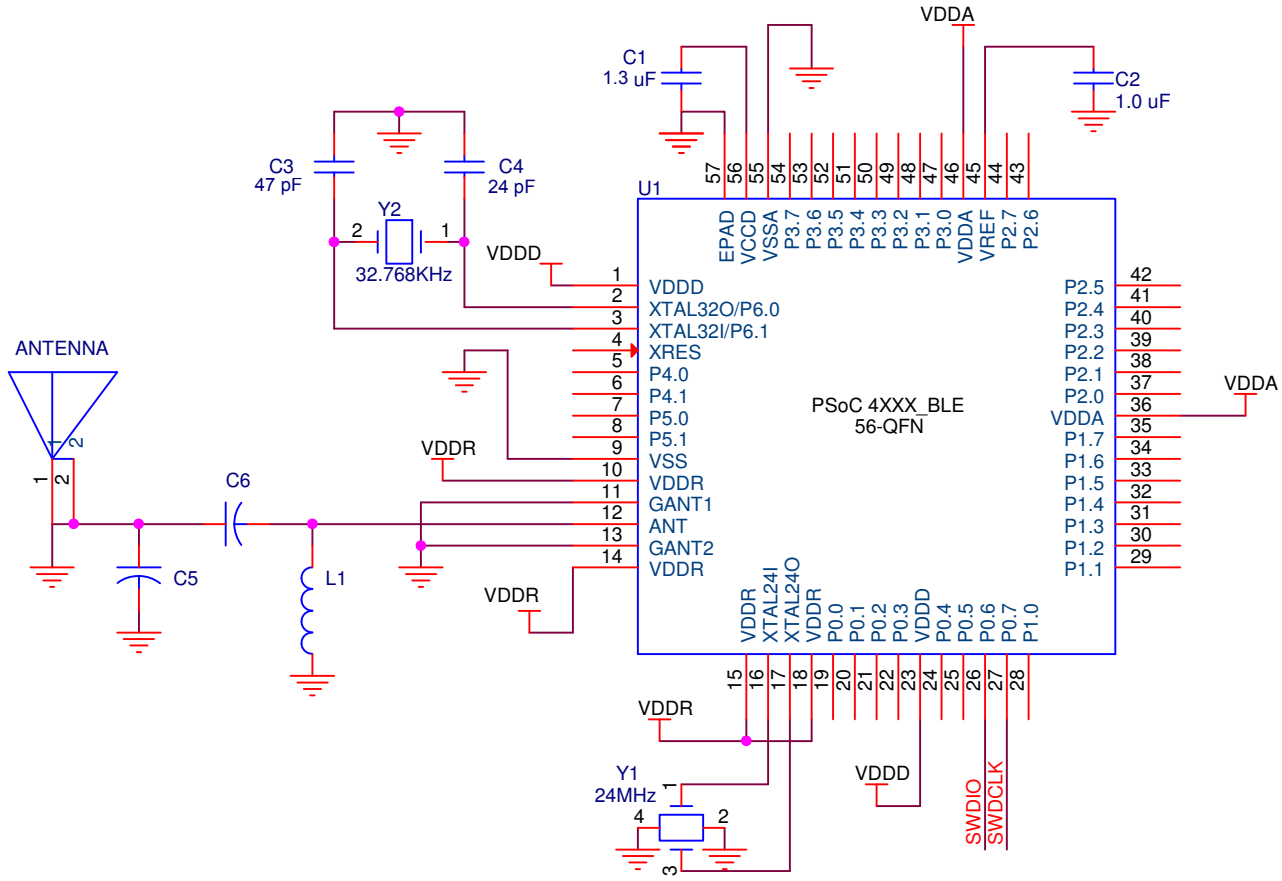
CapSense is supported on all pins in PSoC 4XX8 BLE 4.2 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A Component is provided for the CapSense block to make it easy for the user.

The shield voltage can be driven on another mux bus to provide liquid-tolerance capability. Liquid tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without liquid tolerance (one IDAC is available).

The possible pin connections are shown for all analog and digital peripherals (except the radio, LCD, and CSD blocks, which were shown in Table 1). A typical system application connection diagram is shown in Figure 7.

Figure 7. System Application Connection Diagram



Power

The PSoC 4XX8 BLE 4.2 device can be supplied from batteries with a voltage range of 1.9 V to 5.5 V by directly connecting to the digital supply (VDDD), analog supply (VDDA), and radio supply (VDDR) pins. Internal LDOs in the device regulate the supply voltage to the required levels for different blocks. The device has one regulator for the digital circuitry and separate regulators for radio circuitry for noise isolation. Analog circuits run directly from the analog supply (VDDA) input. The device uses separate regulators for Deep Sleep and Hibernate (lowered power supply and retention) modes to minimize the power consumption. The radio stops working below 1.9 V, but the device continues to function down to 1.71 V without RF.

Bypass capacitors must be used from VDDx (x = A, D, or R) to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range in parallel with a smaller capacitor (for example, 0.1 µF). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD	The internal bandgap may be bypassed with a 1-µF to 10-µF.
VDDA	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF.
VDDR	0.1-µF ceramic at each pin plus bulk capacitor 1-µF to 10-µF.
VCCD	1.3-µF ceramic capacitor at the VCCD pin.
VREF (optional)	The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor.

Development Support

The PSoC 4XX8 BLE 4.2 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4ble to find out more.

Documentation

A suite of documentation supports the PSoC 4XX8 BLE 4.2 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include creating standard and custom BLE profiles. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4XX8 BLE 4.2 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID19	I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID20	I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID21	I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID22	I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V_{DD} = 1.8 to 5.5 V							
SID23	I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 to 5.5 V							
SID24	I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V							
SID25	I_{DD15}	WDT with WCO on	–	1.5	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID26	I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V							
SID27	I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID28	I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID29	I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
SID30	I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V							
SID31	I_{DD21}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID32	I_{DD22}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V							
SID33	I_{DD23}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID34	I_{DD24}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID35	I_{DD25}	Opamp on	–	–	–	µA	T = 25 °C
SID36	I_{DD26}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.8 to 3.6 V							
SID37	I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3V
SID38	I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 3.6 to 5.5 V							
SID39	I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID40	I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID41	I_{DD31}	GPIO and reset active	–	–	–	nA	T = 25 °C
SID42	I_{DD32}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 to 3.6 V							
SID43	I_{DD33}	Stop mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
SID44	I_{DD34}	Stop mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
SID45	I_{DD35}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID46	I_{DD36}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 to 5.5 V							
SID47	I_{DD37}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID48	I_{DD38}	Stop mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
SID49	I_{DD39}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
SID50	I_{DD40}	Stop mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID51	I_{DD41}	Stop mode current (V_{DD})	–	–	–	nA	T = 25 °C
SID52	I_{DD42}	Stop mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C

Table 7. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
SID54	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
SID55	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization.
SID56	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID57	T_{STOP}	Wakeup from Stop mode	–	–	2.2	ms	Guaranteed by characterization

Digital Peripherals

Timer

Table 21. Timer DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID189	I_{TIM1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit timer
SID190	I_{TIM2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit timer
SID191	I_{TIM3}	Block current consumption at 48 MHz	–	–	712	µA	16-bit timer

Table 22. Timer AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID192	$T_{TIMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID193	$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID194	$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID195	T_{TIMRES}	Timer resolution	T_{CLK}	–	–	ns	–
SID196	$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID197	$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID198	$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID199	$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Counter

Table 23. Counter DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID200	I_{CTR1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit counter
SID201	I_{CTR2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit counter
SID202	I_{CTR3}	Block current consumption at 48 MHz	–	–	712	µA	16-bit counter

Table 24. Counter AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID203	$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	–
SID204	$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID205	$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID206	T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	–
SID207	$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID208	$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–
SID209	$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	–
SID210	$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	–

Pulse Width Modulation (PWM)

Table 25. PWM DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID211	I_{PWM1}	Block current consumption at 3 MHz	–	–	50	µA	16-bit PWM
SID212	I_{PWM2}	Block current consumption at 12 MHz	–	–	175	µA	16-bit PWM
SID213	I_{PWM3}	Block current consumption at 48 MHz	–	–	741	µA	16-bit PWM

Voltage Monitors

Table 43. Voltage Monitor DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID265	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
SID266	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
SID267	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
SID268	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
SID269	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
SID270	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
SID271	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
SID272	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
SID273	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
SID274	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
SID2705	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
SID276	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
SID277	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
SID278	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
SID279	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
SID280	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
SID281	LVI_IDD	Block current	–	–	100	µA	–

Table 44. Voltage Monitor AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID282	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	–

SWD Interface

Table 45. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID283	F_SWDCLK1	$3.3\ V \le V_{DD} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID284	F_SWDCLK2	$1.71\ V \le V_{DD} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID285	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID286	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID287	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
SID288	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 46. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID289	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–
SID290	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	–
SID291	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	–
SID292	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	–
SID293	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	–

Table 47. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID296	$F_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
SID297	$F_{IMOTOL3}$	IMO startup time	–	–	12	µs	–

Internal Low-Speed Oscillator

Table 48. ILO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID298	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

Table 49. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID299	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID300	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	–

Table 50. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID301	ExtClkFreq	External clock input frequency	0	–	48	MHz	CMOS input level only
SID302	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	CMOS input level only

Table 51. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path performance							
SID303	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID304	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID305	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
PLD Performance in UDB							
SID306	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
Clock to Output Performance							
SID307	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typical	–	15	–	ns	–
SID308	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case	–	25	–	ns	–

Table 52. BLE Subsystem *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID378	ITX,-6dBm	TX current at –6-dBm setting (PA3)	–	14.5	–	mA	–
SID379	ITX,-12dBm	TX current at –12-dBm setting (PA2)	–	13.2	–	mA	–
SID380	ITX,-18dBm	TX current at –18-dBm setting (PA1)	–	12.5	–	mA	–
SID380A	Iavg_1sec, 0dBm	Average current at 1-second BLE connection interval	–	17.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
SID380B	Iavg_4sec, 0dBm	Average current at 4-second BLE connection interval	–	6.1	–	µA	TXP: 0 dBm; ±20-ppm master and slave clock accuracy.
General RF Specifications							
SID381	FREQ	RF operating frequency	2400	–	2482	MHz	–
SID382	CHBW	Channel spacing	–	2	–	MHz	–
SID383	DR	On-air data rate	–	1000	–	kbps	–
SID384	IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	µs	–
SID385	IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	µs	–
RSSI Specifications							
SID386	RSSI, ACC	RSSI accuracy	–	±5	–	dB	–
SID387	RSSI, RES	RSSI resolution	–	1	–	dB	–
SID388	RSSI, PER	RSSI sample period	–	6	–	µs	–

Table 53. ECO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID389	F_{ECO}	Crystal frequency	–	24	–	MHz	–
SID390	F_{TOL}	Frequency tolerance	–50	–	50	ppm	–
SID391	ESR	Equivalent series resistance	–	–	60	Ω	–
SID392	PD	Drive level	–	–	100	µW	–
SID393	T_{START1}	Startup time (Fast Charge on)	–	–	850	µs	–
SID394	T_{START2}	Startup time (Fast Charge off)	–	–	3	ms	–
SID395	C_L	Load capacitance	–	8	–	pF	–
SID396	C0	Shunt capacitance	–	1.1	–	pF	–
SID397	I_{ECO}	Operating current	–	1400	–	µA	–

Packaging

Table 56. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25.00	105	°C
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA} (56-pin QFN)	–	–	16.9	–	°C/watt
T_{JC}	Package θ_{JC} (56-pin QFN)	–	–	9.7	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball WLCSP)	–	–	20.1	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball WLCSP)	–	–	0.19	–	°C/watt
T_{JA}	Package θ_{JA} (76-ball Thin WLCSP)	–	–	20.9	–	°C/watt
T_{JC}	Package θ_{JC} (76-ball Thin WLCSP)	–	–	0.17	–	°C/watt

Table 57. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
56-pin QFN	260 °C	30 seconds
76-ball WLCSP and Thin WLCSP	260 °C	30 seconds

Table 58. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
56-pin QFN	MSL 3
76-ball WLCSP and Thin WLCSP	MSL 1

Table 59. Package Details

Spec ID	Package	Description
001-58740 Rev. *C	56-pin QFN	7.0 mm × 7.0 mm × 0.6 mm
001-96603 Rev. *A	76-ball WLCSP	4.04 mm × 3.87 mm × 0.55 mm
002-10658, Rev. **	76-ball thin WLCSP	4.04 mm × 3.87 mm × 0.4 mm

Acronyms

Table 60. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 61. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 4: PSoC 4XX8 BLE 4.2 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 002-09848				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5009233	WKA	12/02/2015	Initial release
*A	5132452	WKA	02/10/2016	Updated typ value for SID13. Updated Conditions for SID141A, SID145, SID150, and SID154. Updated max values for Timer, Counter, and PWM specifications.
*B	5302481	MARW	06/09/2016	Updated GATT features and Security Manager features. Updated SAR ADC System diagram. Updated C3 and C4 values in Figure 5. Updated values for SID56, SID380A, and SID380B. Added 76-ball thin CSP package and ordering details.

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