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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Bluetooth, Brown-out Detect/Reset, Cap Sense, DMA LCD, LVD, POR, PWM, SmartCard, SmartSense, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-UFQFN Exposed Pad
Supplier Device Package	56-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4248lqi-bl583

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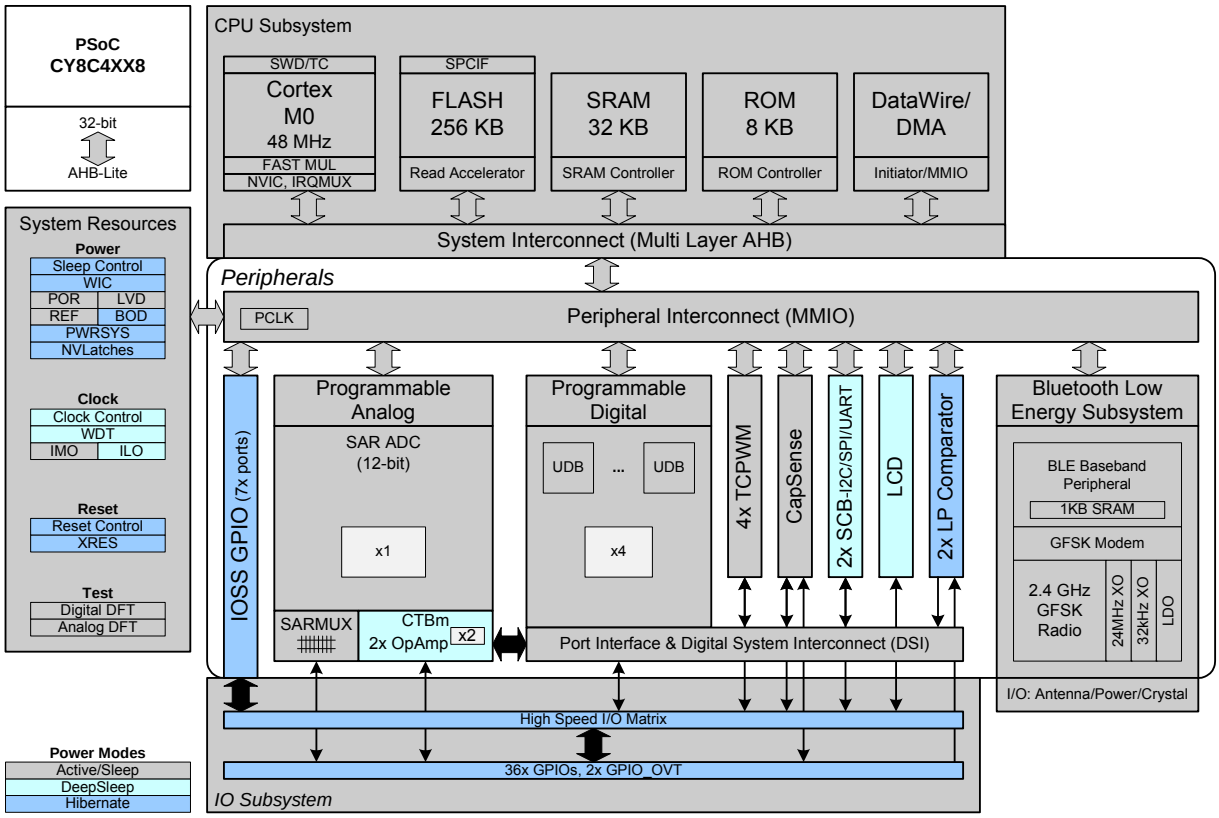
Figure 2. Block Diagram



The PSoC 4XX8 BLE 4.2 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM SWD interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debugging.

The PSoC Creator IDE provides fully integrated programming and debugging support for the PSoC 4XX8 BLE 4.2 devices. The SWD interface is fully compatible with industry-standard third-party tools. With the ability to disable debug features, very robust flash protection, and allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 4XX8 BLE 4.2 family provides a level of security not possible with multi-chip application solutions or with microcontrollers.

Debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with the new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4XX8 BLE 4.2 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4XX8 BLE 4.2 allows the customer to make.

Pinouts

Table 1 shows the pin list for the PSoC 4XX8 BLE 4.2 device. Port 3 consists of the high-speed analog inputs for the SAR mux. All pins support CSD CapSense and analog mux bus connections.

Table 1. PSoC 4XX8 BLE 4.2 Pin List (QFN Package)

Pin	Name	Type	Description
1	VDDD	POWER	1.71-V to 5.5-V digital supply
2	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
3	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
4	XRES	RESET	Reset, active LOW
5	P4.0	GPIO	Port 4 Pin 0, lcd, csd
6	P4.1	GPIO	Port 4 Pin 1, lcd, csd
7	P5.0	GPIO	Port 5 Pin 0, lcd, csd
8	P5.1	GPIO	Port 5 Pin 1, lcd, csd
9	VSSD	GROUND	Digital ground
10	VDDR	POWER	1.9-V to 5.5-V radio supply
11	GANT1	GROUND	Antenna shielding ground
12	ANT	ANTENNA	Antenna pin
13	GANT2	GROUND	Antenna shielding ground
14	VDDR	POWER	1.9-V to 5.5-V radio supply
15	VDDR	POWER	1.9-V to 5.5-V radio supply
16	XTAL24I	CLOCK	24-MHz crystal or external clock input
17	XTAL24O	CLOCK	24-MHz crystal
18	VDDR	POWER	1.9-V to 5.5-V radio supply
19	P0.0	GPIO	Port 0 Pin 0, lcd, csd
20	P0.1	GPIO	Port 0 Pin 1, lcd, csd
21	P0.2	GPIO	Port 0 Pin 2, lcd, csd
22	P0.3	GPIO	Port 0 Pin 3, lcd, csd
23	VDDD	POWER	1.71-V to 5.5-V digital supply
24	P0.4	GPIO	Port 0 Pin 4, lcd, csd
25	P0.5	GPIO	Port 0 Pin 5, lcd, csd
26	P0.6	GPIO	Port 0 Pin 6, lcd, csd
27	P0.7	GPIO	Port 0 Pin 7, lcd, csd
28	P1.0	GPIO	Port 1 Pin 0, lcd, csd
29	P1.1	GPIO	Port 1 Pin 1, lcd, csd
30	P1.2	GPIO	Port 1 Pin 2, lcd, csd
31	P1.3	GPIO	Port 1 Pin 3, lcd, csd
32	P1.4	GPIO	Port 1 Pin 4, lcd, csd
33	P1.5	GPIO	Port 1 Pin 5, lcd, csd
34	P1.6	GPIO	Port 1 Pin 6, lcd, csd
35	P1.7	GPIO	Port 1 Pin 7, lcd, csd
36	VDDA	POWER	1.71-V to 5.5-V analog supply
37	P2.0	GPIO	Port 2 Pin 0, lcd, csd
38	P2.1	GPIO	Port 2 Pin 1, lcd, csd
39	P2.2	GPIO	Port 2 Pin 2, lcd, csd

Table 1. PSoC 4XX8 BLE 4.2 Pin List (QFN Package) *(continued)*

Pin	Name	Type	Description
40	P2.3	GPIO	Port 2 Pin 3, lcd, csd
41	P2.4	GPIO	Port 2 Pin 4, lcd, csd
42	P2.5	GPIO	Port 2 Pin 5, lcd, csd
43	P2.6	GPIO	Port 2 Pin 6, lcd, csd
44	P2.7	GPIO	Port 2 Pin 7, lcd, csd
45	VREF	REF	1.024-V reference
46	VDDA	POWER	1.71-V to 5.5-V analog supply
47	P3.0	GPIO	Port 3 Pin 0, lcd, csd
48	P3.1	GPIO	Port 3 Pin 1, lcd, csd
49	P3.2	GPIO	Port 3 Pin 2, lcd, csd
50	P3.3	GPIO	Port 3 Pin 3, lcd, csd
51	P3.4	GPIO	Port 3 Pin 4, lcd, csd
52	P3.5	GPIO	Port 3 Pin 5, lcd, csd
53	P3.6	GPIO	Port 3 Pin 6, lcd, csd
54	P3.7	GPIO	Port 3 Pin 7, lcd, csd
55	VSSA	GROUND	Analog ground
56	VCCD	POWER	Regulated 1.8-V supply, connect to 1.3-µF capacitor.
57	EPAD	GROUND	Ground paddle for the QFN package

Table 2. PSoC 4XX8 BLE 4.2 Pin List (WLCSP Package)

Pin	Name	Type	Description
A1	NC	NC	Do not connect
A2	VREF	REF	1.024-V reference
A3	VSSA	GROUND	Analog ground
A4	P3.3	GPIO	Port 3 Pin 3, analog/digital/lcd/csd
A5	P3.7	GPIO	Port 3 Pin 7, analog/digital/lcd/csd
A6	VSSD	GROUND	Digital ground
A7	VSSA	GROUND	Analog ground
A8	VCCD	POWER	Regulated 1.8-V supply, connect to 1-µF capacitor
A9	VDDD	POWER	1.71-V to 5.5-V digital supply
B1	NB	NO BALL	No Ball
B2	P2.3	GPIO	Port 2 Pin 3, analog/digital/lcd/csd
B3	VSSA	GROUND	Analog ground
B4	P2.7	GPIO	Port 2 Pin 7, analog/digital/lcd/csd
B5	P3.4	GPIO	Port 3 Pin 4, analog/digital/lcd/csd
B6	P3.5	GPIO	Port 3 Pin 5, analog/digital/lcd/csd
B7	P3.6	GPIO	Port 3 Pin 6, analog/digital/lcd/csd
B8	XTAL32I/P6.1	CLOCK	32.768-kHz crystal or external clock input
B9	XTAL32O/P6.0	CLOCK	32.768-kHz crystal
C1	NC	NC	Do not connect

Table 2. PSoC 4XX8 BLE 4.2 Pin List (WLCSP Package) *(continued)*

Pin	Name	Type	Description
C2	VSSA	GROUND	Analog ground
C3	P2.2	GPIO	Port 2 Pin 2, analog/digital/lcd/csd
C4	P2.6	GPIO	Port 2 Pin 6, analog/digital/lcd/csd
C5	P3.0	GPIO	Port 3 Pin 0, analog/digital/lcd/csd
C6	P3.1	GPIO	Port 3 Pin 1, analog/digital/lcd/csd
C7	P3.2	GPIO	Port 3 Pin 2, analog/digital/lcd/csd
C8	XRES	RESET	Reset, active LOW
C9	P4.0	GPIO	Port 4 Pin 0, analog/digital/lcd/csd
D1	NC	NC	Do not connect
D2	P1.7	GPIO	Port 1 Pin 7, analog/digital/lcd/csd
D3	VDDA	POWER	1.71-V to 5.5-V analog supply
D4	P2.0	GPIO	Port 2 Pin 0, analog/digital/lcd/csd
D5	P2.1	GPIO	Port 2 Pin 1, analog/digital/lcd/csd
D6	P2.5	GPIO	Port 2 Pin 5, analog/digital/lcd/csd
D7	VSSD	GROUND	Digital ground
D8	P4.1	GPIO	Port 4 Pin 1, analog/digital/lcd/csd
D9	P5.0	GPIO	Port 5 Pin 0, analog/digital/lcd/csd
E1	NC	NC	Do not connect
E2	P1.2	GPIO	Port 1 Pin 2, analog/digital/lcd/csd
E3	P1.3	GPIO	Port 1 Pin 3, analog/digital/lcd/csd
E4	P1.4	GPIO	Port 1 Pin 4, analog/digital/lcd/csd
E5	P1.5	GPIO	Port 1 Pin 5, analog/digital/lcd/csd
E6	P1.6	GPIO	Port 1 Pin 6, analog/digital/lcd/csd
E7	P2.4	GPIO	Port 2 Pin 4, analog/digital/lcd/csd
E8	P5.1	GPIO	Port 5 Pin 1, analog/digital/lcd/csd
E9	VSSD	GROUND	Digital ground
F1	NC	NC	Do not connect
F2	VSSD	GROUND	Digital ground
F3	P0.7	GPIO	Port 0 Pin 7, analog/digital/lcd/csd
F4	P0.3	GPIO	Port 0 Pin 3, analog/digital/lcd/csd
F5	P1.0	GPIO	Port 1 Pin 0, analog/digital/lcd/csd
F6	P1.1	GPIO	Port 1 Pin 1, analog/digital/lcd/csd
F7	VSSR	GROUND	Radio ground
F8	VSSR	GROUND	Radio ground
F9	VDDR	POWER	1.9-V to 5.5-V radio supply
G1	NC	NC	Do not connect
G2	P0.6	GPIO	Port 0 Pin 6, analog/digital/lcd/csd
G3	VDDD	POWER	1.71-V to 5.5-V digital supply
G4	P0.2	GPIO	Port 0 Pin 2, analog/digital/lcd/csd
G5	VSSD	GROUND	Digital ground

Development Support

The PSoC 4XX8 BLE 4.2 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4ble to find out more.

Documentation

A suite of documentation supports the PSoC 4XX8 BLE 4.2 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include creating standard and custom BLE profiles. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4XX8 BLE 4.2 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Analog, digital, or radio supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	6	V	Absolute max
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute max
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} +0.5	V	Absolute max
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
BID57	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID58	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
BID61	LU	Pin current for latch-up	–200	–	200	mA	–

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 6. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID6	V_{DD}	Power supply input voltage (V_{DDA} = V_{DDD} = V_{DD})	1.8	–	5.5	V	With regulator enabled
SID7	V_{DD}	Power supply input voltage unregulated (V_{DDA} = V_{DDD} = V_{DD})	1.71	1.8	1.89	V	Internally unregulated Supply
SID8	V_{DDR}	Radio supply voltage (Radio ON)	1.9	–	5.5	V	–
SID8A	V_{DDR}	Radio supply voltage (Radio OFF)	1.71	–	5.5	V	–
SID9	V_{CCD}	Digital regulator output voltage (for core logic)	–	1.8	–	V	–
SID10	C_{VCCD}	Digital regulator output bypass capacitor	1	1.3	1.6	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V							–
SID13	I_{DD3}	Execute from flash; CPU at 3 MHz	–	2.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID14	I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = –40 C to 85 °C
SID15	I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID16	I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID17	I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID18	I_{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C

Note
1. Usage above the absolute maximum conditions listed in Table 5 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 6. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID19	I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID20	I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
SID21	I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
SID22	I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V_{DD} = 1.8 to 5.5 V							
SID23	I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 to 5.5 V							
SID24	I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, VDD = 3.3 V, SYSCLK = 3 MHz
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V							
SID25	I_{DD15}	WDT with WCO on	–	1.5	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID26	I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V							
SID27	I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID28	I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID29	I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
SID30	I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.8 to 3.6 V							
SID31	I_{DD21}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 3.3 V
SID32	I_{DD22}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 3.6 to 5.5 V							
SID33	I_{DD23}	Opamp on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
SID34	I_{DD24}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Deep Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							
SID35	I_{DD25}	Opamp on	–	–	–	µA	T = 25 °C
SID36	I_{DD26}	Opamp on	–	–	–	µA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.8 to 3.6 V							
SID37	I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3V
SID38	I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 3.6 to 5.5 V							
SID39	I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
SID40	I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)							

GPIO

Table 8. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID58	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
SID59	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
SID60	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	-	V	–
SID61	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3× V_{DD}	V	–
SID62	V_{IH}	LVTTL input, V_{DD} >= 2.7 V	2.0	–	-	V	–
SID63	V_{IL}	LVTTL input, V_{DD} >= 2.7 V	–	–	0.8	V	–
SID64	V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	Ioh = 4-mA at 3.3-V V_{DD}
SID65	V_{OH}	Output voltage HIGH level	V_{DD} –0.5	–	–	V	Ioh = 1-mA at 1.8-V V_{DD}
SID66	V_{OL}	Output voltage LOW level	–	–	0.6	V	Iol = 8-mA at 3.3-V V_{DD}
SID67	V_{OL}	Output voltage LOW level	–	–	0.6	V	Iol = 4-mA at 1.8-V V_{DD}
SID68	V_{OL}	Output voltage LOW level	–	–	0.4	V	Iol = 3-mA at 3.3-V V_{DD}
SID69	Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID70	Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID71	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
SID72	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID73	C_{IN}	Input capacitance	–	–	7	pF	–
SID74	Vhysttl	Input hysteresis LVTTL	25	40		mV	V_{DD} > 2.7 V
SID75	Vhyscmos	Input hysteresis CMOS	0.05 × V_{DD}	–	–	mV	–
SID76	Idiode	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID77	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 9. GPIO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID78	T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID79	T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID80	T_{RISES}	Rise time in Slow-Strong mode	10	–	60	–	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID81	T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	–	3.3-V V_{DDD}, C_{LOAD} = 25-pF
SID82	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Fast-Strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 15. Comparator DC Specifications[3] *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID150	I_{CMP3}	Block current in ultra low-power mode	–	6	–	µA	V_{DDD} ≥ 2.6 V for Temp < 0°C, V_{DDD} ≥ 1.8 V for Temp > 0 °C
SID151	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	–

Table 16. Comparator AC Specifications[4]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID152	T_{RESP1}	Response time, normal mode, 50-mV overdrive	–	38	–	ns	50-mV overdrive
SID153	T_{RESP2}	Response time, low power mode, 50-mV overdrive	–	70	–	ns	50-mV overdrive
SID154	T_{RESP3}	Response time, ultra-low-power mode, 50-mV overdrive	–	2.3	–	µs	200-mV overdrive. V_{DDD} ≥ 2.6 V for Temp < 0°C, V_{DDD} ≥ 1.8 V for Temp > 0 °C

Temperature Sensor

Table 17. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID155	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

SAR ADC

Table 18. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID156	A_RES	Resolution	–	–	12	bits	–
SID157	A_CHNIS_S	Number of channels - single-ended	–	–	8	–	8 full-speed
SID158	A-CHNKS_D	Number of channels - differential	–	–	4	–	Diff inputs use neighboring I/O
SID159	A-MONO	Monotonicity	–	–	–	–	Yes
SID160	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID161	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
SID162	A_ISAR	Current consumption	–	–	1	mA	–
SID163	A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	–
SID164	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	–
SID165	A_INRES	Input resistance	–	–	2.2	kΩ	–
SID166	A_INCAP	Input capacitance	–	–	10	pF	–
SID312	VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024-V)

Note
4. ULP LCOMP operating conditions:
   - V_{DDD} 2.6 V-5.5 V for datasheet temp range < 0 °C
   - V_{DDD} 1.8 V-5.5 V for datasheet temp range ≥ 0 °C

Table 47. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID296	$F_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
SID297	$F_{IMOTOL3}$	IMO startup time	–	–	12	µs	–

Internal Low-Speed Oscillator

Table 48. ILO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID298	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

Table 49. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID299	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID300	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	–

Table 50. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID301	ExtClkFreq	External clock input frequency	0	–	48	MHz	CMOS input level only
SID302	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	CMOS input level only

Table 51. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path performance							
SID303	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID304	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID305	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
PLD Performance in UDB							
SID306	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
Clock to Output Performance							
SID307	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typical	–	15	–	ns	–
SID308	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case	–	25	–	ns	–

Ordering Information

The PSoC 4XX8 BLE 4.2 part numbers and features are listed in Table 55.

Table 55. PSoC 4XXX8_BLE Part Numbers

Family	MPN	Features																Package
		Max CPU Speed (MHz)	BLE sub-system	Flash (KB)	SRAM (KB)	UDB	Op-amp	CapSense	TMG (Gestures)	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	PWMs (using UDBs)	I2S (using UDB)	GPIO	
PSoC 4 BLE256K: CY8C41XX	CY8C4128LQI-BL543	24	√	256	32	-	2	-	-	-	806 Ksps	-	4	2	NA		36	QFN
	CY8C4128FNI-BL543	24	√	256	32	-	2	-	-	-	806 Ksps	-	4	2			36	CSP
	CY8C4128LQI-BL573	24	√	256	32	-	2	-	-	-	806 Ksps	2	4	2			36	QFN
	CY8C4128FNI-BL573	24	√	256	32	-	2	-	-	-	806 Ksps	2	4	2			36	CSP
	CY8C4128LQI-BL553	24	√	256	32	-	2	√	-	-	806 Ksps	2	4	2			36	QFN
	CY8C4128FNI-BL553	24	√	256	32	-	2	√	-	-	806 Ksps	2	4	2			36	CSP
	CY8C4128LQI-BL563	24	√	256	32	-	2	-	-	√	806 Ksps	2	4	2			36	QFN
	CY8C4128FNI-BL563	24	√	256	32	-	2	-	-	√	806 Ksps	2	4	2			36	CSP
	CY8C4128LQI-BL583	24	√	256	32	-	2	√	-	√	806 Ksps	2	4	2			36	QFN
	CY8C4128FNI-BL583	24	√	256	32	-	2	√	-	√	806 Ksps	2	4	2			36	CSP
	CY8C4128LQI-BL593	24	√	256	32	-	2	√	√	√	806 Ksps	2	4	2			36	QFN
	CY8C4128FNI-BL593	24	√	256	32	-	2	√	√	√	806 Ksps	2	4	2			36	CSP
PSoC 4 BLE256K: CY8C42xx	CY8C4248LQI-BL543	48	√	256	32	-	2	-	-	-	1 Msps	-	4	2	-	-	36	QFN
	CY8C4248FNI-BL543	48	√	256	32	-	2	-	-	-	1 Msps	-	4	2	-	-	36	CSP
	CY8C4248LQI-BL573	48	√	256	32	4	4	-	-	-	1 Msps	2	4	2	4	√	36	QFN
	CY8C4248FNI-BL573	48	√	256	32	4	4	-	-	-	1 Msps	2	4	2	4	√	36	CSP
	CY8C4248LQI-BL553	48	√	256	32	4	4	√	-	-	1 Msps	2	4	2	4	√	36	QFN
	CY8C4248FNI-BL553	48	√	256	32	4	4	√	-	-	1 Msps	2	4	2	4	√	36	CSP
	CY8C4248LQI-BL563	48	√	256	32	4	4	-	-	√	1 Msps	2	4	2	4	√	36	QFN
	CY8C4248FNI-BL563	48	√	256	32	4	4	-	-	√	1 Msps	2	4	2	4	√	36	CSP
	CY8C4248LQI-BL583	48	√	256	32	4	4	√	-	√	1 Msps	2	4	2	4	√	36	QFN
	CY8C4248FNI-BL583	48	√	256	32	4	4	√	-	√	1 Msps	2	4	2	4	√	36	CSP
	CY8C4248FLI-BL583	48	√	256	32	4	4	√	-	√	1 Msps	2	4	2	4	√	36	Thin CSP
	CY8C4248LQQ-BL583	48	√	256	32	4	4	√	-	√	1 Msps	2	4	2	4	√	36	QFN
	CY8C4248FNQ-BL583	48	√	256	32	4	4	√	-	√	1 Msps	2	4	2	4	√	36	CSP
	CY8C4248LQI-BL593	48	√	256	32	4	4	√	√	√	1 Msps	2	4	2	4	√	36	QFN
	CY8C4248FNI-BL593	48	√	256	32	4	4	√	√	√	1 Msps	2	4	2	4	√	36	CSP

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, …, 9, A,B, …, Z) unless stated otherwise.

Ordering Code Definitions

Example

CY8 C

4 : PSoC 4

2 : 4200 Family

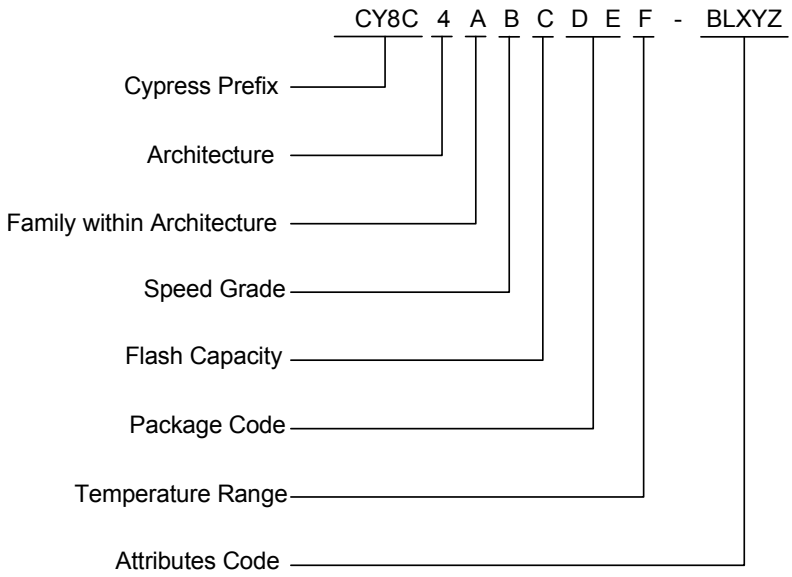
4 : 48 MHz

8 : 256 KB

LQ : QFN

I : Industrial

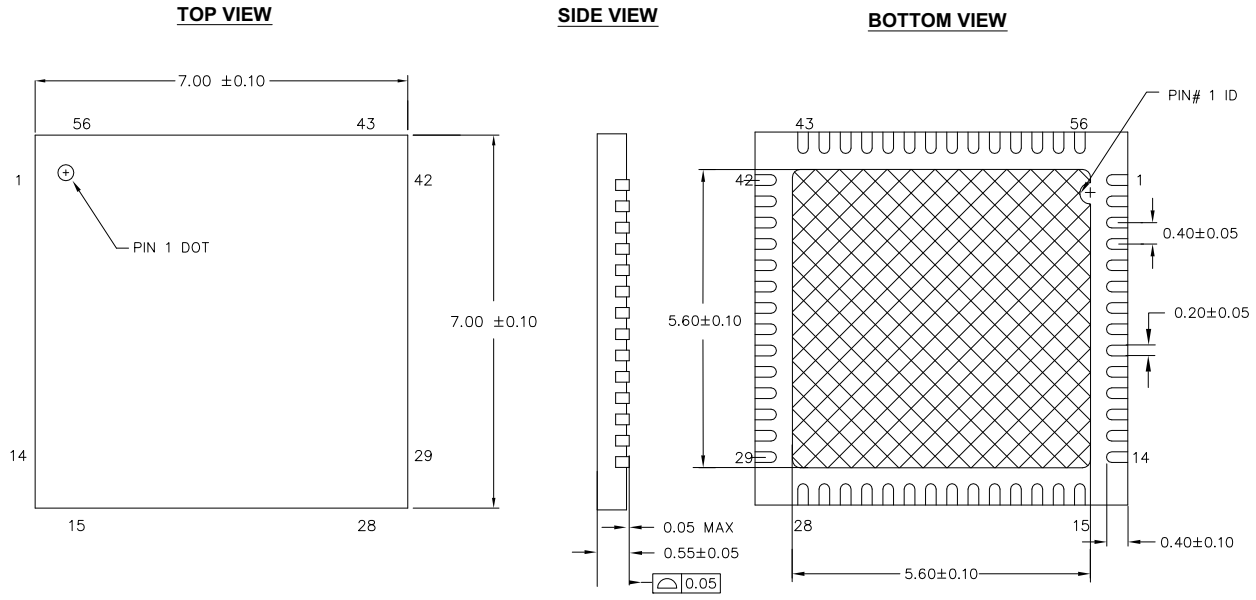
BLXYZ: Attributes



The Field Values are listed in the following table:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family within architecture	1	4100-BLE Family
		2	4200-BLE Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	8, 7	256, 128 KB
DE	Package Code	FN	WLCSP
		LQ	QFN
		FL	Thin CSP
F	Temperature Range	I	Industrial
BLXYZ	Attributes Code	BL500-BL599	BL5 indicates Bluetooth LE 4.2 support

Figure 8. 56-Pin QFN 7 × 7 × 0.6 mm



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-58740 *C

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance.

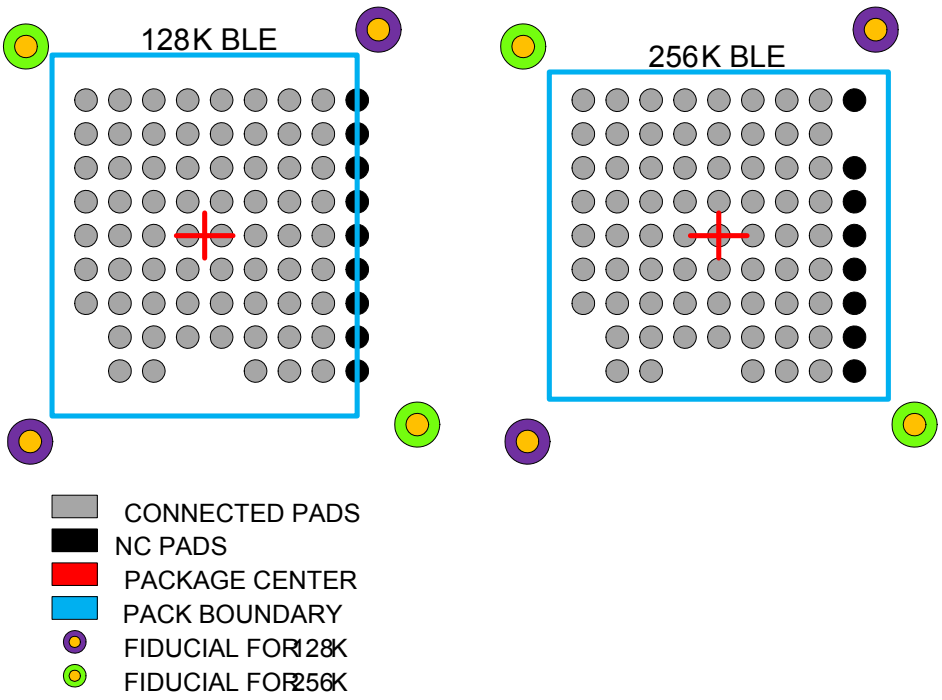
WLCSP Compatibility

The PSoC 4XXX_BLE family has products with 128 KB (16KB SRAM) and 256 KB (32KB SRAM) Flash. Package pin-outs and sizes are identical for the 56-pin QFN package but are different in one dimension for the 68-ball WLCSP.

The 256KB Flash product has an extra column of balls which are required for mechanical integrity purposes in the Chip-Scale package. With consideration for this difference, the land pattern on the PCB may be designed such that either product may be used with no change to the PCB design.

Figure 9 shows the 128KB and 256 KB Flash CSP packages.

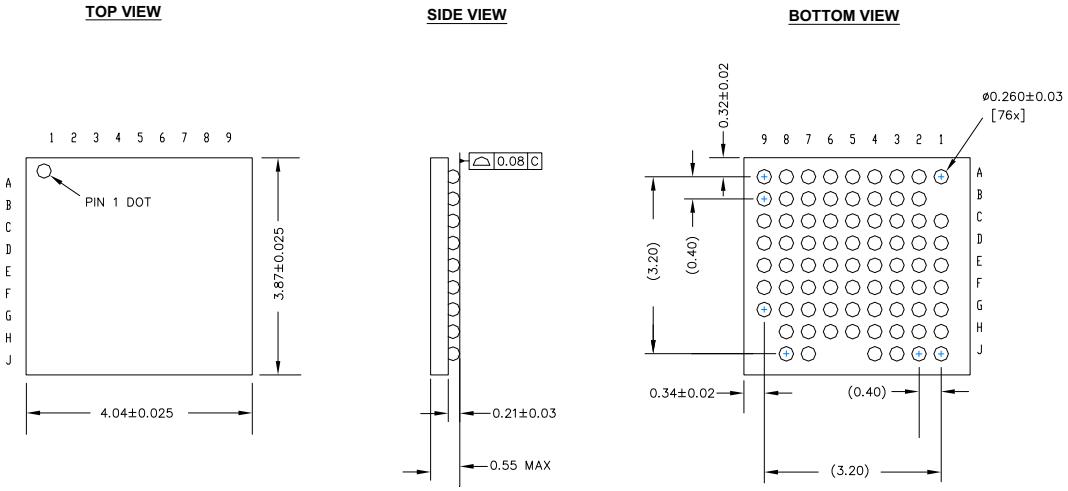
Figure 9. 128KB and 256 KB Flash CSP Packages



The rightmost column of (all NC, No Connect) balls in the 256K BLE WLCSP is for mechanical integrity purposes. The package is thus wider (3.2 mm versus 2.8 mm). All other dimensions are identical. Cypress will provide layout symbols for PCB layout.

The scheme in Figure 9 is implemented to design the PCB for the 256K BLE package with the appropriate space requirements thus allowing use of either package at a later time without redesigning the Printed Circuit Board.

Figure 10. 76-Ball WLCSP Package Outline



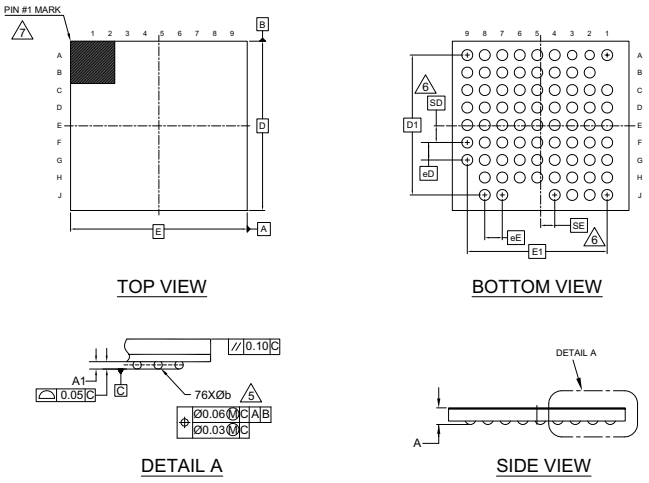
NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18

2. ALL DIMENSIONS ARE IN MILLIMETERS

001-96603 *A

Figure 11. 76-Ball Thin WLCSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.40
A1	0.072	0.08	0.088
D	3.87 BSC		
E	4.04 BSC		
D1	3.20 BSC		
E1	3.20 BSC		
MD	9		
ME	9		
N	76		
Ø b	0.22	0.25	0.28
eD	0.40 BSC		
eE	0.40 BSC		
SD	0.381		
SE	0.321		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-10658 **

Acronyms

Table 60. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 60. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Revision History

Description Title: PSoC® 4: PSoC 4XX8 BLE 4.2 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 002-09848				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5009233	WKA	12/02/2015	Initial release
*A	5132452	WKA	02/10/2016	Updated typ value for SID13. Updated Conditions for SID141A, SID145, SID150, and SID154. Updated max values for Timer, Counter, and PWM specifications.
*B	5302481	MARW	06/09/2016	Updated GATT features and Security Manager features. Updated SAR ADC System diagram. Updated C3 and C4 values in Figure 5. Updated values for SID56, SID380A, and SID380B. Added 76-ball thin CSP package and ordering details.

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