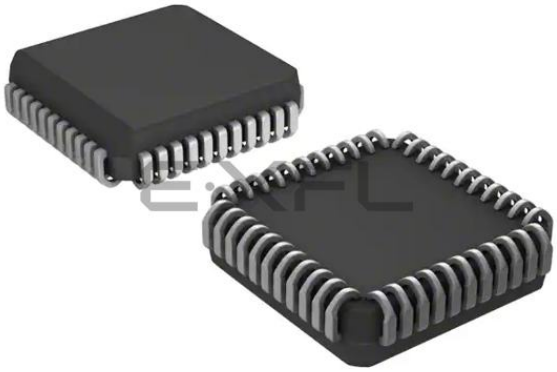

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Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	192 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v52x2fa-512

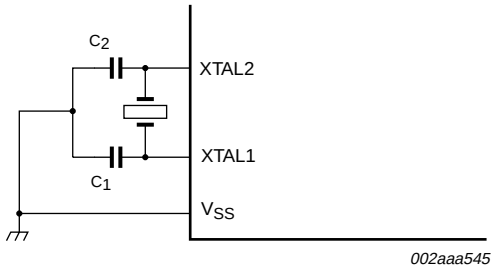


Fig 5. Oscillator characteristics (using the on-chip oscillator)

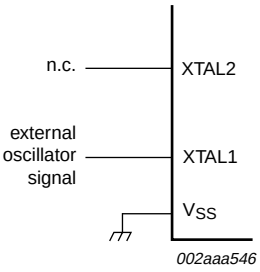


Fig 6. Oscillator characteristics (external clock drive)

6.3.2 Clock control register (CKCON)

By default, the device runs at twelve clocks per machine cycle. The device may be run in 6 clock per machine cycle mode by programming of either a non-volatile bit (FX2) or an SFR bit (Table 5 “Clock modes”). If the FX2 non-volatile bit is programmed the device will run in 6-clock mode and the X2 SFR bit has no effect. If the FX2 bit is erased, then the clock mode is controlled by the X2 SFR bit.

Table 5. Clock modes

FX2 clock mode bit (UCFG.1)	X2 bit (CLKCON.0)	CPU clock mode
erased	0	12-clock mode (default)
erased	1	6-clock mode
programmed	x	6-clock mode

6.4 ALE control

Table 6. AUXR - Auxiliary register (address 8EH) bit allocation

Not bit addressable; Reset value 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	AO

Table 7. AUXR - Auxiliary register (address 8EH) bit description

Bit	Symbol	Description
7 to 1	-	Reserved for future use. Should be set to '0' by user programs.
0	AO	ALE off: disables/enables ALE. AO = 0 results in ALE emitted at a constant rate of ½ the oscillator frequency. In case of AO = 1, ALE is active only during a MOVX or MOVC.

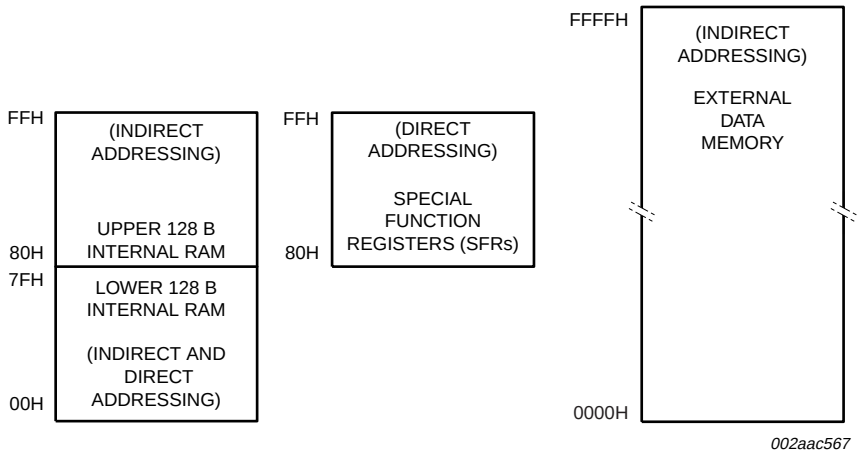


Fig 7. Internal and external data memory structure

6.5 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1 (see Figure 8).

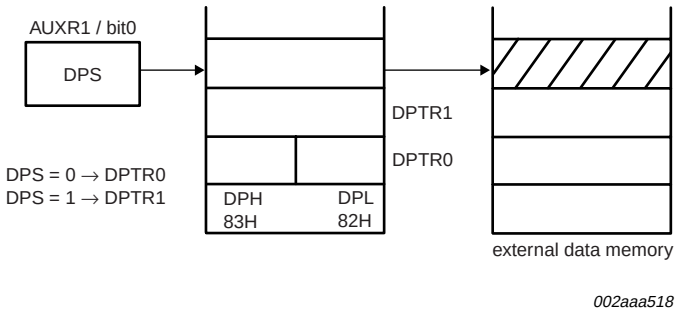


Fig 8. Dual data pointer organization

Table 8. AUXR1 - Auxiliary register 1 (address A2H) bit allocation

Not bit addressable; Reset value 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	GF2	0	-	DPS

6.7 Flash memory

6.7.1 Flash organization

The P89V52X2 program memory consists of an 8 kB block of user code. The flash can be read or written in bytes but may only be erased as an entire block. A chip erase function will erase the entire user code memory and its associated security bits. This flash memory can be erased or programmed using a programmer tool that supports ICP.

6.7.2 Features

- Flash internal program memory.
- Programming and erase over the full operating voltage range.
- Programming with industry-standard commercial programmers.
- 10000 typical erase/program cycles for each byte.
- 100 year minimum data retention.

6.8 Timers/counters 0 and 1

The two 16-bit Timer/Counter registers: Timer 0 and Timer 1 can be configured to operate either as timers or event counters (see Table 10 and Table 11).

In the ‘Timer’ function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of six oscillator periods, the count rate is $\frac{1}{6}$ of the oscillator frequency.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once every machine cycle.

When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register in the machine cycle following the one in which the transition was detected. Since it takes two machine cycles (12 oscillator periods) for 1-to-0 transition to be recognized, the maximum count rate is $\frac{1}{12}$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle. In addition to the ‘Timer’ or ‘Counter’ selection, Timer 0 and Timer 1 have four operating modes from which to select.

The ‘Timer’ or ‘Counter’ function is selected by control bits C/T in the Special Function Register TMOD. These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Table 10. TMOD - Timer/Counter mode control register (address 89H) bit allocation

Not bit addressable; Reset value: 0000 0000B; Reset source(s): any source

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

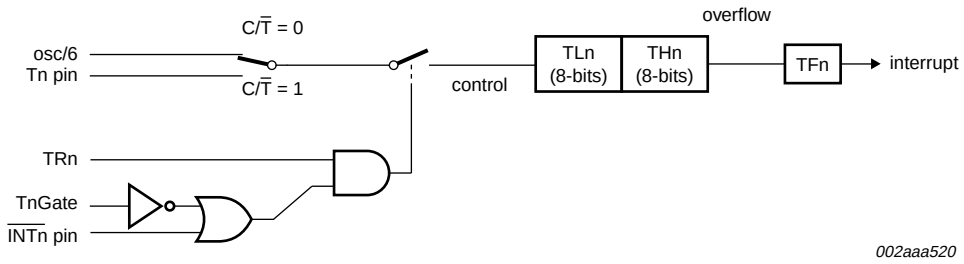


Fig 11. Timer/Counter 0 or 1 in Mode 1 (16-bit counter)

6.8.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 12. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

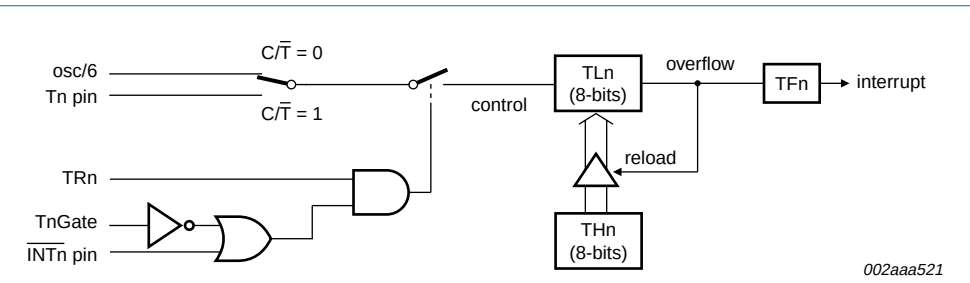


Fig 12. Timer/Counter 0 or 1 in Mode 2 (8-bit auto-reload)

6.8.4 Mode 3

When timer 1 is in Mode 3 it is stopped (holds its count). The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 and Timer 0 is shown in Figure 13. TL0 uses the Timer 0 control bits: T0C/$\overline{T}$, T0GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the 'Timer 1' interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in Mode 3, the P89V52X2 can look like it has an additional Timer.

Note: When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

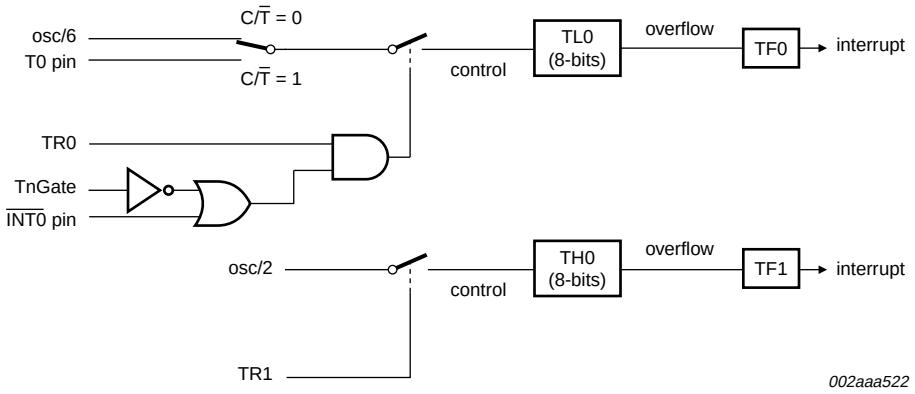


Fig 13. Timer/Counter 0 Mode 3 (two 8-bit counters)

6.9 Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2 in the special function register T2CON. Timer 2 has four operating modes: Capture, Auto-reload (up or down counting), Clock-out, and Baud Rate Generator which are selected according to Table 15 using T2CON (Table 16 and Table 17) and T2MOD (Table 18 and Table 19).

Table 15. Timer 2 operating mode

RCLK+TCLK	CP/$\overline{RL2}$	TR2	T2OE	Mode
0	0	1	0	16-bit auto reload
0	1	1	0	16-bit capture
0	0	1	1	Programmable Clock-Out
1	X	1	0	Baud rate generator
X	X	0	X	off

Table 16. T2CON - Timer/Counter 2 control register (address C8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 17. T2CON - Timer/Counter 2 control register (address C8H) bit description

Bit	Symbol	Description
7	TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1 or when Timer 2 is in Clock-out mode.
6	EXF2	Timer 2 external flag is set when Timer 2 is in capture, reload or baud rate mode, EXEN2 = 1 and a negative transition on T2EX occurs. If Timer 2 interrupt is enabled EXF2 = 1 causes the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
5	RCLK	Receive clock flag. When set, causes the UART to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

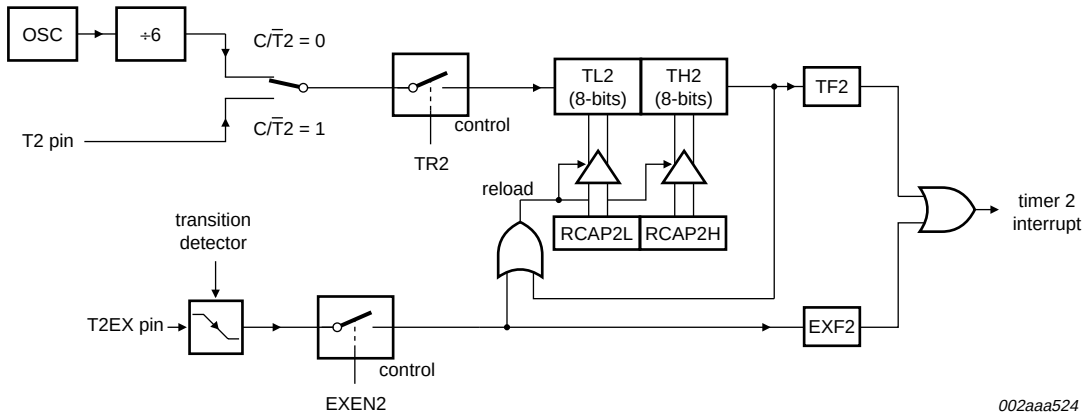


Fig 15. Timer 2 in auto-reload mode (DCEN = 0)

In this mode, there are two options selected by bit EXEN2 in T2CON register. If EXEN2 = 0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

Auto reload frequency when Timer 2 is counting up can be determined from this formula:

$$\frac{SupplyFrequency}{(65536 \angle (RCAP2H, RCAP2L))} \quad (1)$$

Where SupplyFrequency is either f_{osc} (C/$\overline{T2}$ = 0) or frequency of signal on T2 pin (C/$\overline{T2}$ = 1).

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 is ‘1’.

Microcontroller’s hardware will need three consecutive machine cycles in order to recognize falling edge on T2EX and set EXF2 = 1: in the first machine cycle pin T2EX has to be sampled as ‘1’; in the second machine cycle it has to be sampled as ‘0’, and in the third machine cycle EXF2 will be set to ‘1’.

In Figure 16, DCEN = 1 and Timer 2 is enabled to count up or down. This mode allows pin T2EX to control the direction of count. When a logic ‘1’ is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

6.10.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer ½ overflow rate.

6.10.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or (e.g. the parity bit (P, in the PSW) could be moved into TB8). When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

6.10.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer ½ overflow rate.

Table 21. SCON - Serial port control register (address 98H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Table 22. SCON - Serial port control register (address 98H) bit description

Bit	Symbol	Description
7	SM0/FE	The usage of this bit is determined by SMOD0 in the PCON register. If SMOD0 = 0, this bit is SM0, which with SM1, defines the serial port mode. If SMOD0 = 1, this bit is FE (Framing Error). FE is set by the receiver when an invalid stop bit is detected. Once set, this bit cannot be cleared by valid frames but can only be cleared by software. (Note: It is recommended to set up UART mode bits SM0 and SM1 before setting SMOD0 to '1'.)
6	SM1	With SM0, defines the serial port mode (see Table 23 below).
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to '1', then RI will not be activated if the received 9th data bit (RB8) is '0'. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be '0'.
4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.

Table 22. SCON - Serial port control register (address 98H) bit description *...continued*

Bit	Symbol	Description
2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is undefined.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or approximately halfway through the stop bit time in all other modes. (See SM2 for exceptions). Must be cleared by software.

Table 23. SCON - Serial port control register (address 98H) SM0/SM1 mode definition

SM0, SM1	UART mode	Baud rate
0 0	0: shift register	CPU clock/6
0 1	1: 8-bit UART	variable
1 0	2: 9-bit UART	CPU clock/32 or CPU clock/16
1 1	3: 9-bit UART	variable

6.10.5 Framing error

Framing error (FE) is reported in the SCON.7 bit if SMOD0 (PCON.6) = 1. If SMOD0 = 0, SCON.7 is the SM0 bit for the UART, it is recommended that SM0 is set up before SMOD0 is set to '1'.

6.10.6 More about UART mode 1

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset to align its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated.

6.10.7 More about UART modes 2 and 3

Reception is performed in the same manner as in mode 1.

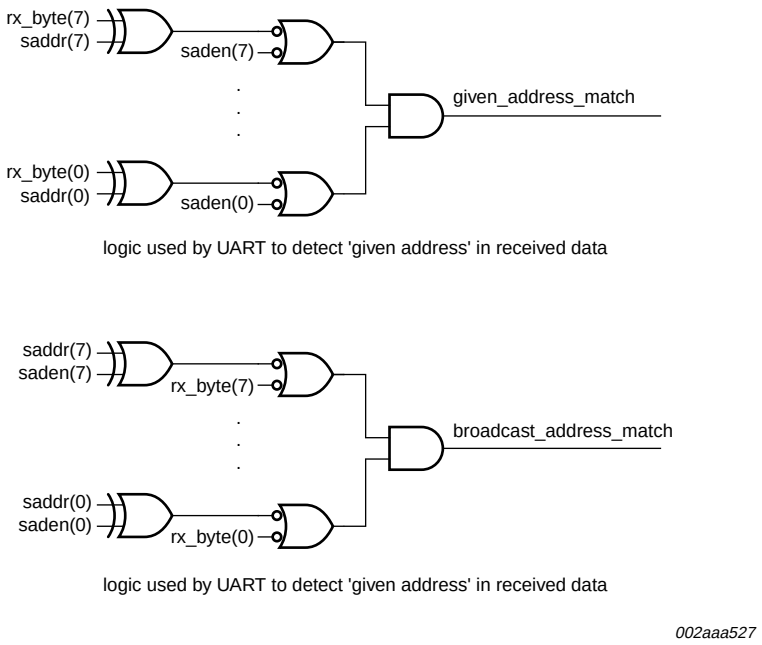


Fig 18. Schemes used by the UART to detect ‘given’ and ‘broadcast’ addresses when multiprocessor communications is enabled

The following examples will help to show the versatility of this scheme.

Example 1, slave 0:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1101} \\ \text{Given} = 1100\ 00\text{X}0 \end{array} \quad (4)$$

Example 2, slave 1:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1110} \\ \text{Given} = 1100\ 000\text{X} \end{array} \quad (5)$$

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a ‘0’ in bit 0 and it ignores bit 1. Slave 1 requires a ‘0’ in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a ‘0’ in bit 1. A unique address for slave 1 would be 1100 0001 since a ‘1’ in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Example 1, slave 0:

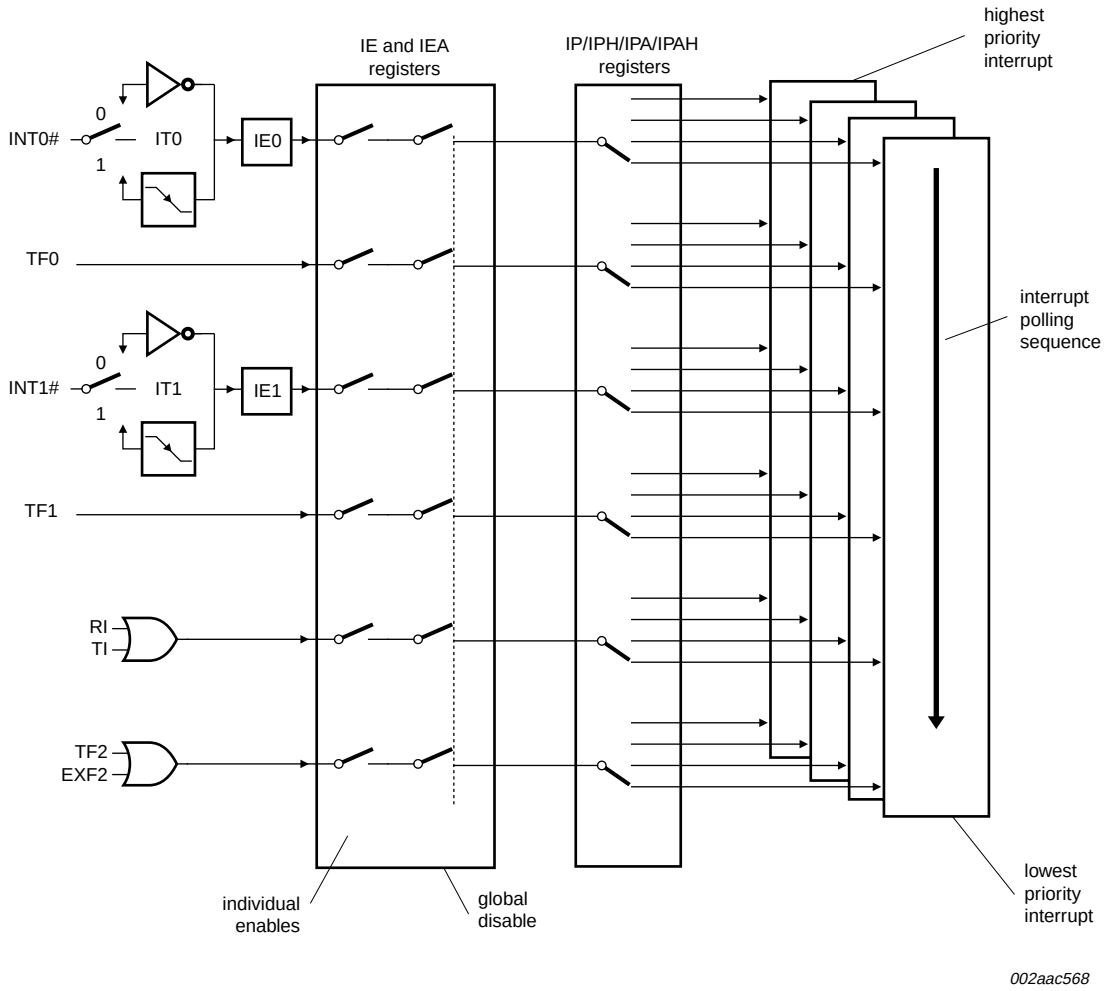


Fig 19. Interrupt structure

Table 25. IE - Interrupt enable register (address A8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Table 26. IE - Interrupt enable register (address A8H) bit description

Bit	Symbol	Description
7	EA	Interrupt Enable Bit: EA = 1 interrupt(s) can be serviced, EA = 0 interrupt servicing disabled.
6	-	Reserved
5	ET2	Timer 2 Overflow Interrupt Enable
4	ES	Serial Port Interrupt Enable
3	ET1	Timer 1 Overflow Interrupt Enable.

Table 26. IE - Interrupt enable register (address A8H) bit description *...continued*

Bit	Symbol	Description
2	EX1	External Interrupt 1 Enable.
1	ET0	Timer 0 Overflow Interrupt Enable.
0	EX0	External Interrupt 0 Enable.

Table 27. IP - Interrupt priority low register (address B8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	PT2	PS	PT1	PX1	PT0	PX0

Table 28. IP - Interrupt priority low register (address B8H) bit description

Bit	Symbol	Description
7:6	-	Reserved
5	PT2	Timer 2 Interrupt Priority Low Bit.
4	PS	Serial Port Interrupt Priority Low Bit.
3	PT1	Timer 1 Interrupt Priority Low Bit.
2	PX1	External Interrupt 1 Priority Low Bit.
1	PT0	Timer 0 Interrupt Priority Low Bit.
0	PX0	External Interrupt 0 Priority Low Bit.

Table 29. IPH - Interrupt priority high register (address B7H) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 30. IPH - Interrupt priority high register (address B7H) bit description

Bit	Symbol	Description
7:6	-	Reserved
5	PT2H	Timer 2 Interrupt Priority High Bit.
4	PSH	Serial Port Interrupt Priority High Bit.
3	PT1H	Timer 1 Interrupt Priority High Bit.
2	PX1H	External Interrupt 1 Priority High Bit.
1	PT0H	Timer 0 Interrupt Priority High Bit.
0	PX0H	External Interrupt 0 Priority High Bit.

6.12 Power-saving modes

The device provides two power saving modes of operation for applications where power consumption is critical. The two modes are idle and Power-down, see Table 31.

6.12.1 Idle mode

Idle mode is entered setting the IDL bit in the PCON register. In Idle mode, the program counter is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

Table 34. Flash Memory Control register (FMCON - address E4H) bit description

Bit	Symbol	Access	Description
0	ERR	R	Set when either of the following conditions occur: • Device was reset before the operation was completed. • Attempt made to access data EEPROM while Data Access Protect (DAP) is set. • An error occurs in the device's internal high voltage circuits.
	FMCMD.0	W	Command byte bit 0.
1	SV	R	Security violation. Set when an attempt is made to program, erase, or CRC a secured page. The specific cause of the security violation depends on the operation: • **PROG or EP**: CSEC.0 = 1 or DPxSEC.1 = 1 for the page addressed by FMADRH/L. • **ERS_G**: Any DPxSEC.0 = 1. • **ERS_DP**: DPxSEC.2 = 1 for addressed page while in execution mode. • **CRC_DP**: DPxCSEC.0 = 1 and DPxSEC.1 = 0.
	FMCMD.1	W	Command byte bit 1
2	-	R	Reserved
	FMCMD.2	W	Command byte bit 2.
3	-	R	Reserved
	FMCMD.3	W	Command byte bit 3.
4	DAP	R	Data Access Protect. When set, access to the data EEPROM is unmapped and thus prohibited. Set by the MAP command. Cleared by the UNMAP command.
	FMCMD.4	W	Command byte bit 4.
5	-	R	Reserved
	FMCMD.5	W	Command byte bit 5.
6	WE	R	When set, indicates that data EEPROM writes during program execution are enabled.
	FMCMD.6	W	Command byte bit 6.
7	BUSY	R	Indicates that a program, erase, CRC calculation or similar operation is in progress. Note that this bit is usable only in ICP mode since the CPU is stalled whenever this bit is set in execution mode.
	FMCMD.7	W	Command byte bit 7.

An assembly language routine to load the page register and perform an erase/program operation is shown below. This code assumes the data EEPROM has been mapped into user code space.

```
;*************************************************
;*    pgm user code          *
;*************************************************
;*
;                                                *

;* Inputs:                                                    *
;*R3 = number of bytes to program (byte)          *
;*R4 = page address MSB(byte)                     *
;*R5 = page address LSB(byte)                     *
;*R7 = pointer to data buffer in RAM(byte)        *
;* Outputs:                                                   *
;*R7 = status (byte)                                 *
;* C = clear on no error, set on error            *
;*************************************************
```

```
LOAD     EQU     00H
EP       EQU     68H

PGM_USER:
          MOV     FMCON,#LOAD   ;load command, clears page register
          MOV     FMADRH,R4     ;get high address
          MOV     FMADRL,R5     ;get low address
          MOV     A,R7          ;
          MOV     R0,A          ;get pointer into R0
 LOAD_PAGE:
          MOV     FMDAT,@R0     ;write data to page register
          INC     R0             ;point to next byte
          DJNZ    R3,LOAD_PAGE  ;do until count is zero
          MOV     FMCON,#EP     ;else erase & program the page

          MOV     R7,FMCON      ;copy status for return
          MOV     A,R7          ;read status
          ANL     A,#0FH        ;save only four lower bits
          JNZ     BAD            ;
          CLR     C              ;clear error flag if good
          RET                    ;and return
BAD:
          SETB    C             ;set error flag
          RET                    ;and return
```

A C-language routine to load the page register and perform an erase/program operation is shown below. This code assumes the data EEPROM has been mapped into user code space.

```
#include <REGV52.H>
unsigned char idata dbytes[64];// data buffer
unsigned char Fm_stat;// status result
bit PGM_USER (unsigned char, unsigned char);
bit prog_fail;
void main ()
{
     prog_fail=PGM_USER(0x1F,0xC0);
}

bit PGM_USER (unsigned char page_hi, unsigned char page_lo)
          {
                    #define LOAD0x00// clear page register, enable loading
                    #define EP0x68// erase & program page
                    unsigned char i;// loop count

           FMCON = LOAD;//load command, clears page reg
           FMADRH = page_hi;//
           FMADRL = page_lo;//write my page address to addr regs

           for(i=0;i<64;i=i+1)
               {
```

7. Limiting values

Table 43. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

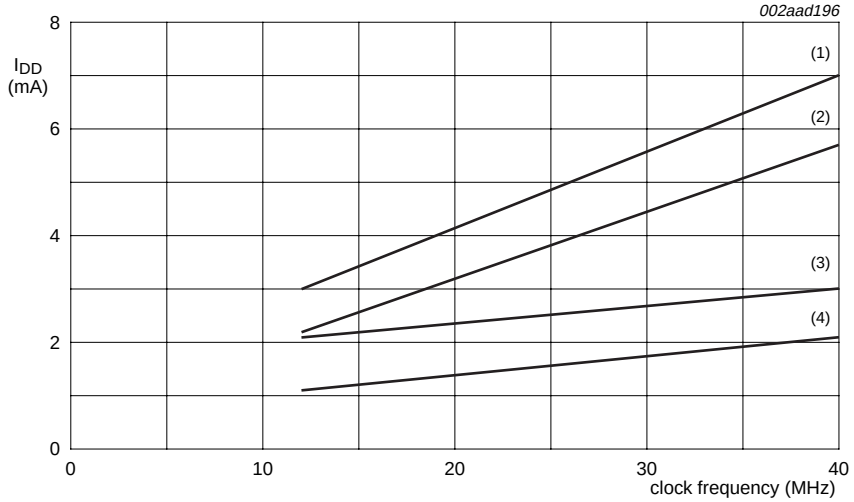
Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	15	mA
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 44. Static characteristics

T_{amb} = –40 °C to +85 °C; V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1]	10000	-		cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1]	100	-		years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1]	100 + I_{DD}	-		mA
V_{IL}	LOW-level input voltage			–0.5	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	6.0	V
V_{OL}	LOW-level output voltage	V_{DD} = 4.5 V	[2][3][4]		-		
		I_{OL} = 3.2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	V_{DD} = 2.7 V, ports 1, 2, 3	[5]		-		
		I_{OH} = –20 µA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V, ports 1, 2, 3	[5]		-		
		I_{OH} = –30 µA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V, Port 0 in External Bus mode, ALE, $\overline{PSEN}$			-		
		I_{OH} = –3.2 mA		V_{DD} – 0.7	-	-	V
I_{IL}	LOW-level input current	V_I = 0.4 V, ports 1, 2, 3		–1	-	–50	µA
I_{THL}	HIGH-LOW transition current	V_I = 2 V, ports 1, 2, 3	[6]	-	-	–650	µA
I_{LI}	input leakage current	0.45 V < V_I < V_{DD} – 0.3 V, port 0		-	-	±10	µA



(1) Maximum $I_{DD(oper)}$

(2) Typical $I_{DD(oper)}$

(3) Maximum $I_{DD(idle)}$

(4) Typical $I_{DD(idle)}$

Fig 20. I_{DD} vs. frequency

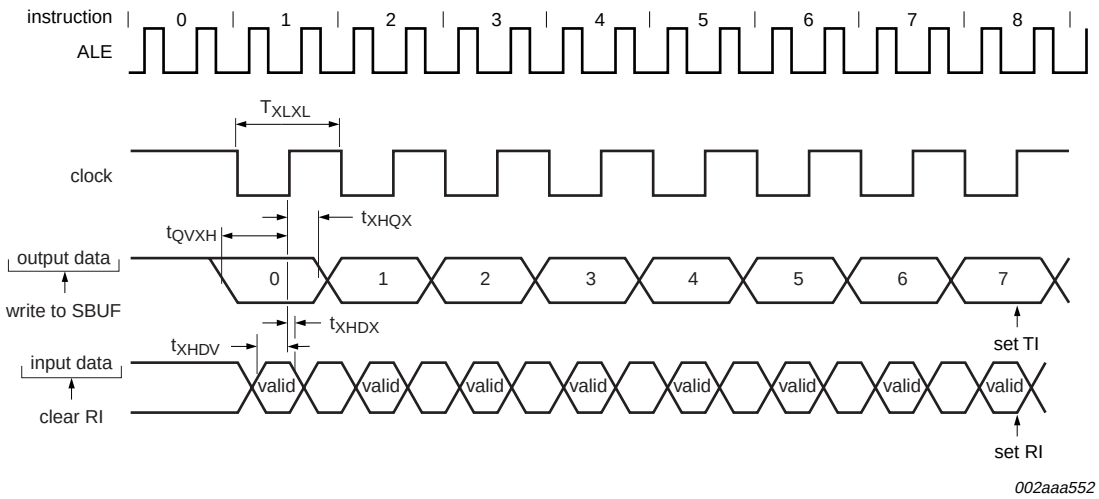


Fig 25. Shift register mode timing waveforms

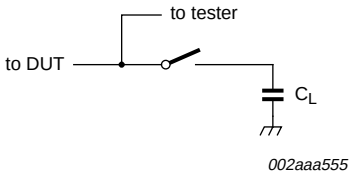
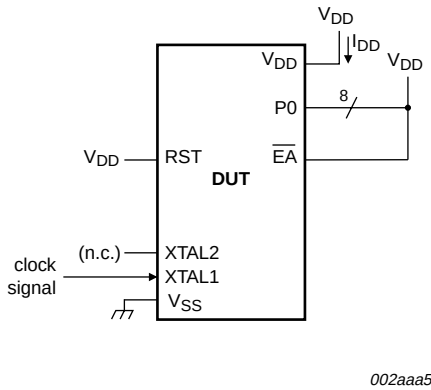
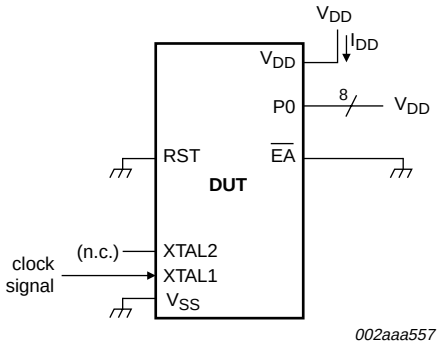


Fig 26. Test load example



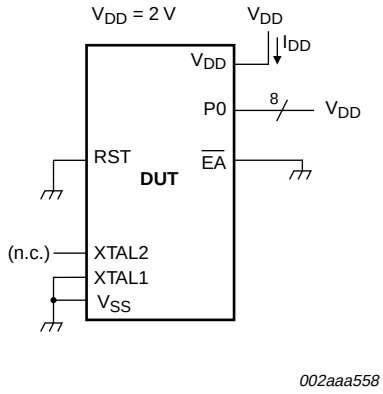
All other pins disconnected

Fig 27. I_{DD} test condition, active mode



All other pins disconnected

Fig 28. I_{DD} test condition, Idle mode

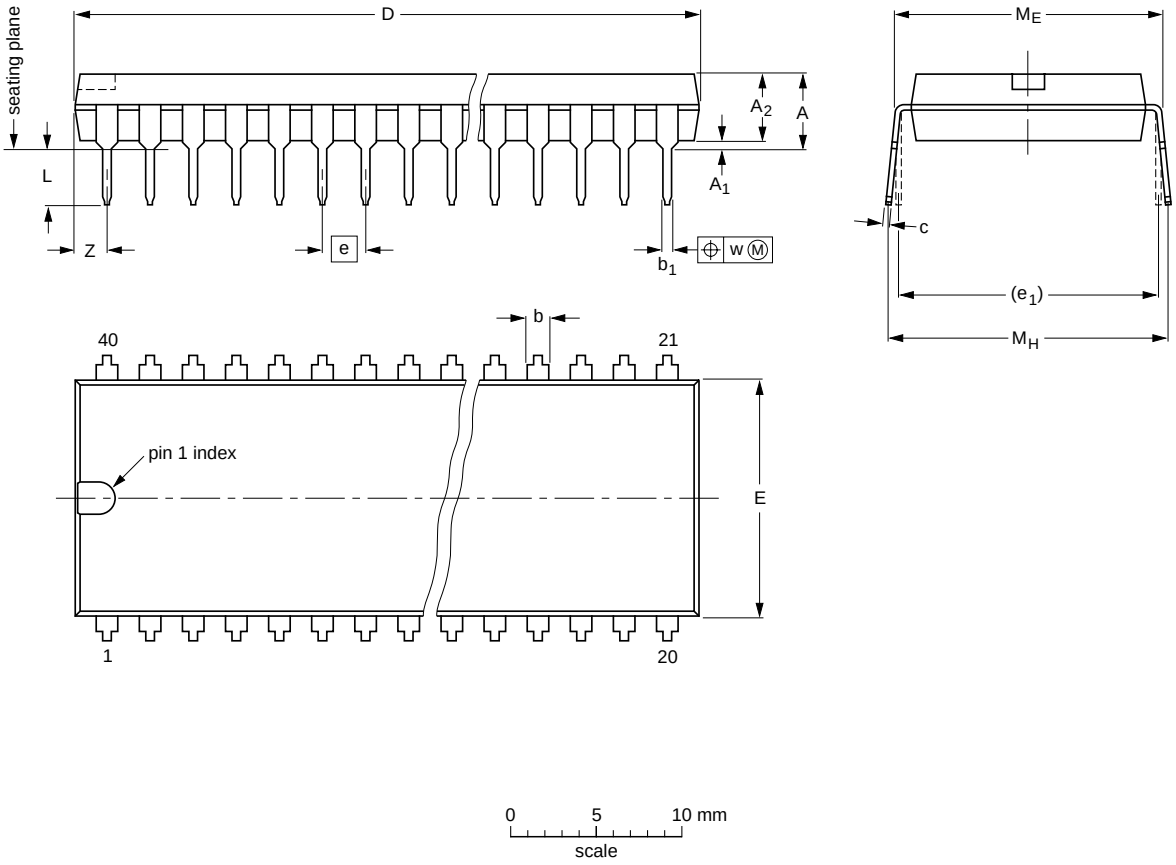


All other pins disconnected

Fig 29. I_{DD} test condition, Power-down mode

10. Package outline

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4	1.70 1.14	0.53 0.38	0.36 0.23	52.5 51.5	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.02	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.1	0.6	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT129-1	051G08	MO-015	SC-511-40			~~99-12-27~~ 03-02-13

Fig 30. Package outline SOT129-1 (DIP40)

11. Abbreviations

Table 48. Acronym list

Acronym	Description
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
IAP	In-Application Programming
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PWM	Pulse Width Modulator
RC	Resistance-Capacitance
RETI	Return From Interrupt
SFR	Special Function Register
UART	Universal Asynchronous Receiver/Transmitter

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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