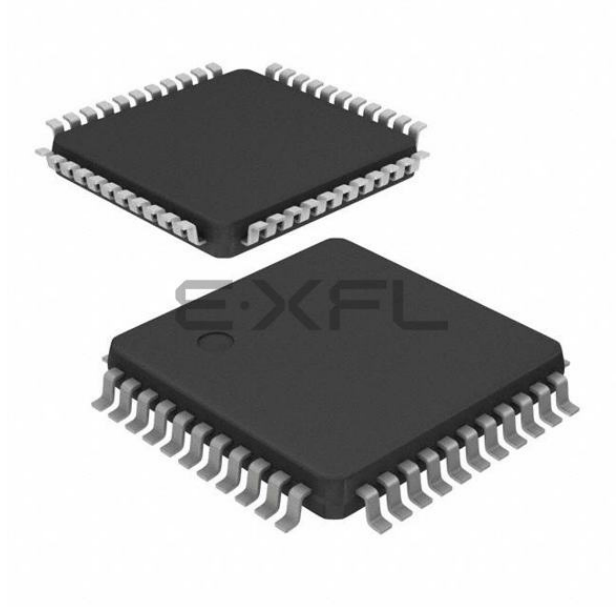

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	192 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v52x2fbd-157

3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
P89V52X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P89V52X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89V52X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

4. Block diagram

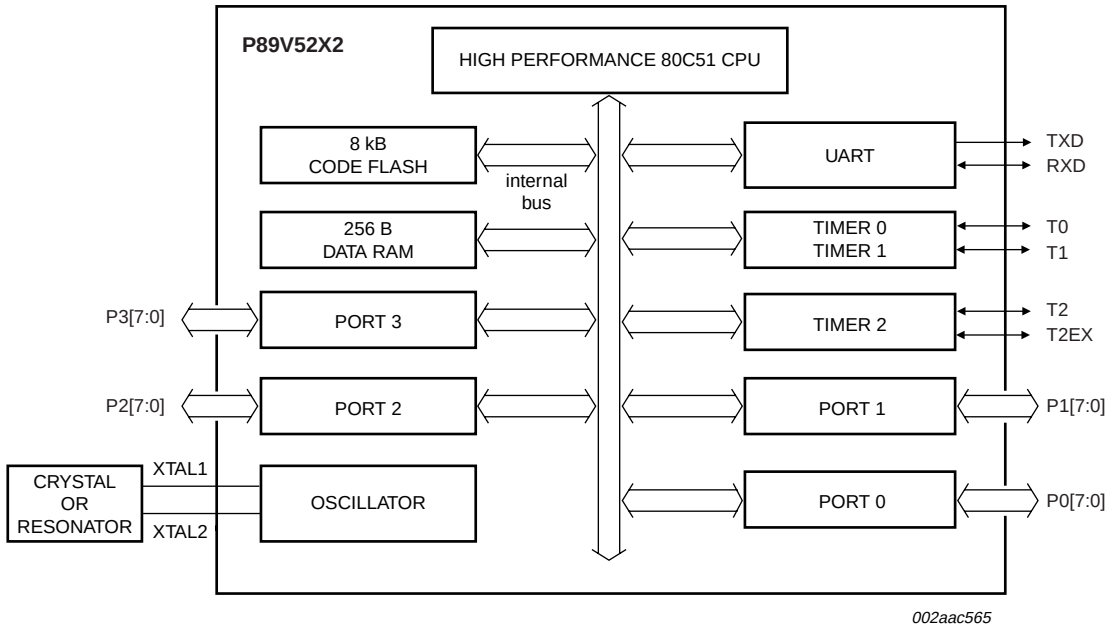


Fig 1. Block diagram

5.2 Pin description

Table 2. Pin description

Symbol	Pin			Type	Description
	DIP40	LQFP44	PLCC44		
P0[0] to P0[7]				I/O	**Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. External pull-ups are required as a general purpose I/O port.
P0[0]/AD0	39	37	43	I/O	**P0[0] —** Port 0 bit 0.
				I/O	**AD0 —** Address/data bit 0.
P0[1]/AD1	38	36	42	I/O	**P0[1] —** Port 0 bit 1.
				I/O	**AD1 —** Address/data bit 1.
P0[2]/AD2	37	35	41	I/O	**P0[2] —** Port 0 bit 2.
				I/O	**AD2 —** Address/data bit 2.
P0[3]/AD3	36	34	40	I/O	**P0[3] —** Port 0 bit 3.
				I/O	**AD3 —** Address/data bit 3.
P0[4]/AD4	35	33	39	I/O	**P0[4] —** Port 0 bit 4.
				I/O	**AD4 —** Address/data bit 4.
P0[5]/AD5	34	32	38	I/O	**P0[5] —** Port 0 bit 5.
				I/O	**AD5 —** Address/data bit 5.
P0[6]/AD6	33	31	37	I/O	**P0[6] —** Port 0 bit 6.
				I/O	**AD6 —** Address/data bit 6.
P0[7]/AD7	32	30	36	I/O	**P0[7] —** Port 0 bit 7.
				I/O	**AD7 —** Address/data bit 7.
P1[0] to P1[7]				I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. P1[5], P1[6], P1[7] have high current drive of 16 mA.
P1[0]/T2	1	40	2	I/O	**P1[0] —** Port 1 bit 0.
				I	**T2 —** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]/T2EX	2	41	3	I/O	**P1[1] —** Port 1 bit 1.
				I	**T2EX**: Timer/Counter 2 capture/reload trigger and direction control
P1[2]	3	42	4	I/O	**P1[2] —** Port 1 bit 2.
P1[3]	4	43	5	I/O	**P1[3] —** Port 1 bit 3.
P1[4]	5	44	6	I/O	**P1[4] —** Port 1 bit 4.
P1[5]	6	1	7	I/O	**P1[5] —** Port 1 bit 5.
P1[6]	7	2	8	I/O	**P1[6] —** Port 1 bit 6.

Table 3. Special function registers[1]

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0
ACC*	Accumulator	E0H	-	-	-	-	-	-	-	-
AUXR	Auxiliary function register	8EH	-	-	-	-	-	-	-	AO
AUXR1	Auxiliary function register 1	A2H	-	-	-		GF2	0	-	DPS
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0
B*	B register	F0H	-	-	-	-	-	-	-	-
CKCON	B register	8FH	-	-	-	-	-	-	-	X2
DPTR	Data Pointer (2 B)									
DPH	Data Pointer HIGH	83H	-	-	-	-	-	-	-	-
DPL	Data Pointer LOW	82H	-	-	-	-	-	-	-	-
FMCON	Flash control register (R)	F4H	BUSY	WE	-	DAP	-	-	SV	ERR
	Flash control register (W)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0
FMDATA	Flash data register	F5H	-	-	-	-	-	-	-	-
FMADRH	Flash memory address HIGH	F6H	-	-	-	-	-	-	-	-
FMADRL	Flash memory address LOW	F7H	-	-	-	-	-	-	-	-
		Bit address	AF	AE	AD	AC	AB	AA	A9	A8
IE*	Interrupt Enable 0	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8
IP*	Interrupt Priority 0	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0
IPH	Interrupt Priority 0 HIGH	B7H	-	-	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H
		Bit address	87	86	85	84	83	82	81	80
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Bit address	97	96	95	94	93	92	91	90
P1*	Port 1	90H	-	-	-	-	-	-	T2EX	T2
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD
PCON	Power Control Register	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Table 3. Special function registers[1] *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	-	P
RCAP2H	Timer2 Capture HIGH	CBH	-	-	-	-	-	-	-	-
RCAP2L	Timer2 Capture LOW	CAH	-	-	-	-	-	-	-	-
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**
SCON*	Serial Port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	Serial Port Data Buffer Register	99H	-	-	-	-	-	-	-	-
SADDR	Serial Port Address Register	A9H	-	-	-	-	-	-	-	-
SADEN	Serial Port Address Enable	B9H	-	-	-	-	-	-	-	-
SP	Stack Pointer	81H	-	-	-	-	-	-	-	-
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**
TCON*	Timer Control Register	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Bit address	**CF**	**CE**	**CD**	**CC**	**CB**	**CA**	**C9**	**C8**
T2CON*	Timer2 Control Register	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
T2MOD	Timer2 mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN
TH0	Timer 0 HIGH	8CH	-	-	-	-	-	-	-	-
TH1	Timer 1 HIGH	8DH	-	-	-	-	-	-	-	-
TH2	Timer 2 HIGH	CDH	-	-	-	-	-	-	-	-
TL0	Timer 0 LOW	8AH	-	-	-	-	-	-	-	-
TL1	Timer 1 LOW	8BH	-	-	-	-	-	-	-	-
TL2	Timer 2 LOW	CCH	-	-	-	-	-	-	-	-
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

[1] Unimplemented bits in SFRs (labeled '-') are 'X's (unknown) at all times. Unless otherwise specified, '1's should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

6.2 Memory organization

The various P89V52X2 memory spaces are as follows:

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 B of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 B immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89V52X2 has 8 kB of on-chip Code memory.

6.3 System clock and clock options

6.3.1 Clock input options and recommended capacitor values for the oscillator

Shown in Figure 5 and Figure 6 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven. Power consumption can be further reduced by programming the EXTCLK bit (UCFG.0).

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Resonator manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C_1 and C_2 should be adjusted appropriately for each design. Table 4 shows the typical values for C_1 and C_2 vs. resonator type for various frequencies.

Table 4. Recommended values for C_1 and C_2 by crystal type

Resonator	$C_1 = C_2$
Quartz	20 pF to 30 pF
Ceramic	40 pF to 50 pF

Table 14. TCON - Timer/Counter control register (address 88H) bit description *...continued*

Bit	Symbol	Description
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/LOW-level is detected. Cleared by hardware when the interrupt is processed, or by software.
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/LOW-level that triggers external interrupt 1.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge/LOW-level is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/LOW-level that triggers external interrupt 0.

6.8.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a fixed divide-by-32 prescaler. Figure 10 shows Mode 0 operation.

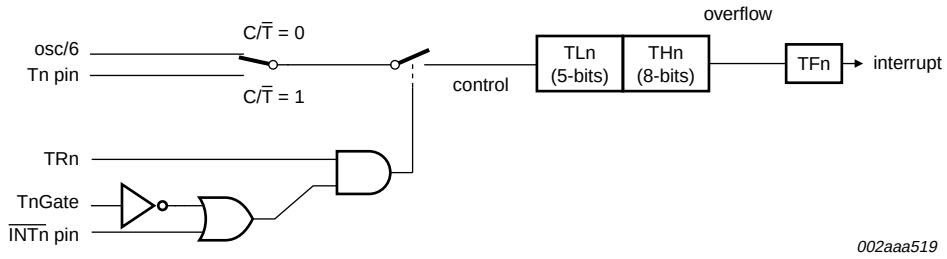


Fig 10. Timer/Counter 0 or 1 in Mode 0 (13-bit counter)

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Figure 8). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1 (see Figure 10). There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

6.8.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 11.

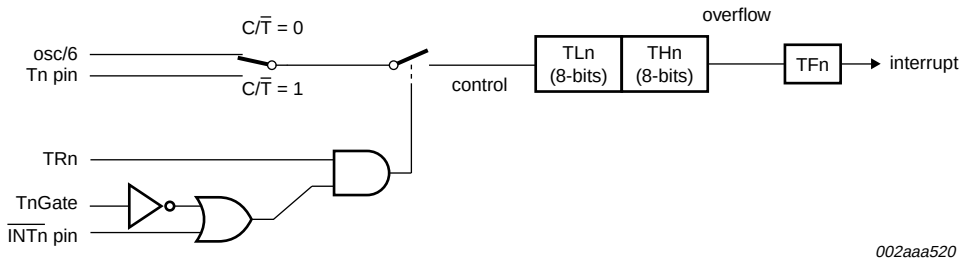


Fig 11. Timer/Counter 0 or 1 in Mode 1 (16-bit counter)

6.8.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 12. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

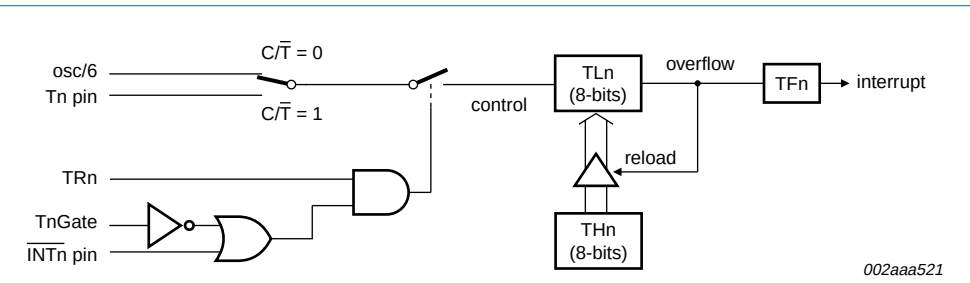


Fig 12. Timer/Counter 0 or 1 in Mode 2 (8-bit auto-reload)

6.8.4 Mode 3

When timer 1 is in Mode 3 it is stopped (holds its count). The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 and Timer 0 is shown in Figure 13. TL0 uses the Timer 0 control bits: T0C/$\overline{T}$, T0GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the 'Timer 1' interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in Mode 3, the P89V52X2 can look like it has an additional Timer.

Note: When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

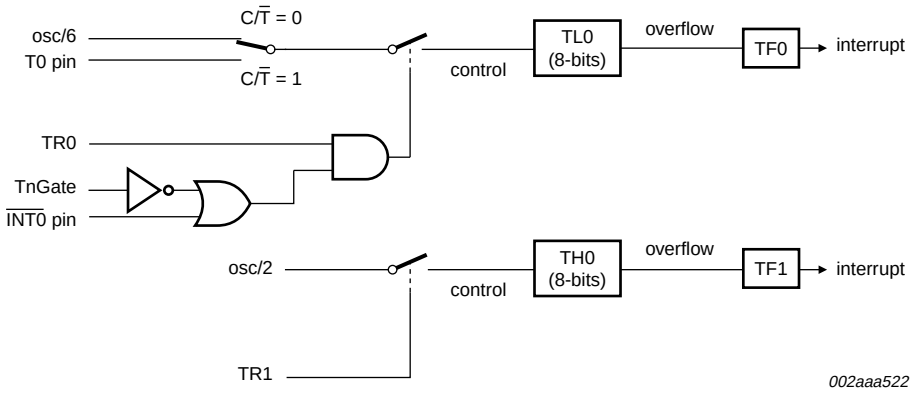


Fig 13. Timer/Counter 0 Mode 3 (two 8-bit counters)

6.9 Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2 in the special function register T2CON. Timer 2 has four operating modes: Capture, Auto-reload (up or down counting), Clock-out, and Baud Rate Generator which are selected according to Table 15 using T2CON (Table 16 and Table 17) and T2MOD (Table 18 and Table 19).

Table 15. Timer 2 operating mode

RCLK+TCLK	CP/$\overline{RL2}$	TR2	T2OE	Mode
0	0	1	0	16-bit auto reload
0	1	1	0	16-bit capture
0	0	1	1	Programmable Clock-Out
1	X	1	0	Baud rate generator
X	X	0	X	off

Table 16. T2CON - Timer/Counter 2 control register (address C8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 17. T2CON - Timer/Counter 2 control register (address C8H) bit description

Bit	Symbol	Description
7	TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1 or when Timer 2 is in Clock-out mode.
6	EXF2	Timer 2 external flag is set when Timer 2 is in capture, reload or baud rate mode, EXEN2 = 1 and a negative transition on T2EX occurs. If Timer 2 interrupt is enabled EXF2 = 1 causes the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
5	RCLK	Receive clock flag. When set, causes the UART to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

used as the UART transmit baud rate generator. RCLK has the same effect for the UART receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – Timer 1 or Timer 2.

Figure 17 shows Timer 2 in baud rate generator mode:

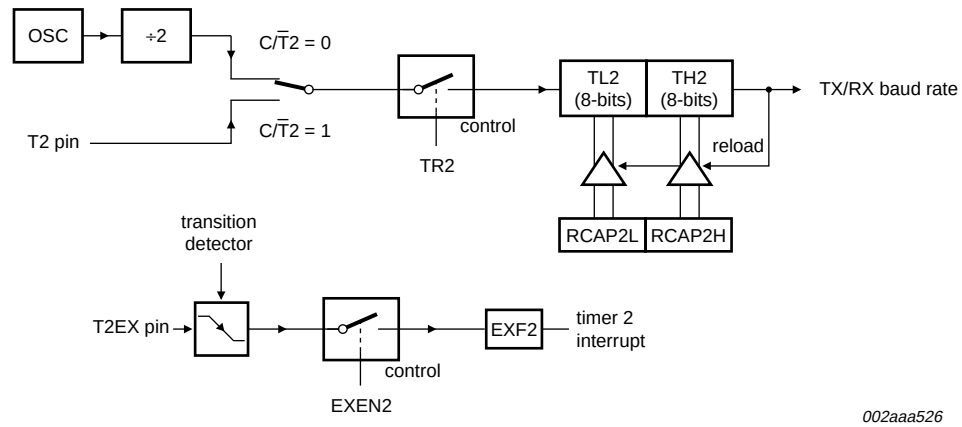


Fig 17. Timer 2 in Baud Rate Generator mode

The baud rate generation mode is like the auto-reload mode, when a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

Modes 1 and 3 Baud Rates = Timer 2 Overflow Rate/16

The timer can be configured for either 'timer' or 'counter' operation. In many applications, it is configured for 'timer' operation (C/$\overline{T}$2 = 0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., $\frac{1}{6}$ the oscillator frequency). As a baud rate generator, it increments at the oscillator frequency. Thus the baud rate formula is as follows:

Modes 1 and 3 Baud Rates =

$$\frac{OscillatorFrequency}{(16 \times (65536 - (RCAP2H, RCAP2L)))} \quad (3)$$

Where: (RCAP2H, RCAP2L) = The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

- Map the data EEPROM into code memory space if not already mapped.
- Write the data EEPROM byte address into the DPTR.
- Use the MOVC instruction to read the data EEPROM.

6.13.5 Erasing a complete page (64 B)

A complete page can be erased by performing the following sequence:

- Map the data EEPROM into code memory space if not already mapped.
- Write the lower 8-bits of the data EEPROM page's start address into FMADRL.
- Write the ERS_DP command (33H) to FMCON.

Once the ERS_DP command is written to FMCON, code execution will stall until the operation is completed, approximately 6 ms.

6.13.6 Data EEPROM programming and erasing using the page register

In addition to page erase, a 64 B page register is included which allows from 1 B to 64 B of a given page to be programmed or erase/programmed at the same time, substantially reducing overall programming time. Two programming operations are provided:

- Program only operation. This operation used the PROG (48H) command and programs the contents of the page register into the data EEPROM page. This operation requires that the bytes being programmed have been previously erased. This operation requires approximately 2 ms to complete.
- Erase and Program operation. This operation uses the EP (68H) command to both erase and program the bytes previously loaded into the page register. This command is often useful to erase and reprogram a single byte of data. This operation requires approximately 4 ms to complete.

The page register consists of 64 B and an update flag for each byte. When a LOAD command is issued to FMCON the page register contents and all of the update flags will be cleared. When FMDATA is written, the value written to FMDATA will be stored in the page register at the location specified by the lower 6 bits of FMADRL. In addition, the update flag for that location will be set. FMADRL will auto-increment to the next location. Auto-increment after writing to the last byte in the page register will 'wrap-around' to the first byte in the page register, but will not affect FMADRL[7:6]. Bytes loaded into the page register do not have to be continuous. Any byte location can be loaded into the page register by changing the contents of FMADRL prior to writing to FMDATA. However, each location in the page register can only be written once following each LOAD command. Attempts to write to a page register location more than once should be avoided.

FMADRH and FMADRL[7:6] are used to specify a page in the code memory space. When the PROG command is written to FMCON, the locations within the data EEPROM page that correspond to updated locations in the page register will have their contents programmed with the contents of their corresponding locations in the page register. Only the bytes that were loaded into the page register will be programmed in the data EEPROM array. Other bytes within the data EEPROM array will not be affected. The EP command works similarly except that If the EP command is written, the corresponding bytes in the data EEPROM will be erased prior to being programmed. This is often useful for erasing and programming a small number of bytes or even a single byte.

```
                                FMDATA = dbytes[i];
                        }
                FMCON = EP;//erase & prog page command
                Fm_stat = FMCON;//read the result status
                if ((Fm_stat & 0x0F)!=0) prog_fail=1; else prog_fail=0;
                return(prog_fail);
        }
```

6.13.7 Data EEPROM write enable

The data EEPROM has a Write Enable mechanism to help prevent against inadvertent writes. If the WE bit (FMCON.6) is set writes to the data EEPROM are enabled. When cleared, writes are disabled. This bit only affects execution mode. The WE bit is set when:

- The disable write enable bit, DISWE (UCFG.2) = 1
- In ICP mode
- The SET_WE (08H) command is written to FMCON followed by the key value (96H) being written to FMDATA

The WE bit is cleared following any reset. The WE bit may also be cleared by writing the CLR_WE (0BH) command to FMCON.

6.13.8 Data EEPROM security bits

The data EEPROM security bits protects each data EEPROM page. The data EEPROM page security bits and their effects are shown in Table 35.

Table 35. DPxSEC - Data page X security register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	XERSx	PWRx	MOVCx

Table 36. DPxSEC - Data page X security register bit description

Bit	Symbol	Description
7 to 3	-	Reserved
2	XERSx	Execution Erase Protect x. When programmed = 1, cannot be erased with ERS_DP command in execution mode. ERS_DP can be used in ICP mode.
1	PWRx	Page Write Protect x. When programmed = 1, data EEPROM cannot be erased or programmed using PROG or EP commands.
0	MOVCx	When programmed = 1, prevents instructions fetched from off-chip from reading the contents of the data EEPROM and returns FFH. CRC_DP are disabled if the corresponding Page Write Protect is disabled.

6.13.9 Summary of data EEPROM commands

Table 37 is a summary of the FMCON commands related to the data EEPROM.

Table 40. UCFG - User configuration register bit description

Bit	Symbol	Description
7 to 3	-	Reserved
2	ENW	Enable Write. When programmed = 1, forces the WE bit to be set.
1	FX2	Force X2. When programmed = 1, the device is in 6-clock mode. When erased = 0, the mode depends on the state of the X2 bit in CKCON.
0	EXTCLK	External Clock. When programmed = 1, disables the XTAL block when using an external digital clock source.

6.16 Code security (CSEC) bits

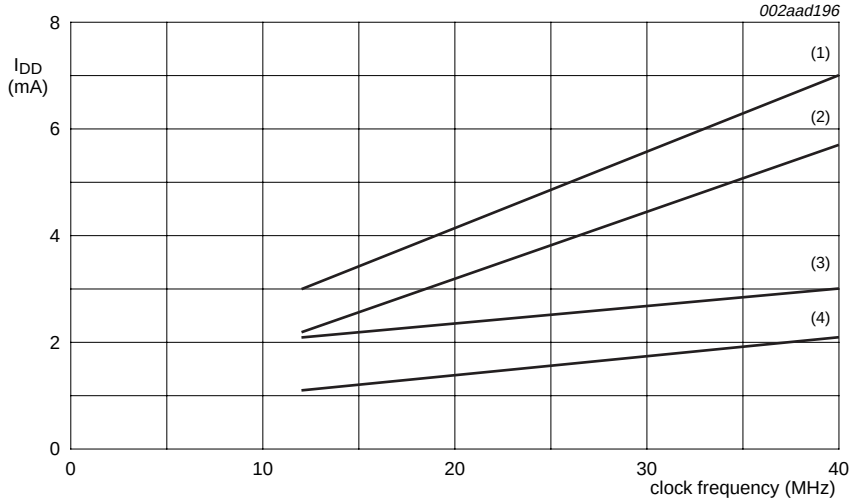
The code security bits protect against software piracy and prevent the contents of the flash from being read by unauthorized parties. The code security bits and their effects are shown in Table 41.

Table 41. CSEC - Code security register bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	INTEXEC	PROT

Table 42. CSEC - Code security register bit description

Bit	Symbol	Description
7 to 2	-	Reserved
1	INTEXEC	Internal execution only. When programmed, if the internal address space is exceeded, the address will rollover into internal space (upper address bits are ignored) for MOVC and instruction fetches. MOVC will access the data EEPROM when the address >= FF00H.
0	PROT	Protect. When programmed, prohibits further erasing or programming of code memory. MOVC instructions executed from external code memory are disabled from fetching code bytes from internal code memory.



(1) Maximum $I_{DD(oper)}$

(2) Typical $I_{DD(oper)}$

(3) Maximum $I_{DD(idle)}$

(4) Typical $I_{DD(idle)}$

Fig 20. I_{DD} vs. frequency

9. Dynamic characteristics

Table 45. Dynamic characteristics

Over operating conditions: load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 5.5 V; V_{SS} = 0 V[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{osc}	oscillator frequency	12-clock mode	0	40	MHz
		6-clock mode	0	20	MHz
t_{LHLL}	ALE pulse width		$2T_{cy(clk)} - 15$	-	ns
t_{AVLL}	address valid to ALE LOW time		$T_{cy(clk)} - 15$	-	ns
t_{LLAX}	address hold after ALE LOW time		$T_{cy(clk)} - 15$	-	ns
t_{LLIV}	ALE LOW to valid instruction in time		-	$4T_{cy(clk)} - 45$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW time		$T_{cy(clk)} - 15$	-	ns
t_{PLPH}	$\overline{PSEN}$ pulse width		$3T_{cy(clk)} - 15$	-	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in time		-	$3T_{cy(clk)} - 55$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$ time		0	-	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$ time		-	$T_{cy(clk)} - 20$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid time		$T_{cy(clk)} - 8$	-	ns
t_{AVIV}	address to valid instruction in time		-	$5T_{cy(clk)} - 60$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float time		-	10	ns
t_{RLRH}	$\overline{RD}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	ns
t_{WLWH}	$\overline{WR}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in time		-	$5T_{cy(clk)} - 50$	ns
t_{RHDX}	data hold after $\overline{RD}$ time		0	-	ns
t_{RHDZ}	data float after $\overline{RD}$ time		-	$2T_{cy(clk)} - 12$	ns
t_{LLDV}	ALE LOW to valid data in time		-	$8T_{cy(clk)} - 50$	ns
t_{AVDV}	address to valid data in time		-	$9T_{cy(clk)} - 75$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW time		$3T_{cy(clk)} - 15$	$3T_{cy(clk)} + 15$	ns
t_{AVWL}	address to $\overline{RD}$ or $\overline{WR}$ LOW time		$4T_{cy(clk)} - 30$	-	ns
t_{WHQX}	data hold after $\overline{WR}$ time		$T_{cy(clk)} - 20$	-	ns
t_{QVWH}	data output valid to $\overline{WR}$ HIGH time		$7T_{cy(clk)} - 50$	-	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float time		-	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH time		$T_{cy(clk)} - 15$	$T_{cy(clk)} + 15$	ns

[1] $T_{cy(clk)} = 1/f_{osc}$.

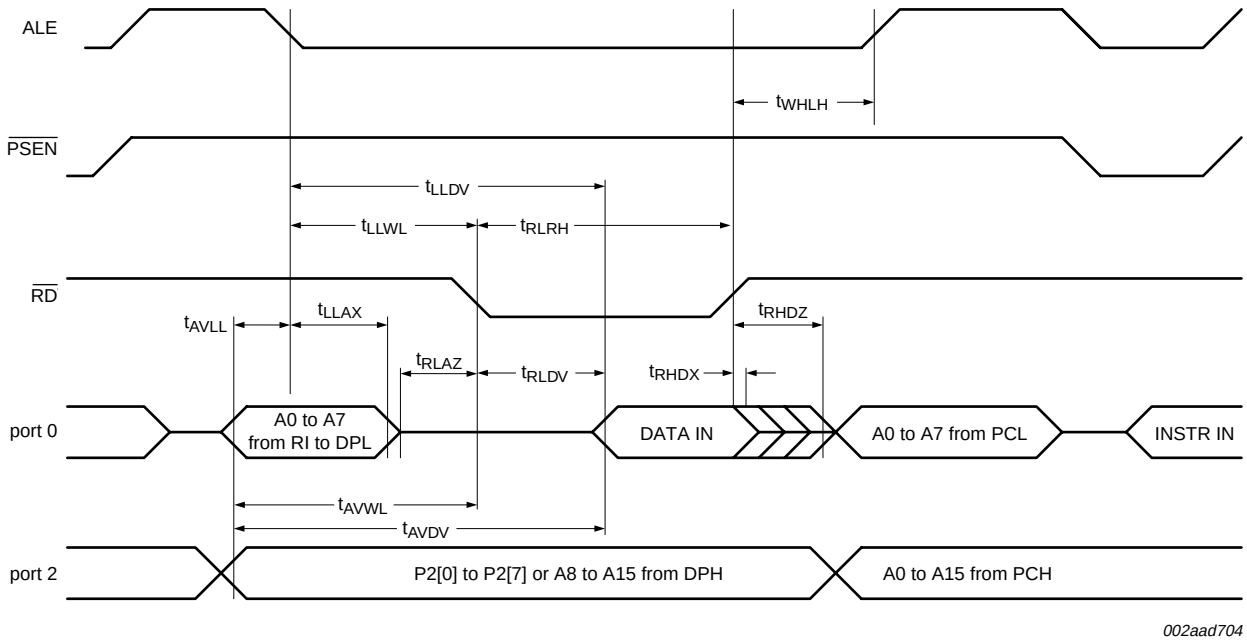


Fig 22. External data memory read cycle

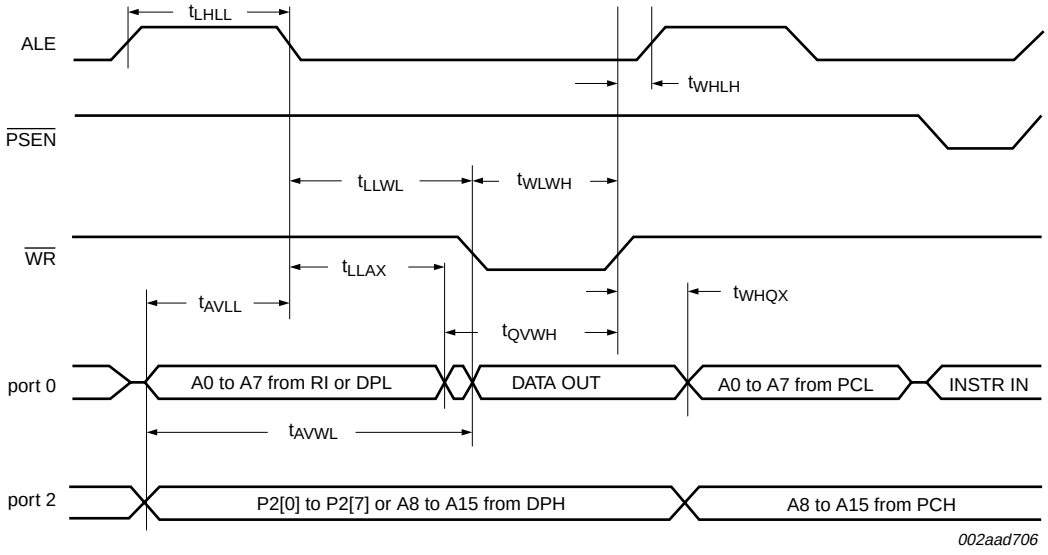


Fig 23. External data memory write cycle

Table 46. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

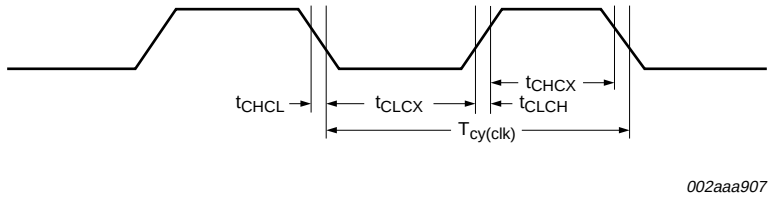
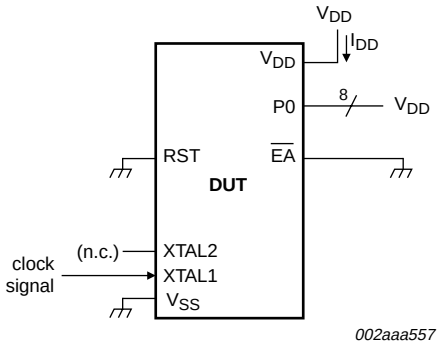


Fig 24. External clock drive waveform (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

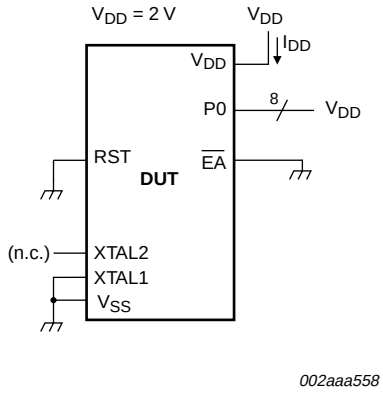
Table 47. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 15$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns



All other pins disconnected

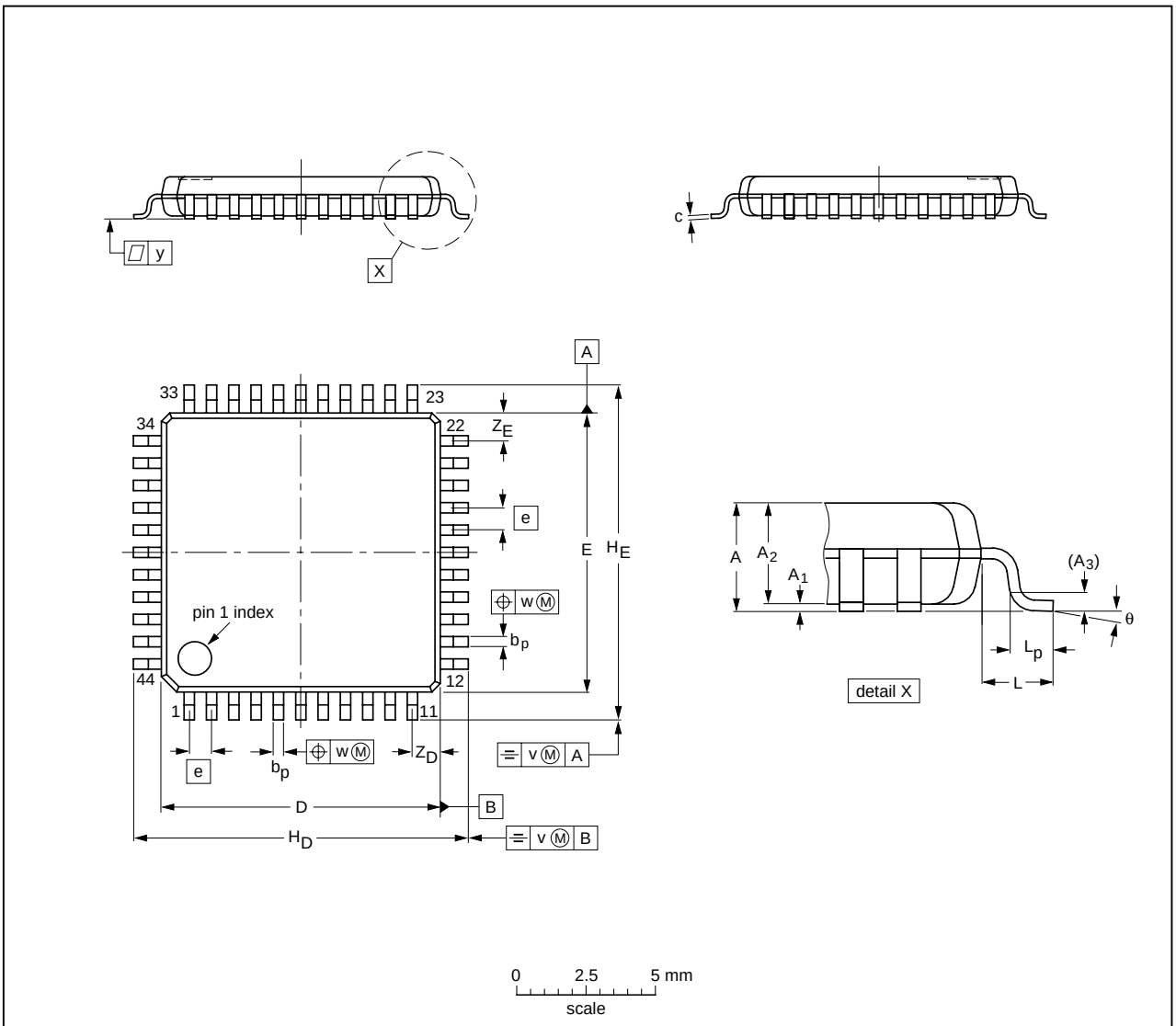
Fig 28. I_{DD} test condition, Idle mode



All other pins disconnected

Fig 29. I_{DD} test condition, Power-down mode

LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.14 0.85	1.14 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT389-1	136E08	MS-026				~~00-01-19~~ 02-06-07

Fig 31. Package outline SOT389-1 (LQFP44)

11. Abbreviations

Table 48. Acronym list

Acronym	Description
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
IAP	In-Application Programming
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PWM	Pulse Width Modulator
RC	Resistance-Capacitance
RETI	Return From Interrupt
SFR	Special Function Register
UART	Universal Asynchronous Receiver/Transmitter

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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