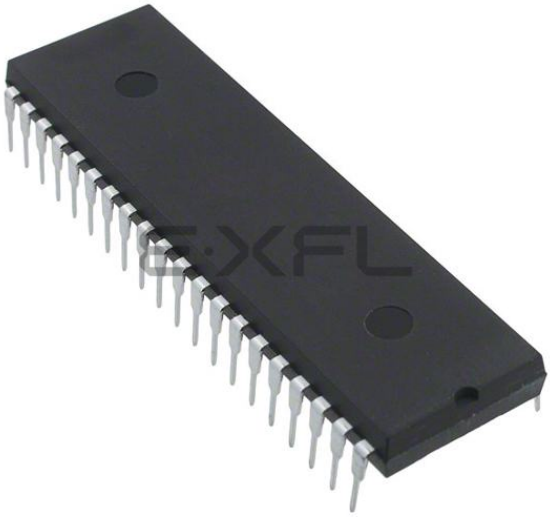

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	192 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v52x2fn-112

3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
P89V52X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P89V52X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89V52X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

4. Block diagram

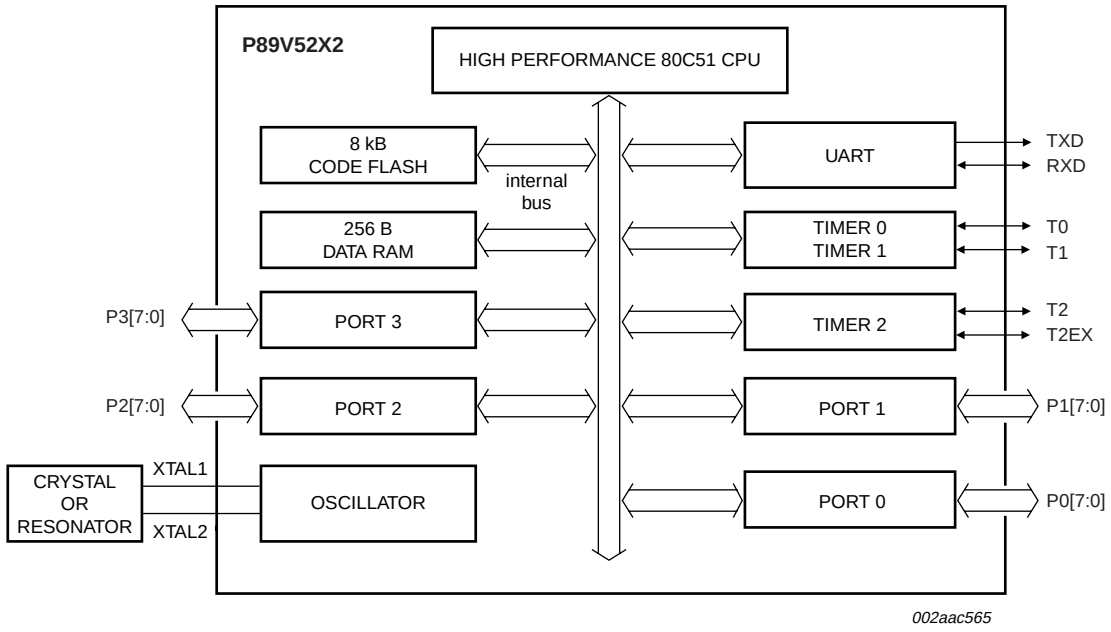


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

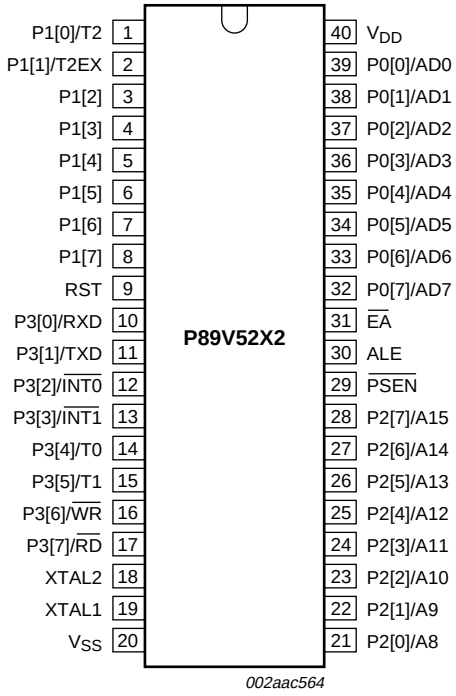


Fig 2. DIP40 pin configuration

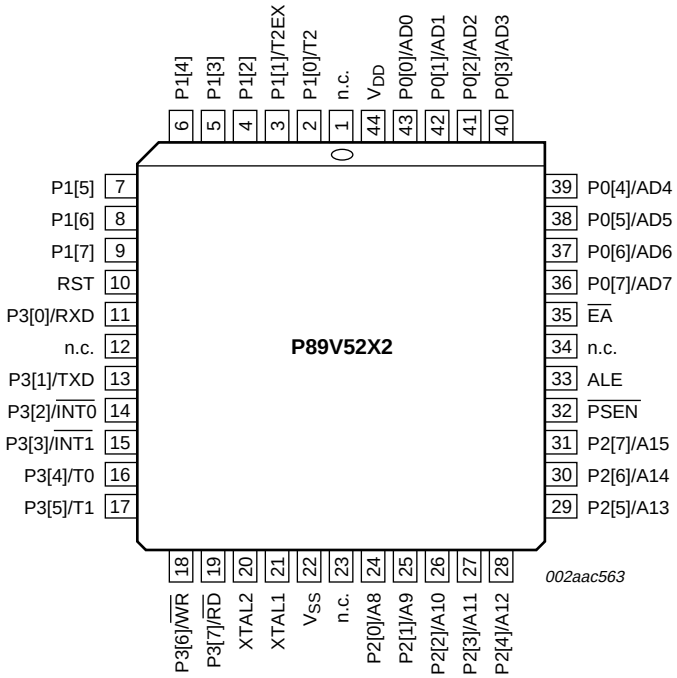


Fig 3. PLCC44 pin configuration

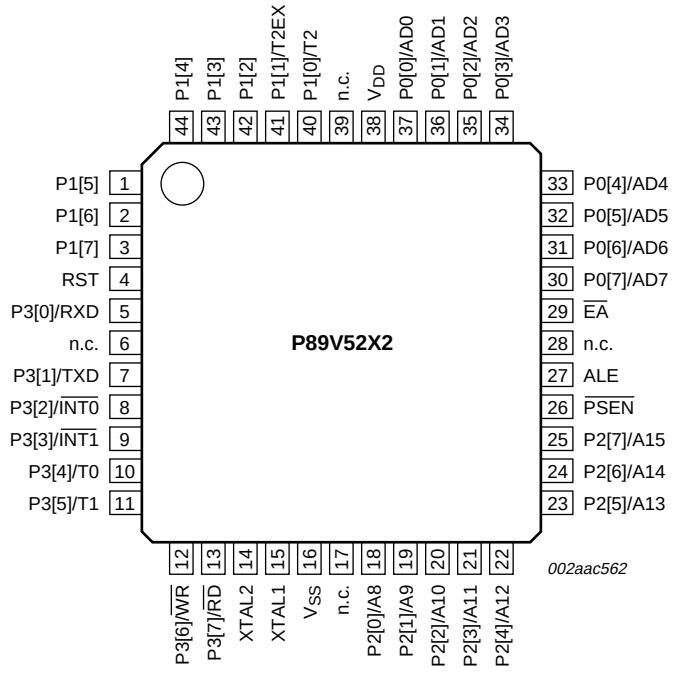


Fig 4. LQFP44 pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin			Type	Description
	DIP40	LQFP44	PLCC44		
P0[0] to P0[7]				I/O	**Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. External pull-ups are required as a general purpose I/O port.
P0[0]/AD0	39	37	43	I/O	**P0[0] —** Port 0 bit 0.
				I/O	**AD0 —** Address/data bit 0.
P0[1]/AD1	38	36	42	I/O	**P0[1] —** Port 0 bit 1.
				I/O	**AD1 —** Address/data bit 1.
P0[2]/AD2	37	35	41	I/O	**P0[2] —** Port 0 bit 2.
				I/O	**AD2 —** Address/data bit 2.
P0[3]/AD3	36	34	40	I/O	**P0[3] —** Port 0 bit 3.
				I/O	**AD3 —** Address/data bit 3.
P0[4]/AD4	35	33	39	I/O	**P0[4] —** Port 0 bit 4.
				I/O	**AD4 —** Address/data bit 4.
P0[5]/AD5	34	32	38	I/O	**P0[5] —** Port 0 bit 5.
				I/O	**AD5 —** Address/data bit 5.
P0[6]/AD6	33	31	37	I/O	**P0[6] —** Port 0 bit 6.
				I/O	**AD6 —** Address/data bit 6.
P0[7]/AD7	32	30	36	I/O	**P0[7] —** Port 0 bit 7.
				I/O	**AD7 —** Address/data bit 7.
P1[0] to P1[7]				I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. P1[5], P1[6], P1[7] have high current drive of 16 mA.
P1[0]/T2	1	40	2	I/O	**P1[0] —** Port 1 bit 0.
				I	**T2 —** External count input to Timer/Counter 2 or Clock-out from Timer/Counter 2
P1[1]/T2EX	2	41	3	I/O	**P1[1] —** Port 1 bit 1.
				I	**T2EX**: Timer/Counter 2 capture/reload trigger and direction control
P1[2]	3	42	4	I/O	**P1[2] —** Port 1 bit 2.
P1[3]	4	43	5	I/O	**P1[3] —** Port 1 bit 3.
P1[4]	5	44	6	I/O	**P1[4] —** Port 1 bit 4.
P1[5]	6	1	7	I/O	**P1[5] —** Port 1 bit 5.
P1[6]	7	2	8	I/O	**P1[6] —** Port 1 bit 6.

Table 3. Special function registers[1]

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses							
			MSB							LSB
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0
ACC*	Accumulator	E0H	-	-	-	-	-	-	-	-
AUXR	Auxiliary function register	8EH	-	-	-	-	-	-	-	AO
AUXR1	Auxiliary function register 1	A2H	-	-	-		GF2	0	-	DPS
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0
B*	B register	F0H	-	-	-	-	-	-	-	-
CKCON	B register	8FH	-	-	-	-	-	-	-	X2
DPTR	Data Pointer (2 B)									
DPH	Data Pointer HIGH	83H	-	-	-	-	-	-	-	-
DPL	Data Pointer LOW	82H	-	-	-	-	-	-	-	-
FMCON	Flash control register (R)	F4H	BUSY	WE	-	DAP	-	-	SV	ERR
	Flash control register (W)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0
FMDATA	Flash data register	F5H	-	-	-	-	-	-	-	-
FMADRH	Flash memory address HIGH	F6H	-	-	-	-	-	-	-	-
FMADRL	Flash memory address LOW	F7H	-	-	-	-	-	-	-	-
		Bit address	AF	AE	AD	AC	AB	AA	A9	A8
IE*	Interrupt Enable 0	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8
IP*	Interrupt Priority 0	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0
IPH	Interrupt Priority 0 HIGH	B7H	-	-	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H
		Bit address	87	86	85	84	83	82	81	80
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Bit address	97	96	95	94	93	92	91	90
P1*	Port 1	90H	-	-	-	-	-	-	T2EX	T2
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD
PCON	Power Control Register	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

6.2 Memory organization

The various P89V52X2 memory spaces are as follows:

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 B of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 B immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89V52X2 has 8 kB of on-chip Code memory.

6.3 System clock and clock options

6.3.1 Clock input options and recommended capacitor values for the oscillator

Shown in Figure 5 and Figure 6 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven. Power consumption can be further reduced by programming the EXTCLK bit (UCFG.0).

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Resonator manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C_1 and C_2 should be adjusted appropriately for each design. Table 4 shows the typical values for C_1 and C_2 vs. resonator type for various frequencies.

Table 4. Recommended values for C_1 and C_2 by crystal type

Resonator	$C_1 = C_2$
Quartz	20 pF to 30 pF
Ceramic	40 pF to 50 pF

Table 9. AUXR1 - Auxiliary register 1 (address A2H) bit description

Bit	Symbol	Description
7 to 4	-	Reserved for future use. Should be set to '0' by user programs.
3	GF2	General purpose user-defined flag.
2	0	This bit contains a hard-wired '0'. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to '0' by user programs.
0	DPS	Data pointer select. Chooses one of two Data Pointers for use by the program. See text for details.

6.6 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins HIGH. Powering up the device without a valid reset could cause the device to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held HIGH long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 9.

During initial power the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

Following a reset condition, under normal conditions, the device will start executing code from address 0000H in the user's code memory. However if the requirements are met for ICP entry, the device will enter ICP mode.

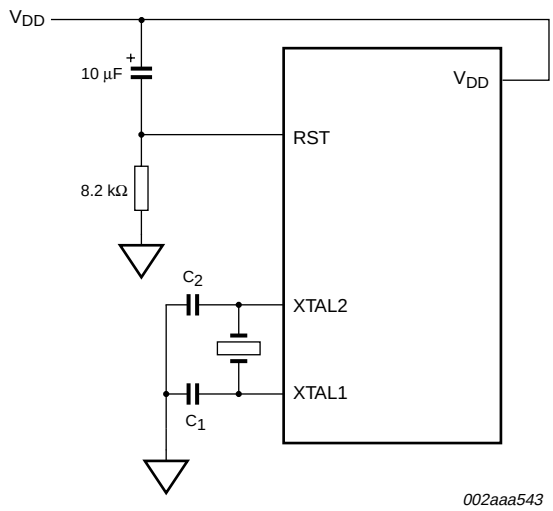


Fig 9. Power-on reset circuit

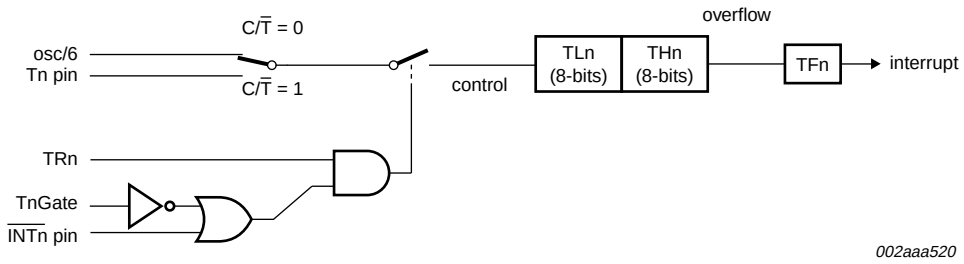


Fig 11. Timer/Counter 0 or 1 in Mode 1 (16-bit counter)

6.8.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 12. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

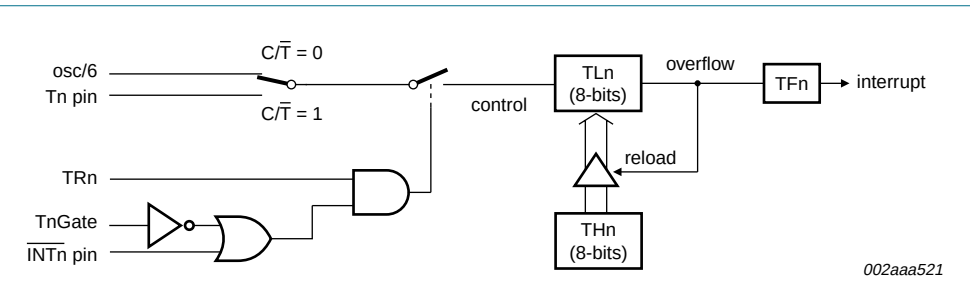


Fig 12. Timer/Counter 0 or 1 in Mode 2 (8-bit auto-reload)

6.8.4 Mode 3

When timer 1 is in Mode 3 it is stopped (holds its count). The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 and Timer 0 is shown in Figure 13. TL0 uses the Timer 0 control bits: T0C/$\overline{T}$, T0GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the 'Timer 1' interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in Mode 3, the P89V52X2 can look like it has an additional Timer.

Note: When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

used as the UART transmit baud rate generator. RCLK has the same effect for the UART receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – Timer 1 or Timer 2.

Figure 17 shows Timer 2 in baud rate generator mode:

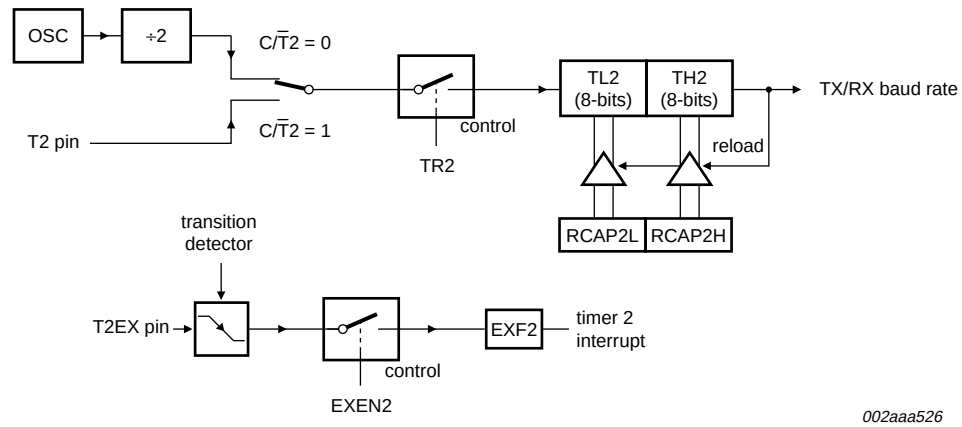


Fig 17. Timer 2 in Baud Rate Generator mode

The baud rate generation mode is like the auto-reload mode, when a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

Modes 1 and 3 Baud Rates = Timer 2 Overflow Rate/16

The timer can be configured for either 'timer' or 'counter' operation. In many applications, it is configured for 'timer' operation (C/$\overline{T}$2 = 0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., $\frac{1}{6}$ the oscillator frequency). As a baud rate generator, it increments at the oscillator frequency. Thus the baud rate formula is as follows:

Modes 1 and 3 Baud Rates =

$$\frac{OscillatorFrequency}{(16 \times (65536 - (RCAP2H, RCAP2L)))} \quad (3)$$

Where: (RCAP2H, RCAP2L) = The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

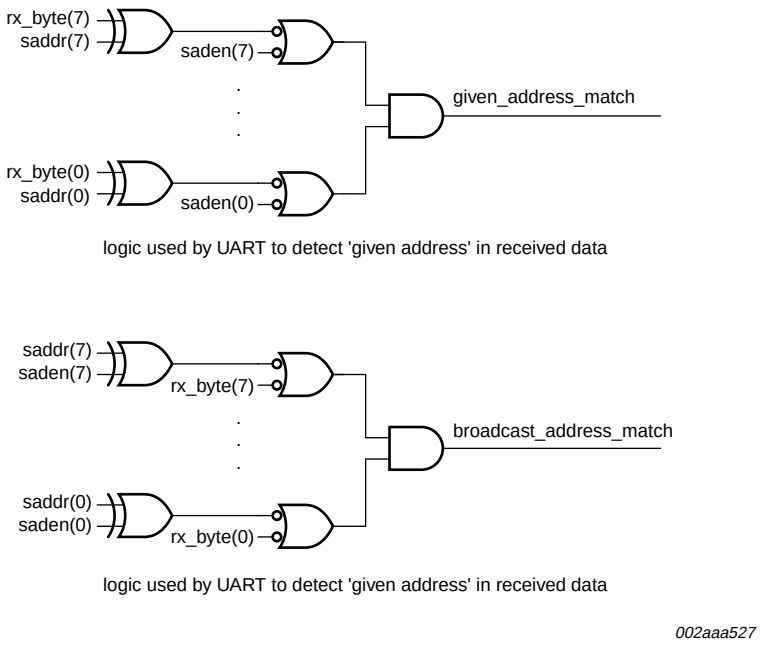


Fig 18. Schemes used by the UART to detect ‘given’ and ‘broadcast’ addresses when multiprocessor communications is enabled

The following examples will help to show the versatility of this scheme.

Example 1, slave 0:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1101} \\ \text{Given} = 1100\ 00\text{X}0 \end{array} \quad (4)$$

Example 2, slave 1:

$$\begin{array}{l} \text{SADDR} = 1100\ 0000 \\ \underline{\text{SADEN} = 1111\ 1110} \\ \text{Given} = 1100\ 000\text{X} \end{array} \quad (5)$$

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a ‘0’ in bit 0 and it ignores bit 1. Slave 1 requires a ‘0’ in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a ‘0’ in bit 1. A unique address for slave 1 would be 1100 0001 since a ‘1’ in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Example 1, slave 0:

SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0 (6)

Example 2, slave 1:

SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X (7)

Example 2, slave 2:

SADDR = 1100 0000
SADEN = 1111 1100
Given = 1100 00XX (8)

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all 'don't cares' as well as a Broadcast address of all 'don't cares'. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

6.11 Interrupt priority and polling sequence

The device supports six interrupt sources under a four level priority scheme. Table 24 summarizes the polling sequence of the supported interrupts. (See Figure 19).

Table 24. Interrupt polling sequence

Description	Interrupt flag	Vector address	Interrupt enable	Interrupt priority	Service priority	Wake-up Power-down
External Interrupt 0	IE0	0003H	EX0	PX0/H	1 (highest)	yes
T0	TF0	000BH	ET0	PT0/H	2	no
External Interrupt 1	IE1	0013H	EX1	PX1/H	3	yes
T1	TF1	001BH	ET1	PT1/H	4	no
UART	TI/RI	0023H	ES0	PS0/H	5	no
T2	TF2, EXF2	003BH	ET2	PT2/H	6	no

Writing either the PROG or EP command to FMCON will start the program or erase-program process and place the CPU in a program-idle state. The CPU will remain in this idle state until the program or erase-program cycle is completed. Interrupts will NOT be serviced until the cycle is completed.

Erase-program or programming of a single byte (or multiple bytes) in the data EEPROM array is accomplished using the following steps:

- Write the LOAD command (00H) to FMCON. The LOAD command will clear all locations in the page register and their corresponding update flags.
- Write the address within the page register to FMADRL. Since the loading the page register uses FMADRL[5:0], and since the erase-program or program command uses FMADRH and FMADRL[7:6], the user can write the byte location within the page register (FMADRL[5:0]) and the code memory page address (FMADRH and FMADRL[7:6]) at this time.
- Write the data to be programmed to FMDATA. This will increment FMADRL pointing to the next byte in the page register.
- Write the address of the next byte to be programmed to FMADRL, if desired. (This is not needed for contiguous bytes since FMADRL is auto-incremented). All bytes to be programmed must be within the same page.
- Write the data for the next byte to be programmed to FMDATA.
- Repeat writing of FMADRL and/or FMDATA until all desired bytes have been loaded into the page register.
- Write the page address mapped into user code memory to FMADRH and FMADRL[7:6], if not previously included when writing the page register address to FMADRL[5:0].
- Write the EP (68H) or PROG (48H) command to FMCON, starting the erase-program or program cycle.
- Read FMCON to check status. If aborted, repeat starting with the LOAD command.

Table 33. Flash Memory Control register (FMCON - address F4H) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol (R)	BUSY	WE	-	DAP	-	-	SV	ERR
Symbol (W)	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0
Reset	0	0	0	0	0	0	0	0

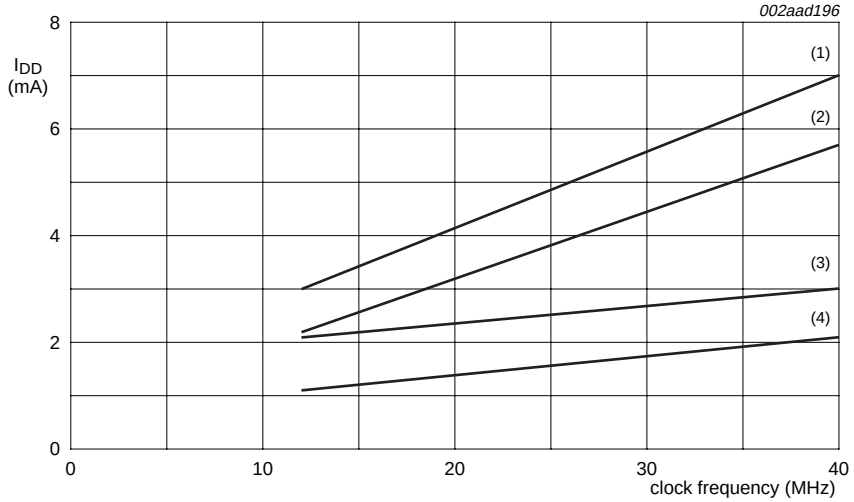
Table 34. Flash Memory Control register (FMCON - address E4H) bit description

Bit	Symbol	Access	Description
0	ERR	R	Set when either of the following conditions occur: • Device was reset before the operation was completed. • Attempt made to access data EEPROM while Data Access Protect (DAP) is set. • An error occurs in the device's internal high voltage circuits.
	FMCMD.0	W	Command byte bit 0.
1	SV	R	Security violation. Set when an attempt is made to program, erase, or CRC a secured page. The specific cause of the security violation depends on the operation: • **PROG or EP**: CSEC.0 = 1 or DPxSEC.1 = 1 for the page addressed by FMADRH/L. • **ERS_G**: Any DPxSEC.0 = 1. • **ERS_DP**: DPxSEC.2 = 1 for addressed page while in execution mode. • **CRC_DP**: DPxCSEC.0 = 1 and DPxSEC.1 = 0.
	FMCMD.1	W	Command byte bit 1
2	-	R	Reserved
	FMCMD.2	W	Command byte bit 2.
3	-	R	Reserved
	FMCMD.3	W	Command byte bit 3.
4	DAP	R	Data Access Protect. When set, access to the data EEPROM is unmapped and thus prohibited. Set by the MAP command. Cleared by the UNMAP command.
	FMCMD.4	W	Command byte bit 4.
5	-	R	Reserved
	FMCMD.5	W	Command byte bit 5.
6	WE	R	When set, indicates that data EEPROM writes during program execution are enabled.
	FMCMD.6	W	Command byte bit 6.
7	BUSY	R	Indicates that a program, erase, CRC calculation or similar operation is in progress. Note that this bit is usable only in ICP mode since the CPU is stalled whenever this bit is set in execution mode.
	FMCMD.7	W	Command byte bit 7.

An assembly language routine to load the page register and perform an erase/program operation is shown below. This code assumes the data EEPROM has been mapped into user code space.

```
;*************************************************
;*    pgm user code          *
;*************************************************
;*
;                                                *

;* Inputs:                                                    *
;*R3 = number of bytes to program (byte)          *
;*R4 = page address MSB(byte)                     *
;*R5 = page address LSB(byte)                     *
;*R7 = pointer to data buffer in RAM(byte)        *
;* Outputs:                                                   *
;*R7 = status (byte)                                 *
;* C = clear on no error, set on error            *
;*************************************************
```



(1) Maximum $I_{DD(oper)}$

(2) Typical $I_{DD(oper)}$

(3) Maximum $I_{DD(idle)}$

(4) Typical $I_{DD(idle)}$

Fig 20. I_{DD} vs. frequency

9.1 Explanation of symbols

Each timing symbol has 5 characters. The first character is always a 't' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A — Address

C — Clock

D — Input data

H — Logic level HIGH

I — Instruction (program memory contents)

L — Logic level LOW or ALE

P — $\overline{\text{PSEN}}$

Q — Output data

R — $\overline{\text{RD}}$ signal

T — Time

V — Valid

W — $\overline{\text{WR}}$ signal

X — No longer a valid logic level

Z — High impedance (Float)

Example:

t_{AVLL} = Address valid to ALE LOW time

t_{LLPL} = ALE LOW to $\overline{\text{PSEN}}$ LOW time

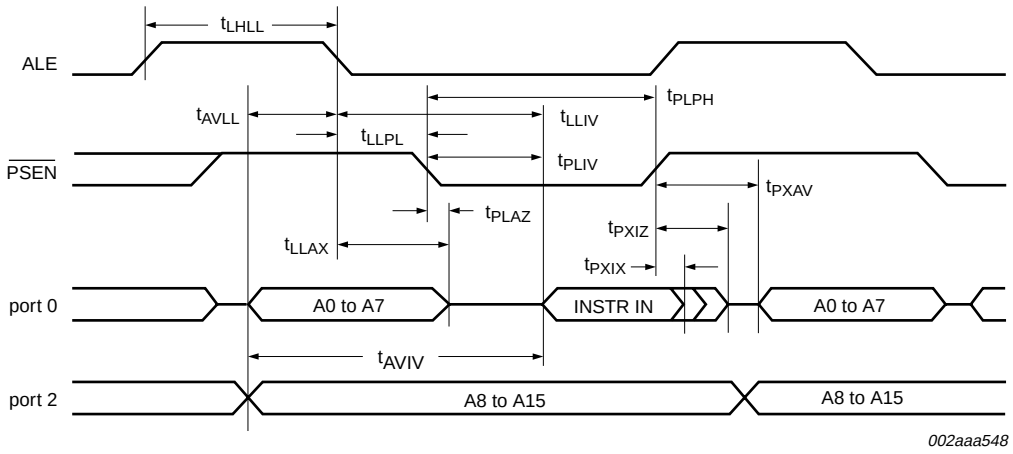


Fig 21. External program memory read cycle

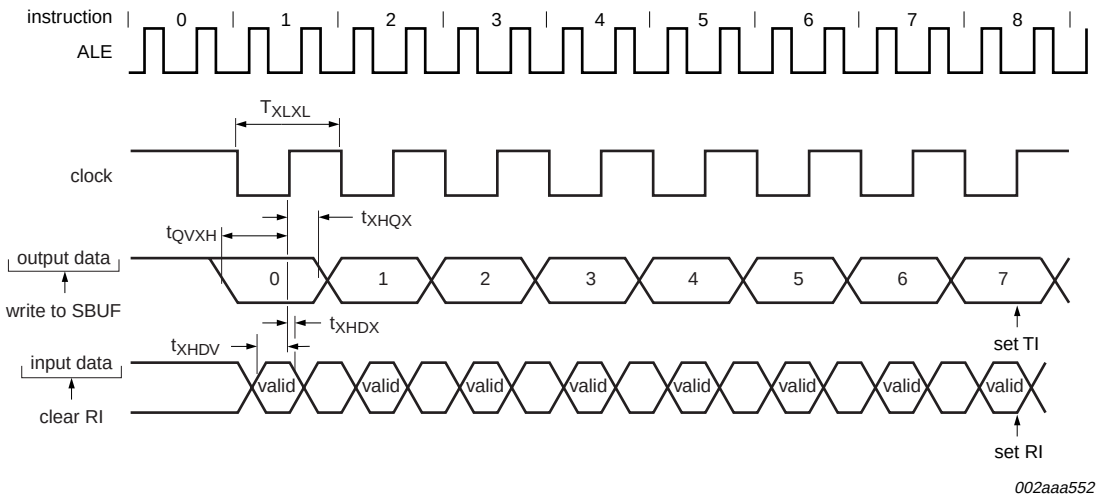


Fig 25. Shift register mode timing waveforms

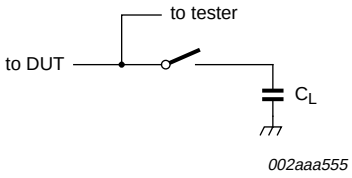
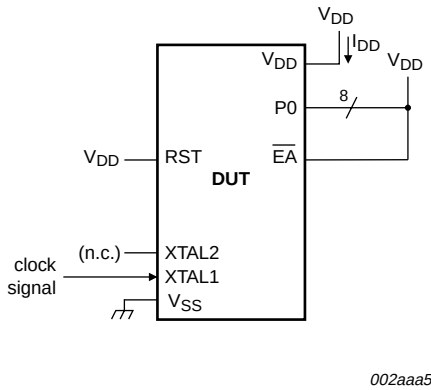
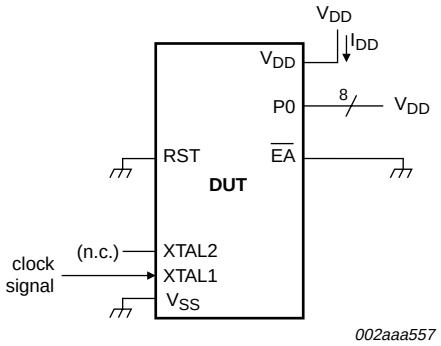


Fig 26. Test load example



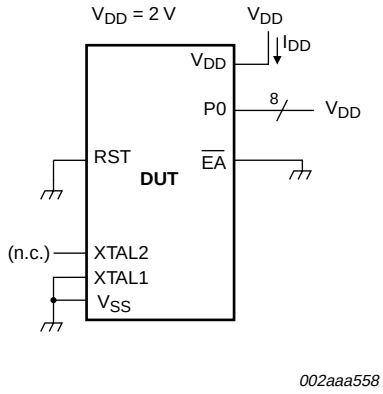
All other pins disconnected

Fig 27. I_{DD} test condition, active mode



All other pins disconnected

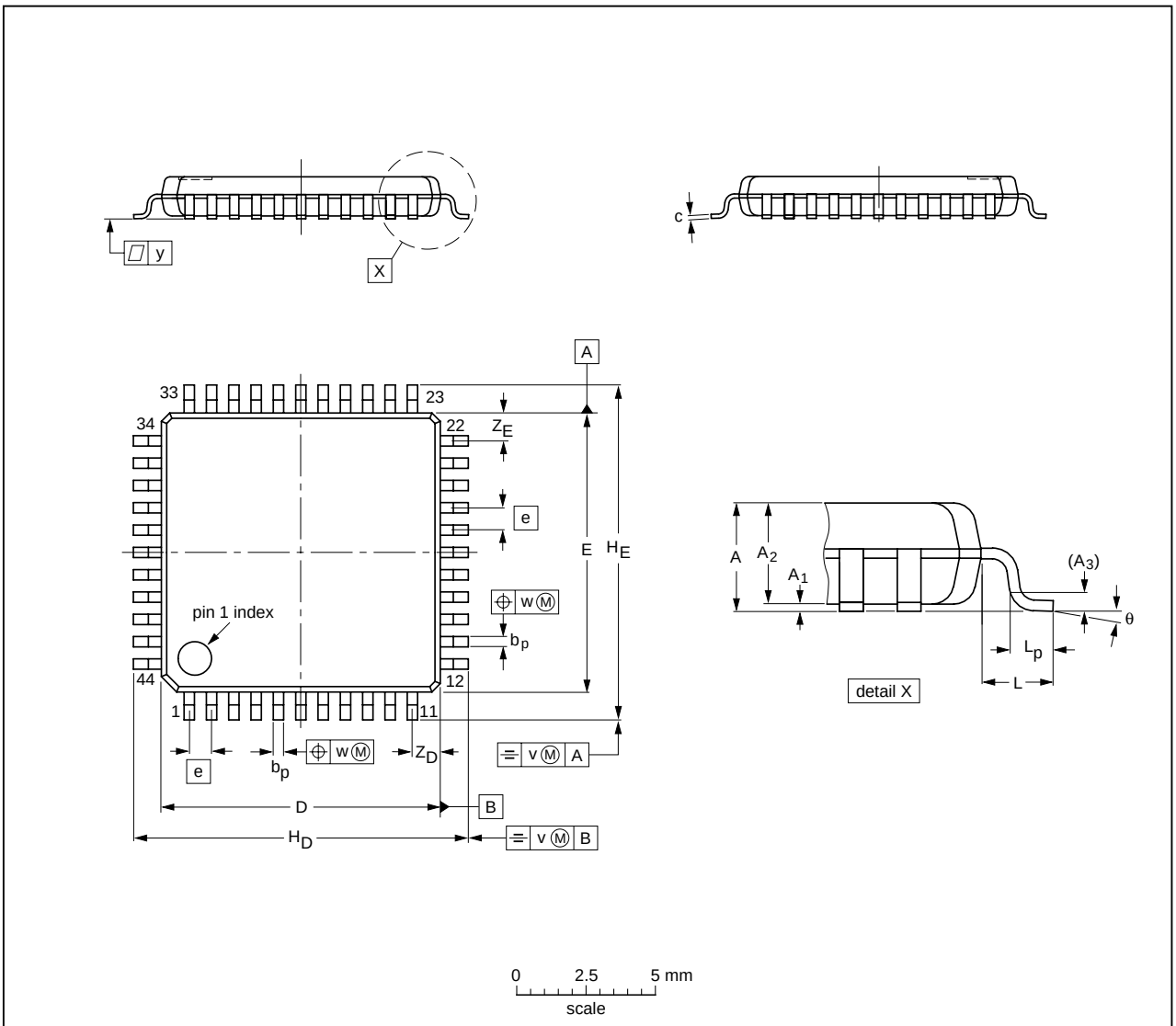
Fig 28. I_{DD} test condition, Idle mode



All other pins disconnected

Fig 29. I_{DD} test condition, Power-down mode

LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.14 0.85	1.14 0.85	7^o 0^o

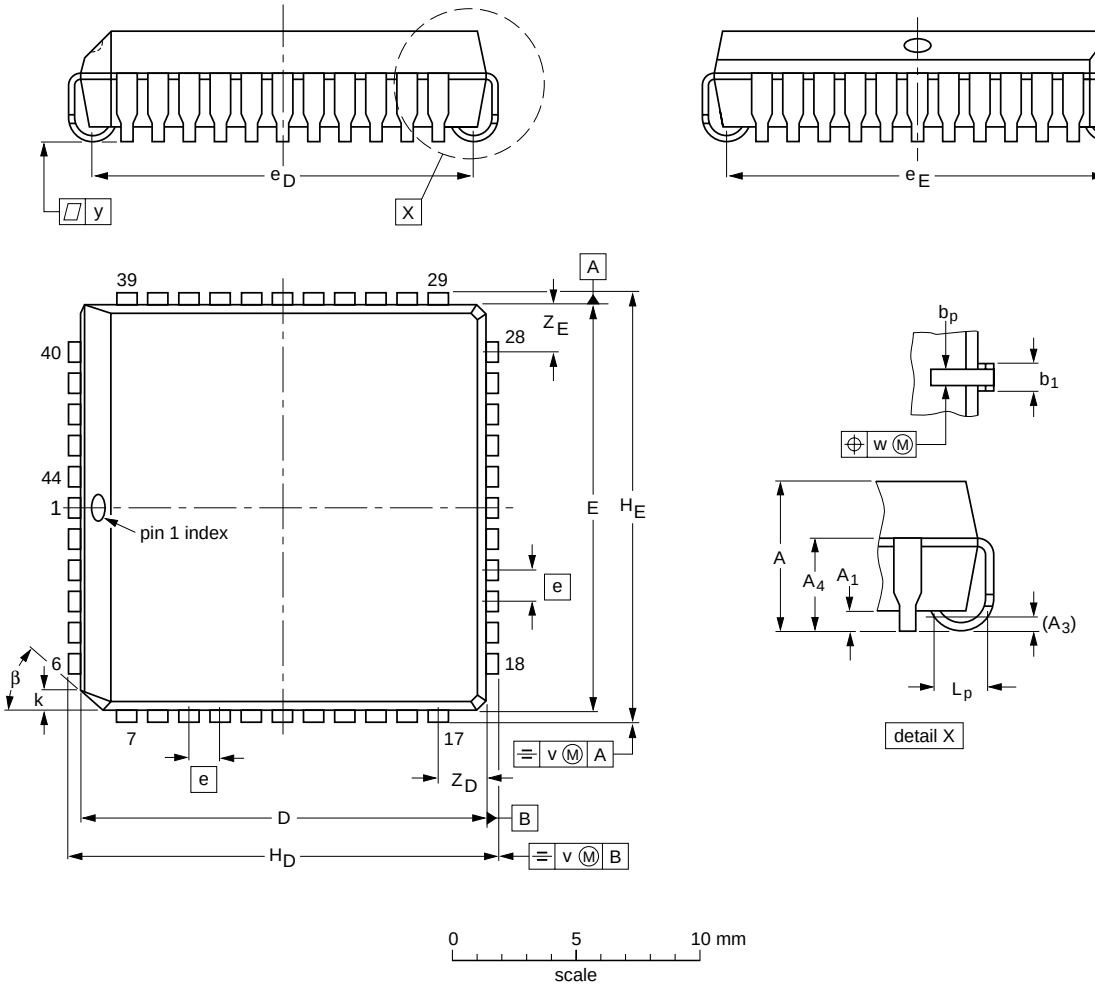
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT389-1	136E08	MS-026				~~00-01-19~~ 02-06-07

Fig 31. Package outline SOT389-1 (LQFP44)

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 32. Package outline SOT187-2 (PLCC44)

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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