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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78i052ddg

1 GENERAL DESCRIPTION

The W78I054D/W78I052D/W78I051D series is an 8-bit microcontroller which can accommodate a wider frequency range with low power consumption. The instruction set for the W78I054D/ W78I052D/ W78I051D series is fully compatible with the standard 8052.

The W78I054D/W78I052D/W78I051D series contains 16K/8K/4K bytes Flash EPROM programmable by hardware writer; a 256 bytes RAM; four 8-bit bi-directional (P0, P1, P2, P3) and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by 8 sources 4-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78I054D/W78I052D/W78I051D series allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78I054D/W78I052D/W78I051D series microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor. The W78I054D/W78I052D/W78I051D series contains In-System Programmable (ISP) 2KB LD Flash EPROM for loader program, operating voltage from 3.3V to 5.5V.

The W78I054D/W78I052D/W78I051D series feature industrial temperature rage (-40 degrees Celsius to +85 degrees Celsius).

8 MEMORY ORGANIZATION

The W78I054D/W78I052D/W78I051D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

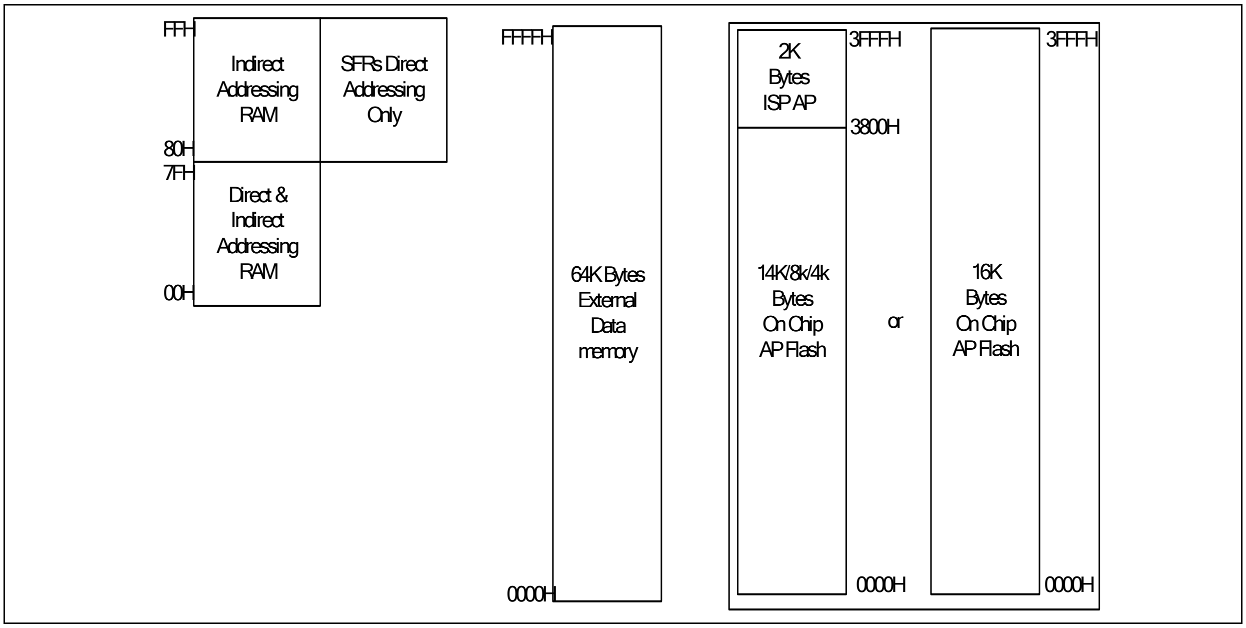


Figure 8- 1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78I054D/W78I052D/W78I051D series can be up to 16K/8K/4K bytes (2K bytes for ISP F/W, share with the W78E054D) long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78I054D/W78I052D/W78I051D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

Address								
FFH – 80H	Indirect RAM							
7FH – 30H	Direct RAM							
2FH	7F	7E	7D	7C	7B	7A	79	78
2EH	77	76	75	74	73	72	71	70
2DH	6F	6E	6D	6C	6B	6A	69	68
2CH	67	66	65	64	63	62	61	60
2BH	5F	5E	5D	5C	5B	5A	59	58
2AH	57	56	55	54	53	52	51	50
29H	4F	4E	4D	4C	4B	4A	49	48
28H	47	46	45	44	43	42	41	40
27H	3F	3E	3D	3C	3B	3A	39	38
26H	37	36	35	34	33	32	31	30
25H	2F	2E	2D	2C	2B	2A	29	28
24H	27	26	25	24	23	22	21	20
23H	1F	1E	1D	1C	1B	1A	19	18
22H	17	16	15	14	13	12	11	10
21H	0F	0E	0D	0C	0B	0A	09	08
20H	07	06	05	04	03	02	01	00
1FH – 18H	Bank 3							
17H – 10H	Bank 2							
0FH – 08H	Bank 1							
07H – 00H	Bank 0							

Figure 8- 3 Scratch-pad RAM

8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78I054D/W78I052D/W78I051D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

-	-	-	-	-	-	-	P0UP

Mnemonic: P0UPR Address: 86h

BIT	NAME	FUNCTION
0	P0UP	0: Port 0 pins are open-drain. 1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.
6	SMOD 0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	-	Reserved
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.

SWRST	-	-	-	-	-	FBOOTSL	ENP

Mnemonic: CHPCON Address: BFh

Bit	Name	Function
7	SWRST	When this bit is set to 1, and both FBOOTSL and ENP are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit can determine that the F02KBOOT mode is running. Note: Software Reset only LDROM jump to APROM, APROM can't software reset to LDROM.
1	FBOOTSL	The Loader Program Location Select. 0: The Loader Program locates at the APROM flash memory bank. 1: The Loader Program locates at the LD flash memory bank.
0	ENP	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. In this mode, erase, program and read operations are achieved. 0: Disable in-system programming mode. The on-chip flash memory is read-only.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	External interrupt 3 priority is higher if set this bit to 1
6	EX3	Enable External interrupt 3 if set this bit to 1
5	IE3	If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced
4	IT3	External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software
3	PX2	External interrupt 2 priority is higher if set this to 1
2	EX2	Enable External interrupt 2 if set this bit to 1
1	IE2	If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced
0	IT2	External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

SFR program of address low

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

BIT	NAME	FUNCTION
7-0	TH2.[7:0]	Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8^{th} bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: D8h

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$, $\overline{INT3}$).

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

Bit	Name	Function

10 INSTRUCTION

The W78I054D/W78I052D/W78I051D series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly the same.

Op-code	HEX Code	Bytes	W78I054D/W78I052D/W78I051D series Clock cycles
NOP	00	1	12
ADD A, R0	28	1	12
ADD A, R1	29	1	12
ADD A, R2	2A	1	12
ADD A, R3	2B	1	12
ADD A, R4	2C	1	12
ADD A, R5	2D	1	12
ADD A, R6	2E	1	12
ADD A, R7	2F	1	12
ADD A, @R0	26	1	12
ADD A, @R1	27	1	12
ADD A, direct	25	2	12
ADD A, #data	24	2	12
ADDC A, R0	38	1	12
ADDC A, R1	39	1	12
ADDC A, R2	3A	1	12
ADDC A, R3	3B	1	12
ADDC A, R4	3C	1	12
ADDC A, R5	3D	1	12
ADDC A, R6	3E	1	12
ADDC A, R7	3F	1	12
ADDC A, @R0	36	1	12
ADDC A, @R1	37	1	12
ADDC A, direct	35	2	12
ADDC A, #data	34	2	12
SUBB A, R0	98	1	12
SUBB A, R1	99	1	12
SUBB A, R2	9A	1	12

Op-code	HEX Code	Bytes	W78I054D/W78I052D/W78I051D series Clock cycles
ORL direct, #data	43	3	24
XRL A, R0	68	1	12
XRL A, R1	69	1	12
XRL A, R2	6A	1	12
XRL A, R3	6B	1	12
XRL A, R4	6C	1	12
XRL A, R5	6D	1	12
XRL A, R6	6E	1	12
XRL A, R7	6F	1	12
XRL A, @R0	66	1	12
XRL A, @R1	67	1	12
XRL A, direct	65	2	12
XRL A, #data	64	2	12
XRL direct, A	62	2	12
XRL direct, #data	63	3	24
CLR A	E4	1	12
CPL A	F4	1	12
RL A	23	1	12
RLC A	33	1	12
RR A	03	1	12
RRC A	13	1	12
SWAP A	C4	1	12
MOV A, R0	E8	1	12
MOV A, R1	E9	1	12
MOV A, R2	EA	1	12
MOV A, R3	EB	1	12
MOV A, R4	EC	1	12
MOV A, R5	ED	1	12
MOV A, R6	EE	1	12
MOV A, R7	EF	1	12
MOV A, @R0	E6	1	12
MOV A, @R1	E7	1	12

Op-code	HEX Code	Bytes	W78I054D/W78I052D/W78I051D series Clock cycles
MOV direct, A	F5	2	12
MOV direct, R0	88	2	24
MOV direct, R1	89	2	24
MOV direct, R2	8A	2	24
MOV direct, R3	8B	2	24
MOV direct, R4	8C	2	24
MOV direct, R5	8D	2	24
MOV direct, R6	8E	2	24
MOV direct, R7	8F	2	24
MOV direct, @R0	86	2	24
MOV direct, @R1	87	2	24
MOV direct, direct	85	3	24
MOV direct, #data	75	3	24
MOV DPTR, #data 16	90	3	24
MOVC A, @A+DPTR	93	1	24
MOVC A, @A+PC	83	1	24
MOVX A, @R0	E2	1	24
MOVX A, @R1	E3	1	24
MOVX A, @DPTR	E0	1	24
MOVX @R0, A	F2	1	24
MOVX @R1, A	F3	1	24
MOVX @DPTR, A	F0	1	24
PUSH direct	C0	2	24
POP direct	D0	2	24
XCH A, R0	C8	1	12
XCH A, R1	C9	1	12
XCH A, R2	CA	1	12
XCH A, R3	CB	1	12
XCH A, R4	CC	1	12
XCH A, R5	CD	1	12
XCH A, R6	CE	1	12
XCH A, R7	CF	1	12

Op-code	HEX Code	Bytes	W78I054D/W78I052D/W78I051D series Clock cycles
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12
CPL bit	B2	2	12
ANL C, bit	82	2	24
ANL C, /bit	B0	2	24
ORL C, bit	72	2	24
ORL C, /bit	A0	2	24
MOV C, bit	A2	2	12
MOV bit, C	92	2	24
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	24
LCALL addr16	12	3	24
RET	22	1	24
RETI	32	1	24
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	24
LJMP addr16	02	3	24
JMP @A+DPTR	73	1	24
SJMP rel	80	2	24
JZ rel	60	2	24
JNZ rel	70	2	24
JC rel	40	2	24
JNC rel	50	2	24

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH	IP/ XICON.7/ XICON.3	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being executed.
3. The current instruction does not involve a write to IE, IP, IPH, XICON registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on the below table. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what is was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

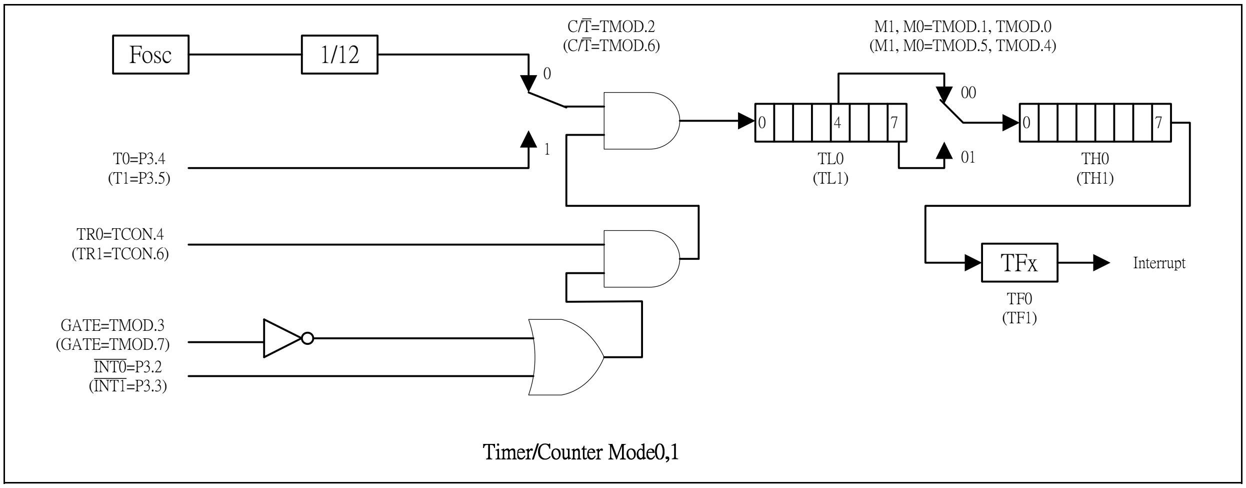


Figure 14- 1 Timer/Counters 0 & 1 in Mode 0,1

14.2.3 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as an 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{\text{INTx}}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of clock/12 or pulses on pin Tn.

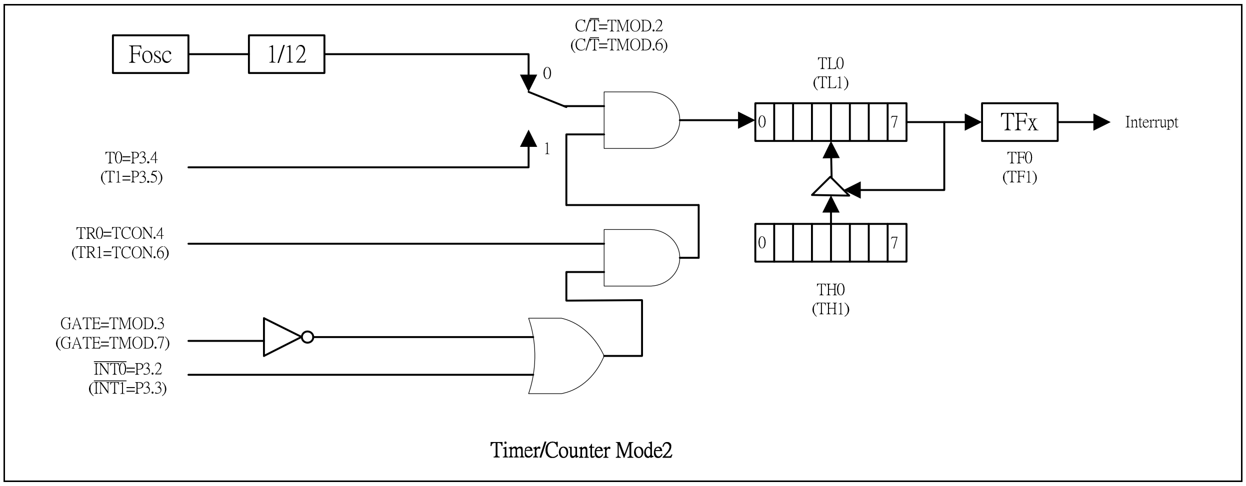


Figure 14- 2 Timer/Counter 0 & 1 in Mode 2

14.2.4 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0

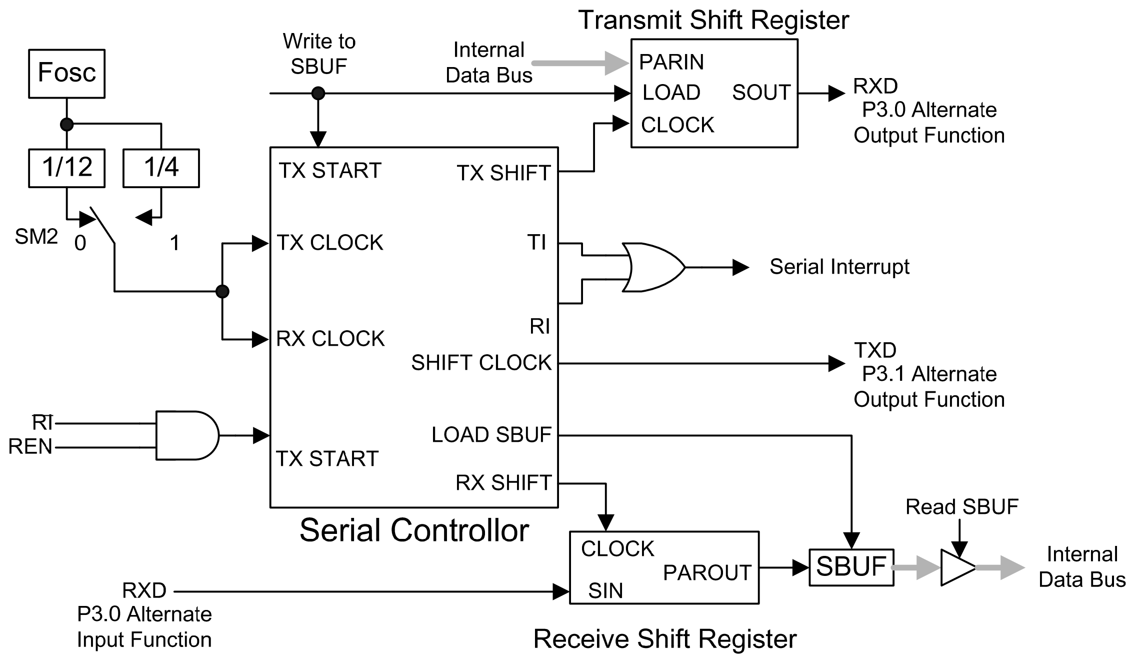


Figure 16- 1 Serial port mode 0

The TI flag is set high in S6P2 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in S6P2 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counters after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters.

grammable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counters after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

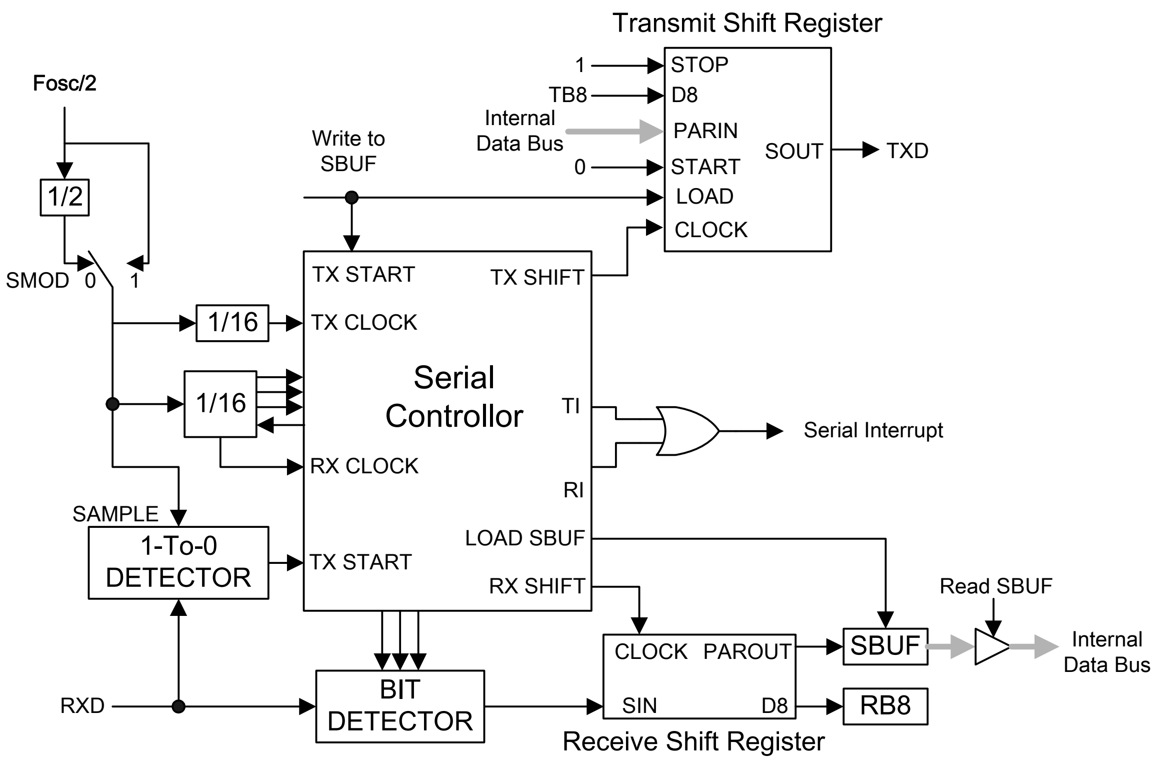
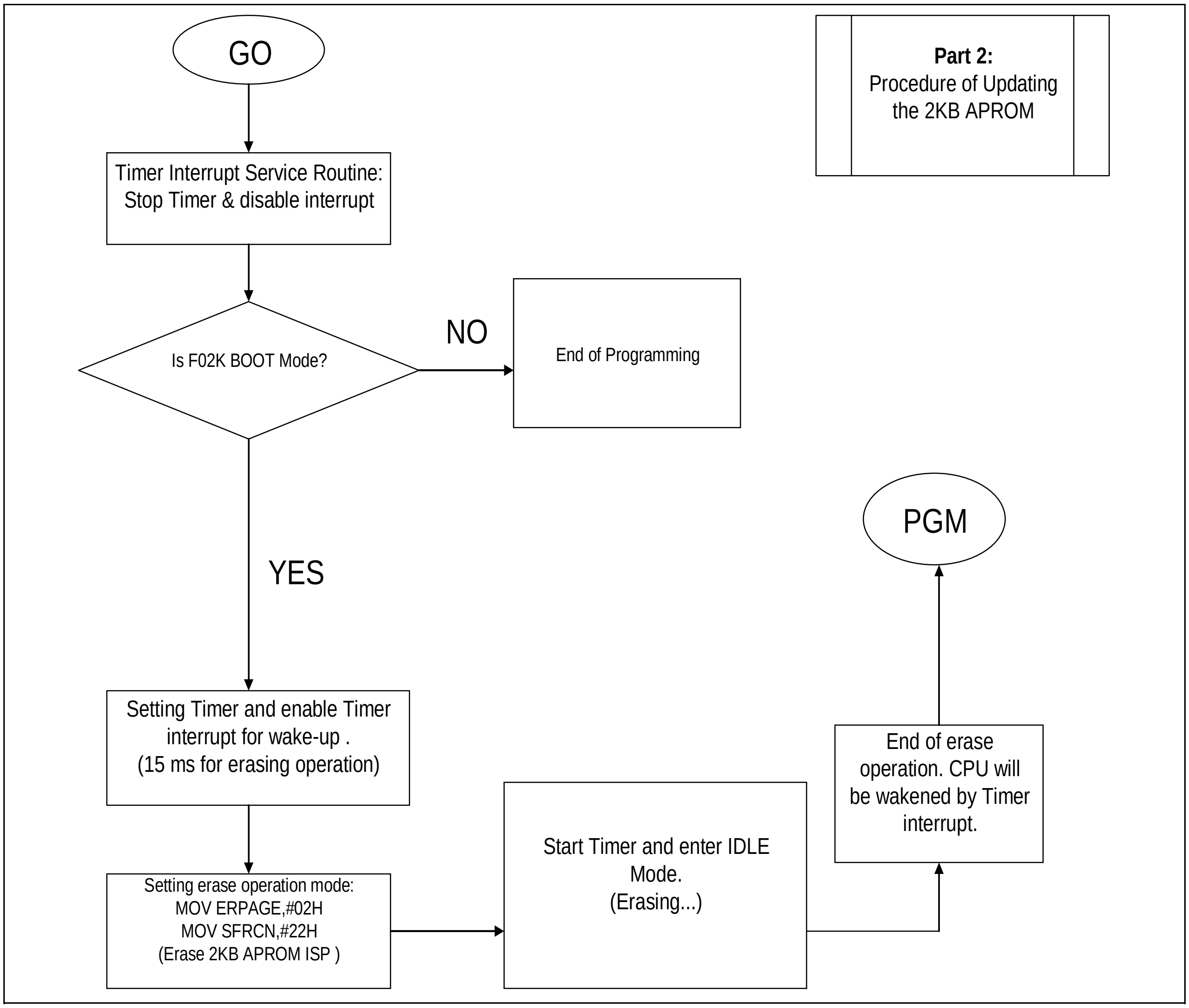


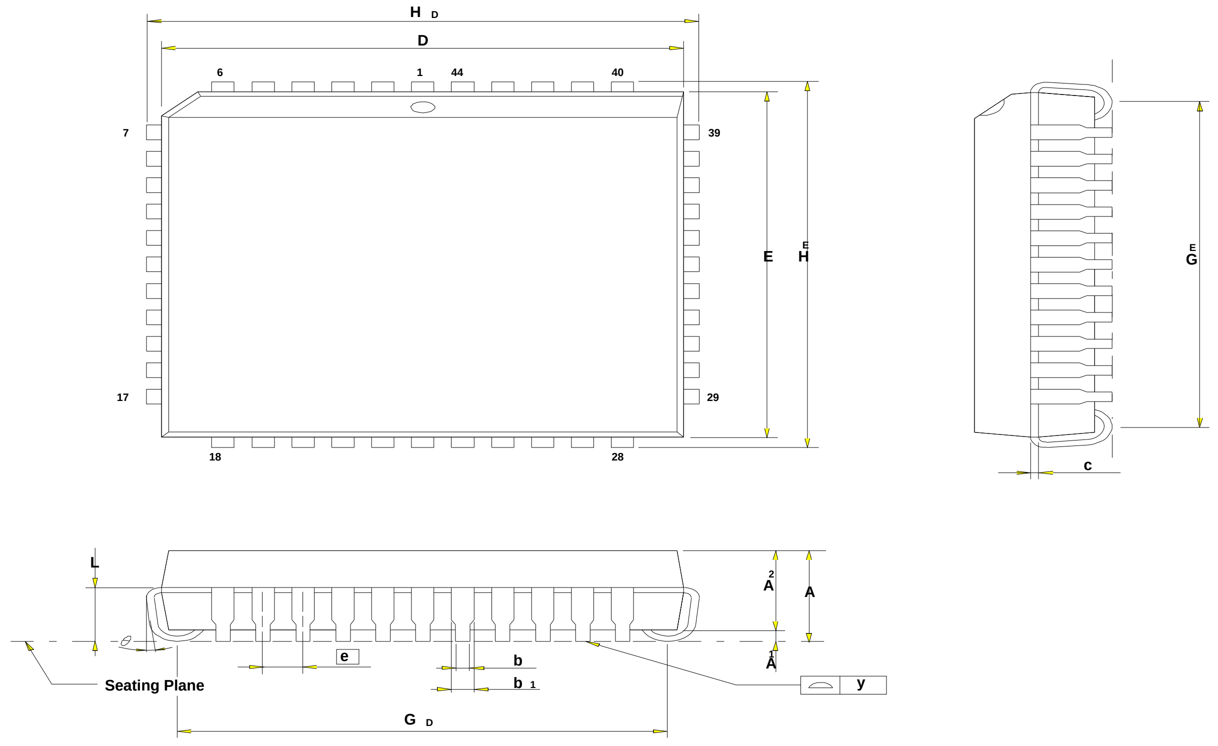
Figure 16- 3 Serial port mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

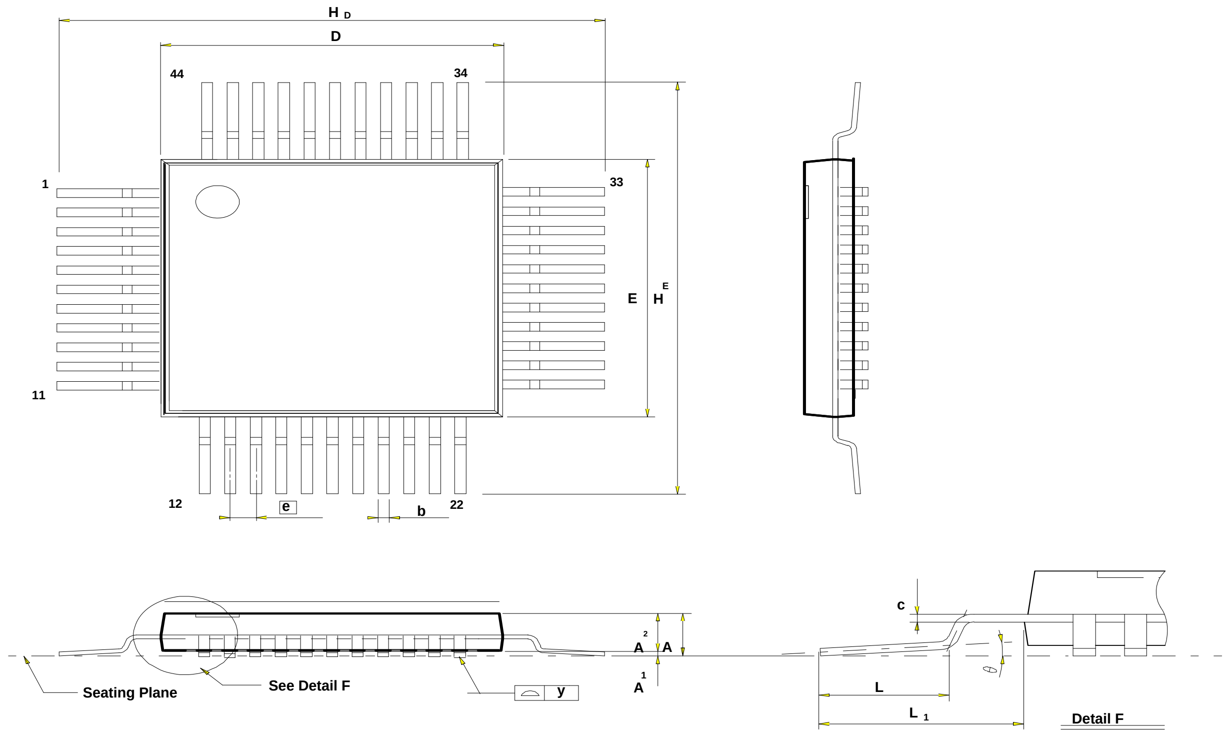

Part 2:
Procedure of Updating the 2KB APROM
GO
Timer Interrupt Service Routine: Stop Timer & disable interrupt
Is F02K BOOT Mode?
NO
End of Programming
YES
Setting Timer and enable Timer interrupt for wake-up . (15 ms for erasing operation)
Setting erase operation mode: MOV ERPAGE,#02H MOV SFRCN,#22H (Erase 2KB APROM ISP)
Start Timer and enter IDLE Mode. (Erasing...)
End of erase operation. CPU will be wakened by Timer interrupt.
PGM

22.2 44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	——	——	0.185	——	——	4.70
A_1	0.020	——	——	0.51	——	——
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	——	——	0.004	——	——	0.10

22.3 44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	-	—	—	-
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	—	.0315	—	—	0.80	—
H_D	0.510	0.520	0.530	12.95	13.20	13.45
H_E	0.510	0.520	0.530	12.95	13.20	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	—	0.063	—	—	1.60	—
y	—	—	0.004	—	—	0.10
θ	0 °	—	10 °	0 °	—	10 °

```
    cpl     A
    mov     B,A
    inc     DPTR
    mov     R0,DPL
    cjne    R0,#LOW (APROM_END_ADDRESS),rd_lp
    mov     R1,DPH
    cjne    R1,#HIGH(APROM_END_ADDRESS),rd_lp
    ret
Program_Fail:
    mov     P1,#03h
    sjmp    $
;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU TO APROM
;*****************************************************************************
Software_Reset:
    MOV     CHPCON,#081h    ;CHPCON=081h, SOFTWARE RESET to APROM.
;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU TO LDROM
;*****************************************************************************
    ;MOV CHPCON,#083h    ;CHPCON=083h, SOFTWARE RESET to LDROM.

    sjmp    $

    end
```

23 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	August 14, 2008	-	Initial Issued
A02	November 3,2008	-	Update DC table typing error.
A03	December 15,2008	-	Update config bit table, and ISP BOOT
A04	January 7,2007	70	Update V_{IL} and V_{IH} .
A05	March 9, 2009	43	Update soft reset, only LD jump to AP function.
A06	March 20, 2009	18 - -	1. Rename SFR Register POR (0x86H) to P0UPR. 2. Revise some typing errors in data sheet. 3. Update DC table
A07	April 22, 2009	68	1. Revise Type Application Circuit in data sheet.
A08	June 30, 2009	30 61 81	1. Add the ISP control table. 2. Revise content of Char. 17. 3. Modify the ISP demo code. 4. Remove the “Preliminary” character for each page.
A09	Dec 30, 2009	68 77	1. Revise the “CONFIG BITS” description for Bit4, Bit6 and Bit7. 2. Add the timing for external reset pin.