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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78i052dfg

7 FUNCTIONAL DESCRIPTION

The W78I054D/W78I052D/W78I051D series architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 16K/8K/4K flash EPROM, 2K FLASH EPROM for ISP function, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different op-codes and references both a 64K program address space and a 64K data storage space.

7.1 On-Chip Flash EPROM

The W78I054D/W78I052D/W78I051D series include one 16K/8K/4K bytes of main Flash EPROM for application program.

7.2 I/O Ports

The W78I054D/W78I052D/W78I051D series has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port1 and 3 act as I/O ports with alternate functions. Port 4 is only available on PLCC/PQFP/LQFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

7.3 Serial I/O

The W78I054D/W78I052D/W78I051D series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on the W78I054D/ W78I052D/ W78I051D series can operate in different modes in order to obtain timing similarity as well.

7.4 Timers

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the 8051 CPU. Timer 2 is a special feature of the W78I054D/W78I052D/W78I051D: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

7.5 Interrupts

The Interrupt structure in the W78I054D/W78I052D/W78I051D is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W78I054D/W78I052D/W78I051D provides 8 interrupt resources with four priority level, including four external interrupt sources, three timer interrupts, serial I/O interrupts.

8 MEMORY ORGANIZATION

The W78I054D/W78I052D/W78I051D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

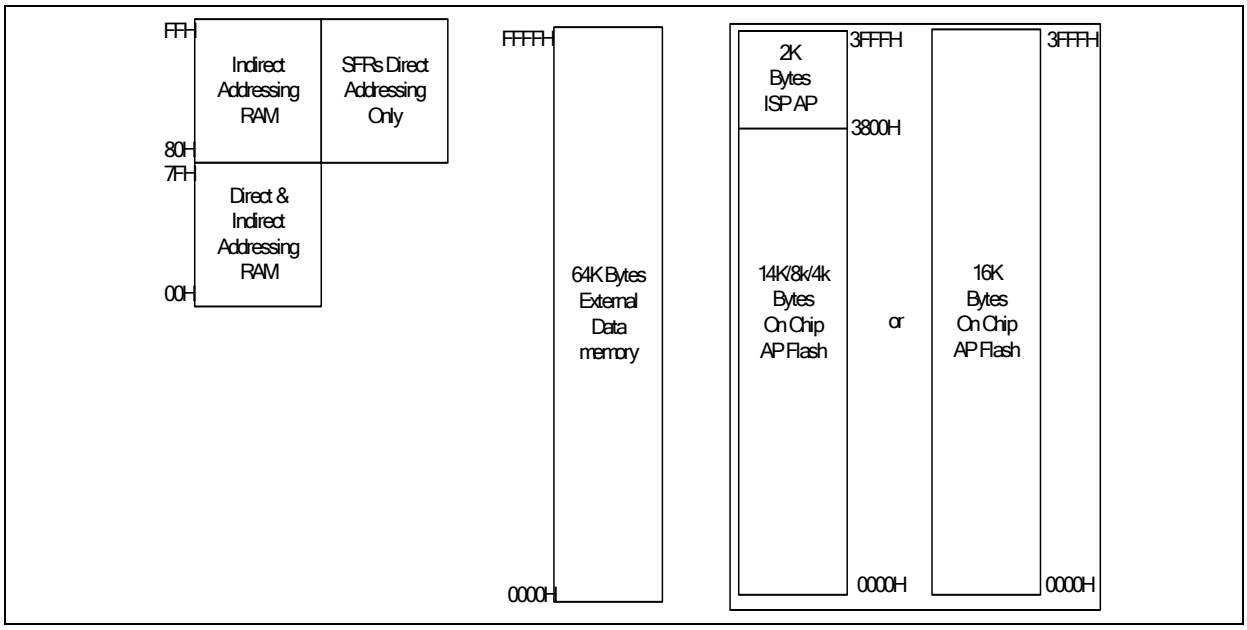


Figure 8- 1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78I054D/W78I052D/W78I051D series can be up to 16K/8K/4K bytes (2K bytes for ISP F/W, share with the W78E054D) long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78I054D/W78I052D/W78I051D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

Special Function Registers:

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
P4	Port 4	D8H					INT2	INT3			0000 1111B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B
TH2	T2 reg. high	CDH									0000 0000B
TL2	T2 reg. low	CCH									0000 0000B
RCAP2H	T2 capture low	CBH									0000 0000B
RCAP2L	T2 capture high	CAH									0000 0000B
T2MOD	Timer 2 Mode	C9								DCEN	0000 0000B
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
SFRCN	SFR program of control	C7H			NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	0000 0000B
SFRRD	SFR program of data register	C6H									0000 0000B
SFRAH	SFR program of address high byte	C5H									0000 0000B
SFRAL	SFR program of address low byte	C4H									0000 0000B
XICON	External interrupt control	C0H	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2	0000 0000B
CHPCON	Chip control	BFH	SWRST	-		-	-	-	FBOOTSL	ENP	0000 0000B
EAPAGE	Erase page operation modes	BEH							EAPG1	EAPG0	0000 0000B
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	1100 0000B
IPH	Interrupt priority High	B7H									0000 0000B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0100 0000B
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111B
SBUF	Serial buffer	99H									0000 0000B
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91) T2EX	(90) T2	1111 1111B
WDTC	Watchdog control	8FH	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0	0000 0000B
AUXR	Auxiliary	8EH	-	-	-	-				ALEOFF	0000 0110B
TH1	Timer high 1	8DH									0000 0000B
TH0	Timer high 0	8CH									0000 0000B
TL1	Timer low 1	8BH									0000 0000B
TL0	Timer low 0	8AH									0000 0000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power control	87H	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL	0011 0000B
P0UPR	Port 0 pull up option Register	86H	-	-	-	-	-	-	-	P0UP	0000 0001B
DPH	Data pointer high	83H									0000 0000B

4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 13-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1)

BIT	NAME	FUNCTION
0	ALE_OFF	1: Disenable ALE output 0: Enable ALE output

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

BIT	NAME	FUNCTION
7	ENW	Enable watch-dog if set.
6	CLRW	Clear watch-dog timer and Pre-scalar if set. This flag will be cleared automatically.
5	WIDL	If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.
2-0	PS2-0	Watch-dog Pre-scalar timer select. Pre-scalar is selected when set PS2–0 as follows:

PS2	PS1	PS0	PRE-SCALAR SELECT
0	0	0	2
0	0	1	8
0	1	0	4
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

BIT	NAME	FUNCTION
7-0	P1.[7:0]	General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read.

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7-0	P2.[7:0]	Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	-	Reserved
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$

6	P3.6	$\overline{WR}$
5	P3.5	T1
4	P3.4	T0
3	P3.3	$\overline{INT1}$
2	P3.2	$\overline{INT0}$
1	P3.1	TX
0	P3.0	RX

Interrupt High Priority

Bit:	7	6	5	4	3	2	1	0
	IPH.7	IPH.6	IPH.5	IPH.4	IPH.3	IPH.2	IPH.1	IPH.0

Mnemonic: IPH Address: B7h

BIT	NAME	FUNCTION
7	IPH.7	1: Interrupt high priority of INT3 is highest priority level.
6	IPH.6	1: Interrupt high priority of INT2 is highest priority level.
5	IPH.5	1: Interrupt high priority of Timer 2 is highest priority level.
4	IPH.4	1: Interrupt high priority of Serial Port 0 is highest priority level.
3	IPH.3	1: Interrupt high priority of Timer 1 is highest priority level.
2	IPH.2	1: Interrupt high priority of External interrupt 1 is highest priority level.
1	IPH.1	1: Interrupt high priority of Timer 0 is highest priority level.
0	IPH.0	1: Interrupt high priority of External interrupt 0 is highest priority level.

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	-	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
5	PT2	1: Interrupt priority of Timer 2 is higher priority level.
4	PS	1: Interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: Interrupt priority of Timer 1 is higher priority level.
2	PX1	1: Interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: Interrupt priority of Timer 0 is higher priority level.
0	PX0	1: Interrupt priority of External interrupt 0 is higher priority level.

BIT	NAME	FUNCTION
7-0	TH2.[7:0]	Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: D8h

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$, $\overline{INT3}$).

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

Bit	Name	Function

Op-code	HEX Code	Bytes	W78I054D/W78I052D/W78I051D series Clock cycles
ORL direct, #data	43	3	24
XRL A, R0	68	1	12
XRL A, R1	69	1	12
XRL A, R2	6A	1	12
XRL A, R3	6B	1	12
XRL A, R4	6C	1	12
XRL A, R5	6D	1	12
XRL A, R6	6E	1	12
XRL A, R7	6F	1	12
XRL A, @R0	66	1	12
XRL A, @R1	67	1	12
XRL A, direct	65	2	12
XRL A, #data	64	2	12
XRL direct, A	62	2	12
XRL direct, #data	63	3	24
CLR A	E4	1	12
CPL A	F4	1	12
RL A	23	1	12
RLC A	33	1	12
RR A	03	1	12
RRC A	13	1	12
SWAP A	C4	1	12
MOV A, R0	E8	1	12
MOV A, R1	E9	1	12
MOV A, R2	EA	1	12
MOV A, R3	EB	1	12
MOV A, R4	EC	1	12
MOV A, R5	ED	1	12
MOV A, R6	EE	1	12
MOV A, R7	EF	1	12
MOV A, @R0	E6	1	12
MOV A, @R1	E7	1	12

Op-code	HEX Code	Bytes	W78I054D/W78I052D/W78I051D series Clock cycles
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12
CPL bit	B2	2	12
ANL C, bit	82	2	24
ANL C, /bit	B0	2	24
ORL C, bit	72	2	24
ORL C, /bit	A0	2	24
MOV C, bit	A2	2	12
MOV bit, C	92	2	24
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	24
LCALL addr16	12	3	24
RET	22	1	24
RETI	32	1	24
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	24
LJMP addr16	02	3	24
JMP @A+DPTR	73	1	24
SJMP rel	80	2	24
JZ rel	60	2	24
JNZ rel	70	2	24
JC rel	40	2	24
JNC rel	50	2	24

13.2 Interrupts

The W78I054D/W78I052D/W78I051D has a 4 priority level interrupt structure with 8 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

13.3 Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON o is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts $\overline{INT2}$ and $\overline{INT3}$. By default, the individual interrupt flag corresponding to external interrupt 2 to 3 must be cleared manually by software.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Serial block can generate interrupts on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR, These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts, at once.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Timer 2 Overflow	002Bh
External Interrupt 2	0033h	External Interrupt 3	003Bh

Table 13- 1 W78I054D/W78I052D/W78I051D interrupt vector table

13.4 Priority Level Structure

There are 4 priority levels for the interrupts high, low. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table.

Each interrupt source can be individually programmed to one of 2 priority levels by setting or clearing bits in the IP registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table below summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and External interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Enable bit	Interrupt Priority	Flag cleared by	Arbitration ranking	Power-down wakeup
External Interrupt 0	IE0	0003H	EX0 (IE.0)	IPH.0, IP.0	Hardware, software	1(highest)	Yes
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	IPH.1, IP.1	Hardware, software	2	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	IPH.2, IP.2	Hardware, software	3	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	IPH.3, IP.3	Hardware, software	4	No
Serial Port	RI + TI	0023H	ES (IE.4)	IPH.4, IP.4	Software	5	No
Timer 2 Over-flow/Match	TF2	002BH	ET2 (IE.5)	IPH.5, IP.5	Software	6	No
External Interrupt 2	IE2	0033H	EX2 (XICON.2)	IPH.6, PX2	Hardware, software	7	Yes
External Interrupt 3	IE3	003BH	EX3 (XICON.6)	IPH.7, PX3	Hardware, software	8(lowest)	Yes

Table 13- 2 Summary of interrupt sources

13.5 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ and $\overline{INT1}$, they are sampled at S5P2 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the

control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

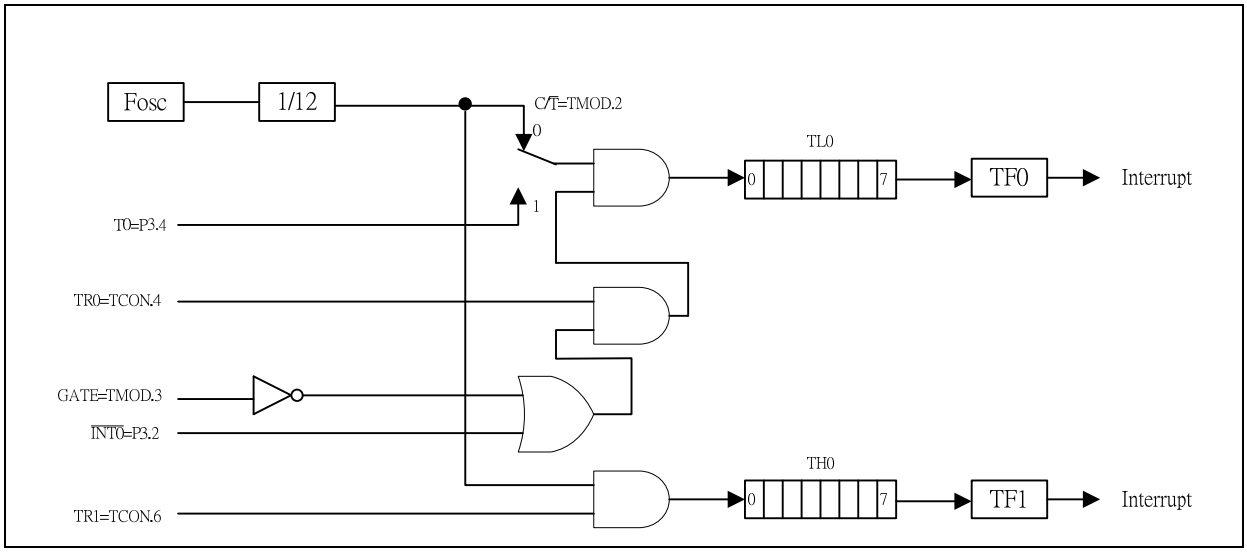


Figure 14- 3 Timer/Counter Mode 3

14.3 Timer/Counter 2

Timer/Counter 2 is a 16 bit up/down counter which is configured by the T2MOD(bit 0) register and controlled by the T2CON register. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/T2 = 1) or the crystal oscillator, which is divided by 12 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

14.3.1 Capture Mode

The capture mode is enabled by setting the $CP/\overline{RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from 0FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will also generate an interrupt.

(RCLK,TCLK, $CP/\overline{RL2}$)= (0,0,1)

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

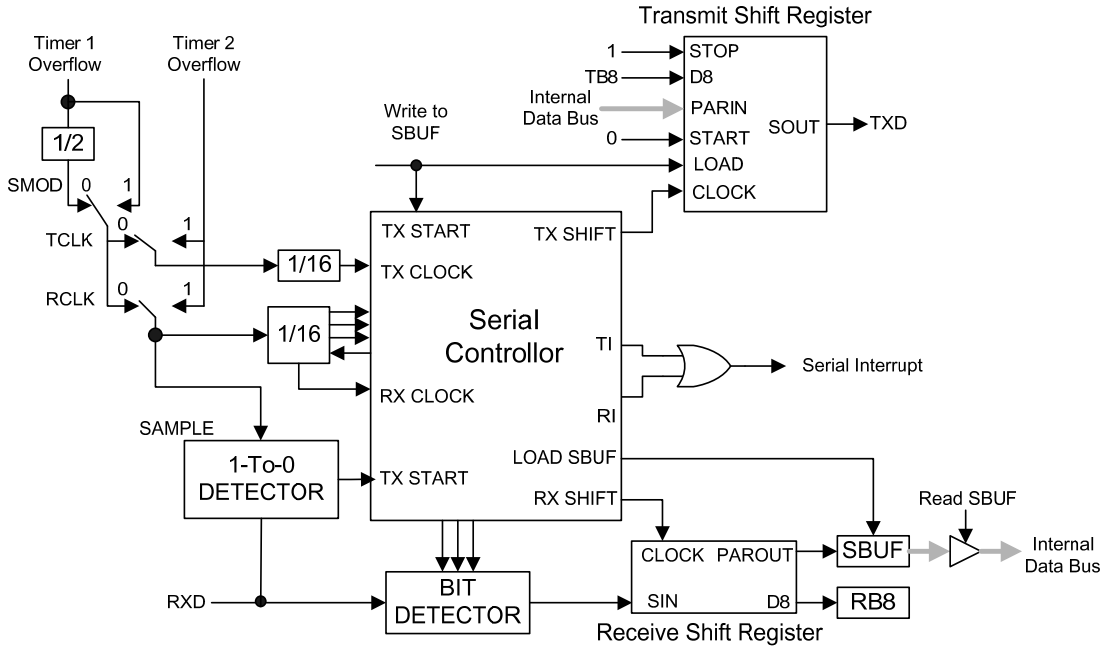
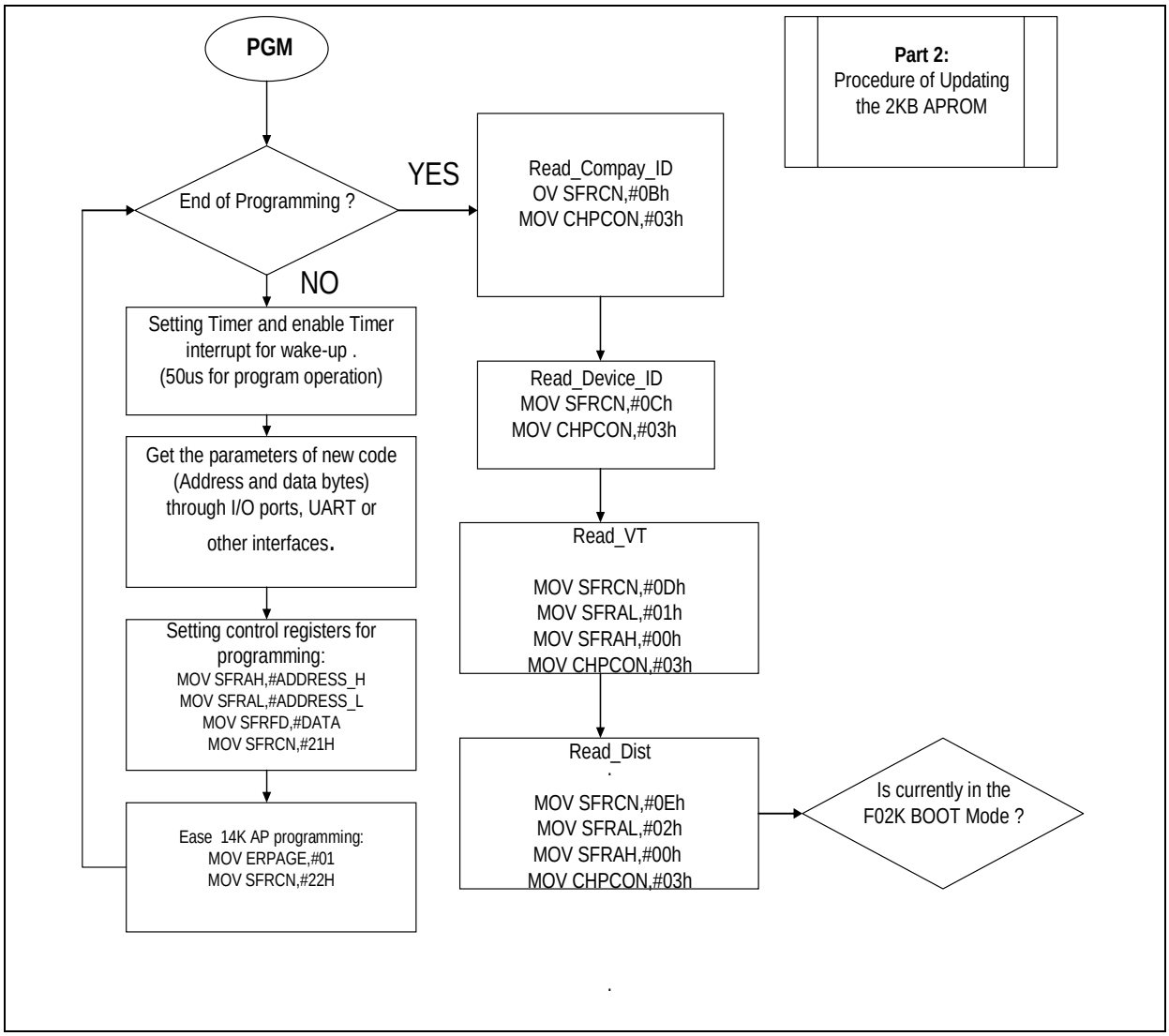


Figure 16- 4 Serial port mode 3

SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit Function
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

Table 17- 1 Serial Ports Modes


PGM
End of Programming ?
YES
NO
Read_Compay_ID
OV SFRCN,#0Bh
MOV CHPCON,#03h
Part 2:
Procedure of Updating
the 2KB APROM
Setting Timer and enable Timer
interrupt for wake-up .
(50us for program operation)
Read_Device_ID
MOV SFRCN,#0Ch
MOV CHPCON,#03h
Get the parameters of new code
(Address and data bytes)
through I/O ports, UART or
other interfaces.
Read_VT
MOV SFRCN,#0Dh
MOV SFRAL,#01h
MOV SFRAH,#00h
MOV CHPCON,#03h
Setting control registers for
programming:
MOV SFRAH,#ADDRESS_H
MOV SFRAL,#ADDRESS_L
MOV SFRFD,#DATA
MOV SFRCN,#21H
Read_Dist
MOV SFRCN,#0Eh
MOV SFRAL,#02h
MOV SFRAH,#00h
MOV CHPCON,#03h
Is currently in the
F02K BOOT Mode ?
Ease 14K AP programming:
MOV ERPAGE,#01
MOV SFRCN,#22H

3. There are no duty cycle requirements on the XTAL1 input.

21.3.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	Taas	1 TCP - Δ	-	-	nS	4
Address Hold from ALE Low	Taah	1 TCP - Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	Tapl	1 TCP - Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	Tpda	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	Tpdh	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	Tpdz	0	-	1 TCP	nS	
ALE Pulse Width	Talw	2 TCP - Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	Tpsw	3 TCP - Δ	3 TCP	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

21.3.3 Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	Tdar	3 TCP -Δ	-	3 TCP +Δ	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	Tdda	-	-	4 TCP	nS	1
Data Hold from $\overline{\text{RD}}$ High	Tddh	0	-	2 TCP	nS	
Data Float from $\overline{\text{RD}}$ High	Tddz	0	-	2 TCP	nS	
$\overline{\text{RD}}$ Pulse Width	Tdrd	6 TCP -Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

21.3.4 Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	Tdaw	3 TCP -Δ	-	3 TCP +Δ	nS
Data Valid to $\overline{WR}$ Low	Tdad	1 TCP -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	Tdwd	1 TCP -Δ	-	-	nS
$\overline{WR}$ Pulse Width	Tdwr	6 TCP -Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

21.3.5 Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	Tpds	1 TCP	-	-	nS
Port Input Hold from ALE Low	Tpdh	0	-	-	nS
Port Output to ALE	Tpda	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to

ALE, since it provides a convenient reference.

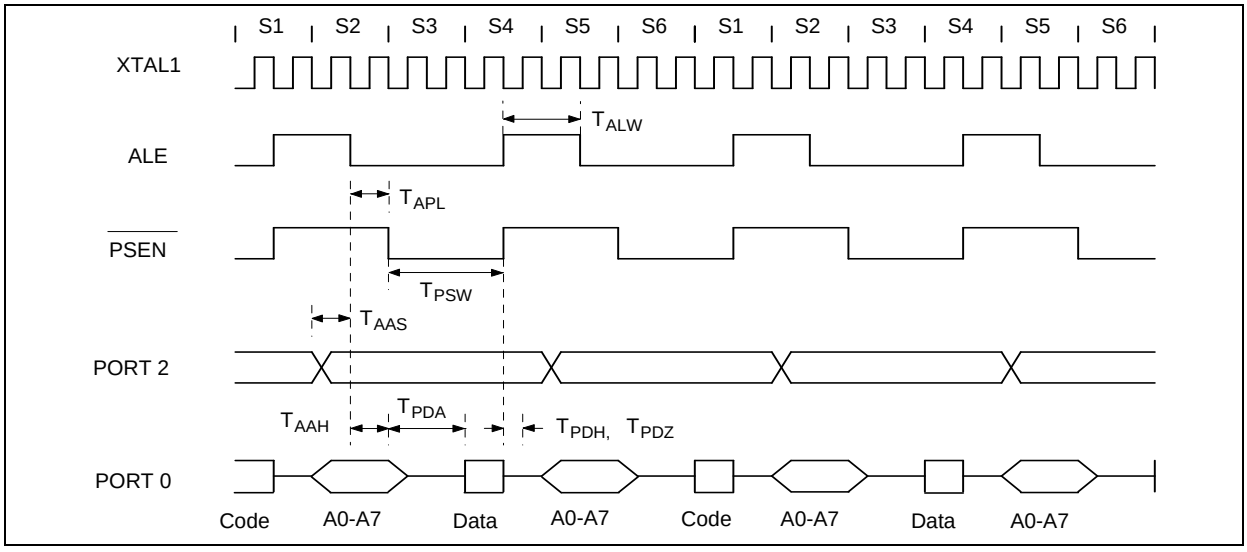
21.3.6 Program Operation

PARAMETER	Symbol	Min.	TYP.	Max.	Unit
VPP Setup Time	TVPS	2.0	-	-	μS
Data Setup Time	TDS	2.0	-	-	μS
Data Hold Time	TDH	2.0	-	-	μS
Address Setup Time	TAS	2.0	-	-	μS
Address Hold Time	TAH	0	-	-	μS
$\overline{CE}$ Program Pulse Width for Program Operation	TPWP	290	300	310	μS
OECTRL Setup Time	TOCS	2.0	-	-	μS
OECTRL Hold Time	TOCH	2.0	-	-	μS
$\overline{OE}$ Setup Time	TOES	2.0	-	-	μS
$\overline{OE}$ High to Output Float	TDFP	0	-	130	nS
Data Valid from $\overline{OE}$	TOEV	-	-	150	nS

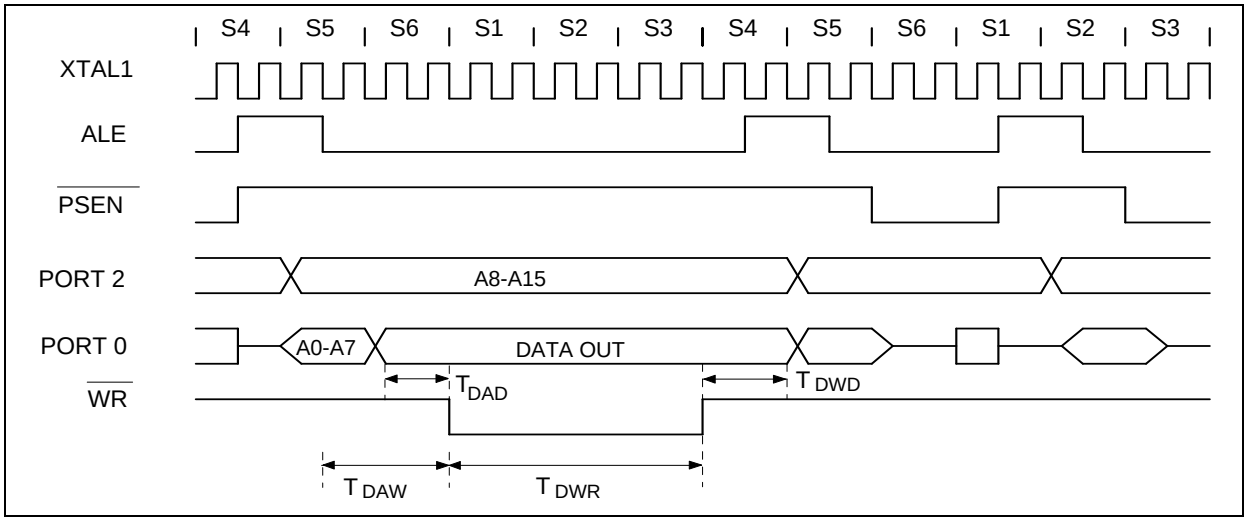
Note: Flash data can be accessed only in flash mode. The RST pin must pull in VIH status, the ALE pin must pull in VIL status, and the $\overline{PSEN}$ pin must pull in VIH status.

21.4 TIMING waveforms

21.4.1 Program Fetch Cycle



21.4.2 Data Read Cycle



```
    mov     SFRCN,#PROGRAM_ROM
    mov     DPTR,#0000h
    mov     A,#055h
wr_lp:
    mov     TH0,#HIGH(65536-PROGRAM_TIME)
    mov     TL0,#LOW (65536-PROGRAM_TIME)
    mov     SFRFD,A
    mov     SFRAL,DPL
    mov     SFRAH,DPH
    setb    TR0
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    cpl     A
    inc     DPTR
    mov     R0,DPL
    cjne    R0,#LOW (APROM_END_ADDRESS),wr_lp
    mov     R1,DPH
    cjne    R1,#HIGH(APROM_END_ADDRESS),wr_lp
    ret
;*********************************************************************************
;*Program Verify APROM BANK, read APROM 55h,AAh,55h,AAh........
;*********************************************************************************
Program_Verify_APROM:
    mov     SFRCN,#PROGRAM_VERIFY_ROM
    mov     DPTR,#0000h
    mov     B,#055h
rd_lp:
    mov     TH0,#HIGH(65536-READ_TIME)
    mov     TL0,#LOW (65536-READ_TIME)
    mov     SFRAL,DPL
    mov     SFRAH,DPH
    setb    TR0
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    mov     A,SFRFD
    cjne    A,B,Program_Fail
    mov     A,B
```