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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78i054dfg

2 FEATURES

- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
  - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
  - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4V to 5.5V
- Temperature grade is (-40°C~85°C)
- Pin and Instruction-sets compatible with MCS-51
- 256 bytes of on-chip scratchpad RAM
- 16K/8K/4K bytes electrically erasable/programmable Flash EPROM
- 2K bytes LDROM support ISP function (Reference Application Note)
- 64KB program memory address space
- 64KB data memory address space
- Four 8-bit bi-directional ports
- 8-sources, 4-level interrupt capability
- One extra 4-bit bit-addressable I/O port, additional $\overline{INT2}$ / $\overline{INT3}$ (available on PQFP, PLCC and LQFP package)
- Three 16-bit timer/counters
- One full duplex serial port
- Watchdog Timer
- EMI reduction mode
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78I054DDG
  - Lead Free (RoHS) PLCC 44: W78I054DPG
  - Lead Free (RoHS) PQFP 44: W78I054DFG
  - Lead Free (RoHS) LQFP 48: W78I054DLG
  - Lead Free (RoHS) DIP 40: W78I052DDG
  - Lead Free (RoHS) PLCC 44: W78I052DPG
  - Lead Free (RoHS) PQFP 44: W78I052DFG
  - Lead Free (RoHS) LQFP 48: W78I052DLG
  - Lead Free (RoHS) DIP 40: W78I051DDG
  - Lead Free (RoHS) PLCC 44: W78I051DPG
  - Lead Free (RoHS) PQFP 44: W78I051DFG
  - Lead Free (RoHS) LQFP 48: W78I051DLG

6 BLOCK DIAGRAM

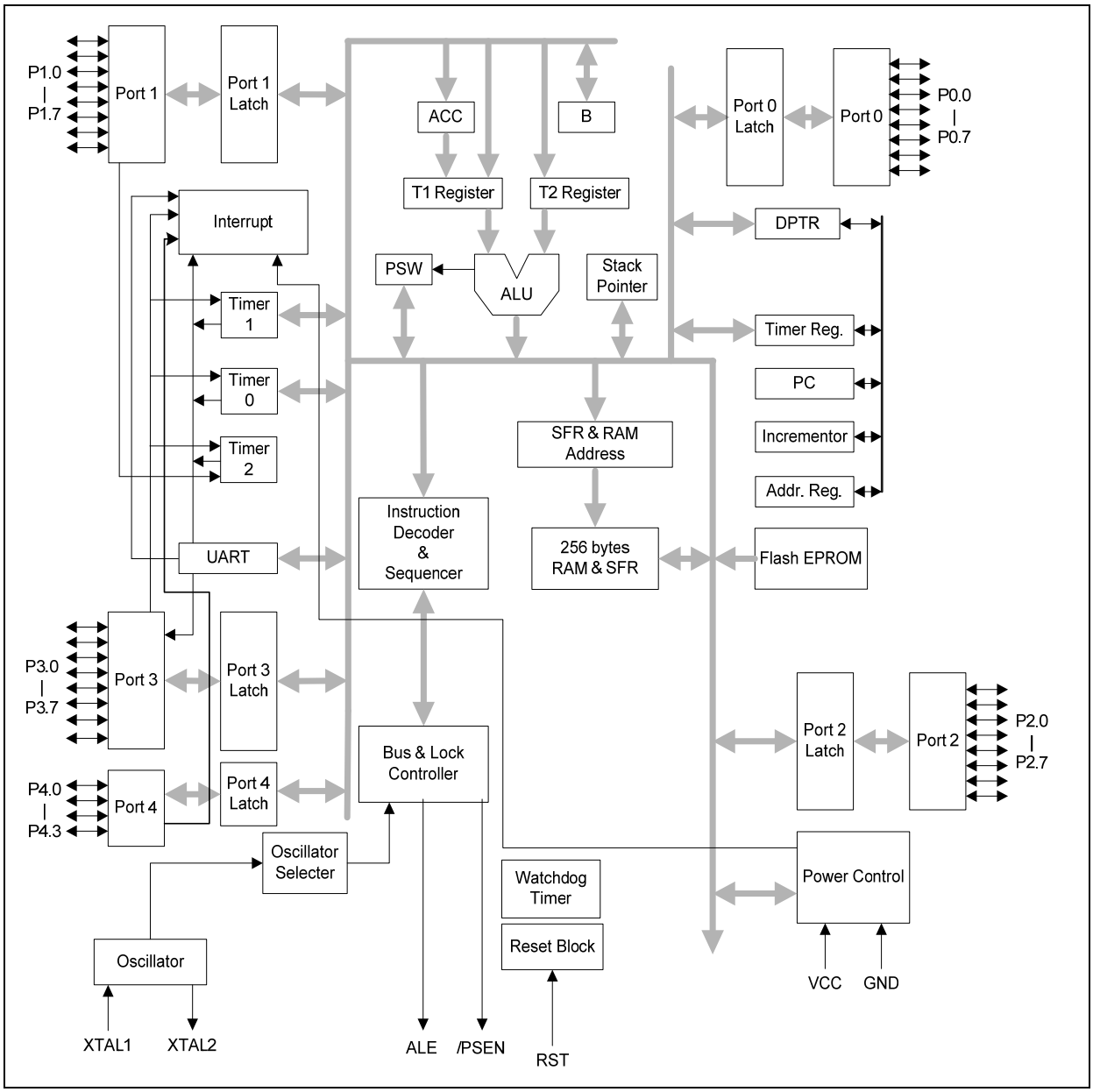


Figure 6- 1 W78I054D/W78I052D/W78I051D Block Diagram

7.6 Data Pointers

The data pointer of W78I054D/W78I052D/W78I051D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

7.7 Architecture

The W78I054D/W78I052D/W78I051D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

7.7.1 ALU

The ALU is the heart of the W78I054D/W78I052D/W78I051D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

7.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78I054D/W78I052D/W78I051D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

7.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

7.7.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

7.7.5 Scratch-pad RAM

The W78I054D/W78I052D/W78I051D series has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

7.7.6 Stack Pointer

The W78I054D/W78I052D/W78I051D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78I054D/W78I052D/W78I051D. Hence the size of the stack is limited by the size of this RAM.

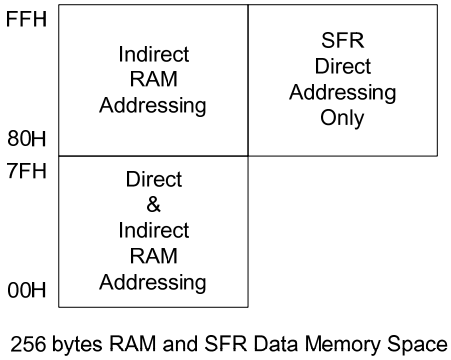


Figure 8- 2 W78I054D/W78I052D/W78I051D RAM and SFR Memory Map

Since the scratch-pad RAM is only 256bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

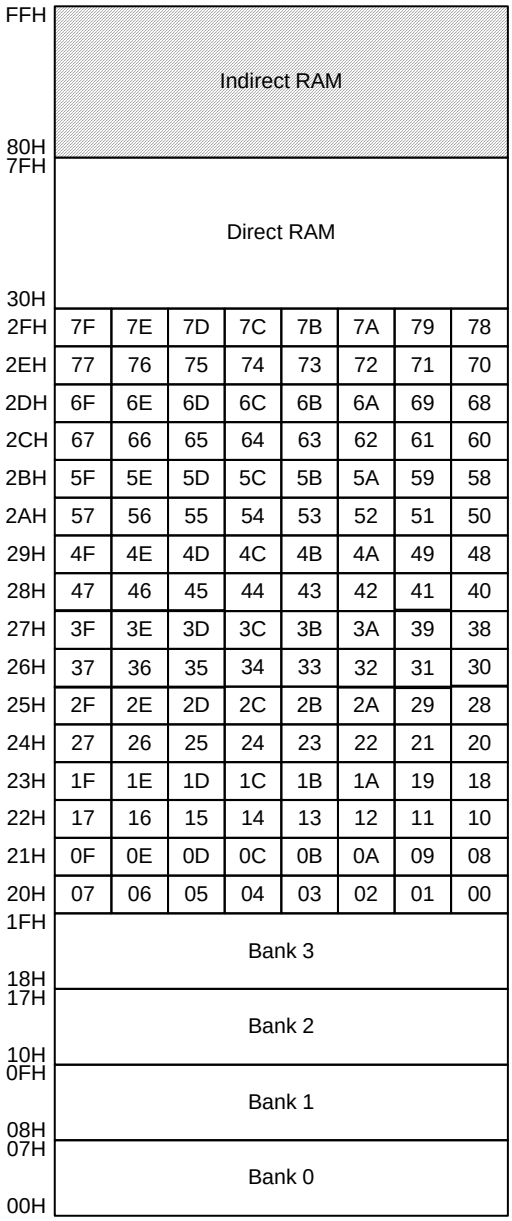


Figure 8- 3 Scratch-pad RAM

8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78I054D/W78I052D/W78I051D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 13-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1)

BIT	NAME	FUNCTION
0	ALE_OFF	1: Disenable ALE output 0: Enable ALE output

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

BIT	NAME	FUNCTION
7	ENW	Enable watch-dog if set.
6	CLRW	Clear watch-dog timer and Pre-scalar if set. This flag will be cleared automatically.
5	WIDL	If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.
2-0	PS2-0	Watch-dog Pre-scalar timer select. Pre-scalar is selected when set PS2–0 as follows:

PS2	PS1	PS0	PRE-SCALAR SELECT
0	0	0	2
0	0	1	8
0	1	0	4
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

BIT	NAME	FUNCTION
7-0	P1.[7:0]	General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read.

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

EAPAGE ERASE PAGE Operation Modes

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	EAPG1	EAPG0

Mnemonic: EAPAGE Address: BD

BIT	NAME	FUNCTION
1	EAPG1	1.To ease PAGE1 when ease command is set.(LD flash)
0	EAPG0	1.To ease PAGE0 when ease command is set. (AP Flash)

```
;CPU Clock = 12MHz/12T mode
READ_TIME           EQU     1
PROGRAM_TIME        EQU     50
ERASE_TIME          EQU     5000
```

Erase_AP Flash:

```
    mov     EAPAGE,#01h         ;set EAPAGE is APROM
    mov     SFRCN,#ERASE_ROM
    mov     TL0,#LOW (65536-ERASE_TIME)
    mov     TH0,#HIGH(65536-ERASE_TIME)
    setb    TR0
    mov     CHPCON,#00000011b
    mov     EAPAGE,#00h         ;clear EAPAGE
    clr     TF0
    clr     TR0
    ret
```

Erase_LD Flash:

```
    mov     EAPAGE,#02h         ;set EAPAGE is LDROM
    mov     SFRCN,#ERASE_ROM
    mov     TL0,#LOW (65536-ERASE_TIME)
    mov     TH0,#HIGH(65536-ERASE_TIME)
    setb    TR0
    mov     CHPCON,#00000011b
    mov     EAPAGE,#00h         ;clear EAPAGE
    clr     TF0
    clr     TR0
    ret
```

Chip Control

Bit:	7	6	5	4	3	2	1	0

7-0	ACC	The A or ACC register is the standard 8052 accumulator.

B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

Bit	Name	Function
7-0	B	The B register is the standard 8052 register that serves as a second accumulator.

Op-code	HEX Code	Bytes	W78I054D/W78I052D/W78I051D series Clock cycles
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12
CPL bit	B2	2	12
ANL C, bit	82	2	24
ANL C, /bit	B0	2	24
ORL C, bit	72	2	24
ORL C, /bit	A0	2	24
MOV C, bit	A2	2	12
MOV bit, C	92	2	24
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	24
LCALL addr16	12	3	24
RET	22	1	24
RETI	32	1	24
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	24
LJMP addr16	02	3	24
JMP @A+DPTR	73	1	24
SJMP rel	80	2	24
JZ rel	60	2	24
JNZ rel	70	2	24
JC rel	40	2	24
JNC rel	50	2	24

11 INSTRUCTION TIMING

A machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods or 1us if the oscillator frequency is 12MHz.

Each state is divided into a Phase 1 half and a Phase 2 half. The fetch/execute sequences in states and phases for various kinds of instructions. Normally two program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code bytes, the CPU simply ignores the extra fetch, and the Program Counter is not incremented. Execution of a one-cycle instruction begins during State 1 of the machine cycle, when the OPCODE is latched into the Instruction Register. A second fetch occurs during S4 of the same machine cycle. Execution is complete at the end of State 6 of this machine cycle.

The MOVX instructions take two machine cycles to execute. No program fetch is generated during the second cycle of a MOVX instruction. This is the only time program fetches are skipped. The fetch/execute sequence for MOVX instructions.

The fetch/execute sequences are the same whether the Program Memory is internal or external to the chip. Execution times do not depend on whether the Program Memory is internal or external.

the signals and timing involved in program fetches when the Program Memory is external. If Program Memory is external, then the Program Memory read strobe PSEN is normally activated twice per machine cycle. If an access to external Data Memory occurs, two PSEN pulse are skipped, because the address and data bus are being used for the Data Memory access. Note that a Data Memory bus cycle takes twice as much time as a Program Memory bus cycle.

16 SERIAL PORT

Serial port in this device is a full duplex port. The serial port is capable of synchronous as well as asynchronous communication. In Synchronous mode the device generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the device whether it is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W78I054D/W78I052D/W78I051D.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of this device and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

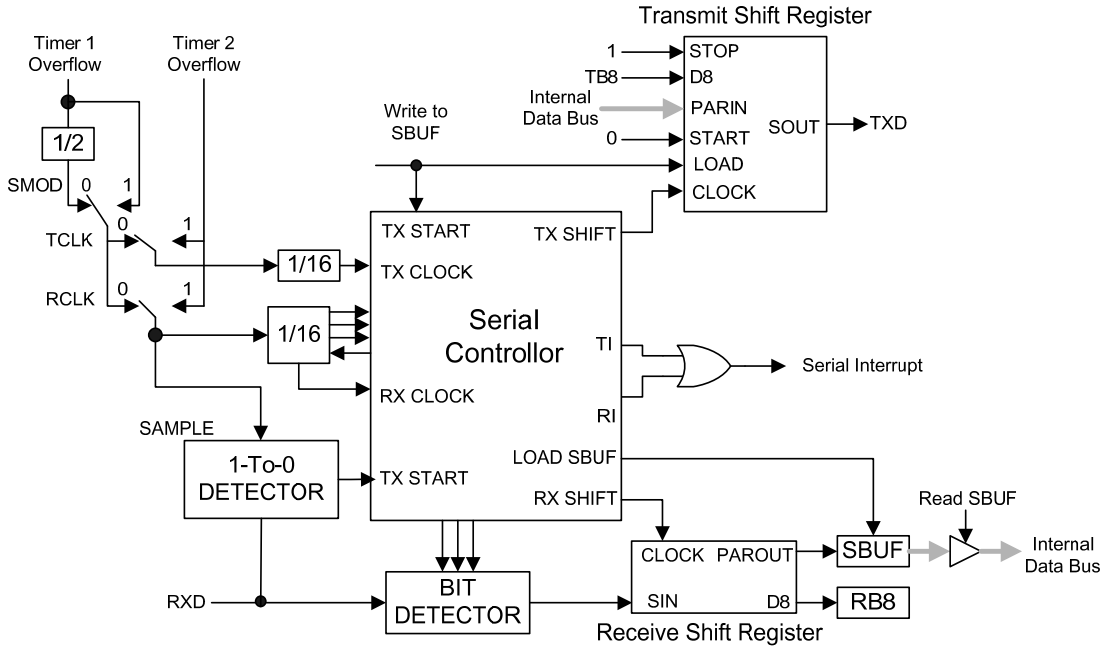


Figure 16- 4 Serial port mode 3

SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit Function
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

Table 17- 1 Serial Ports Modes

20 TYPICAL APPLICATION CIRCUITS

External Program Memory and Crystal

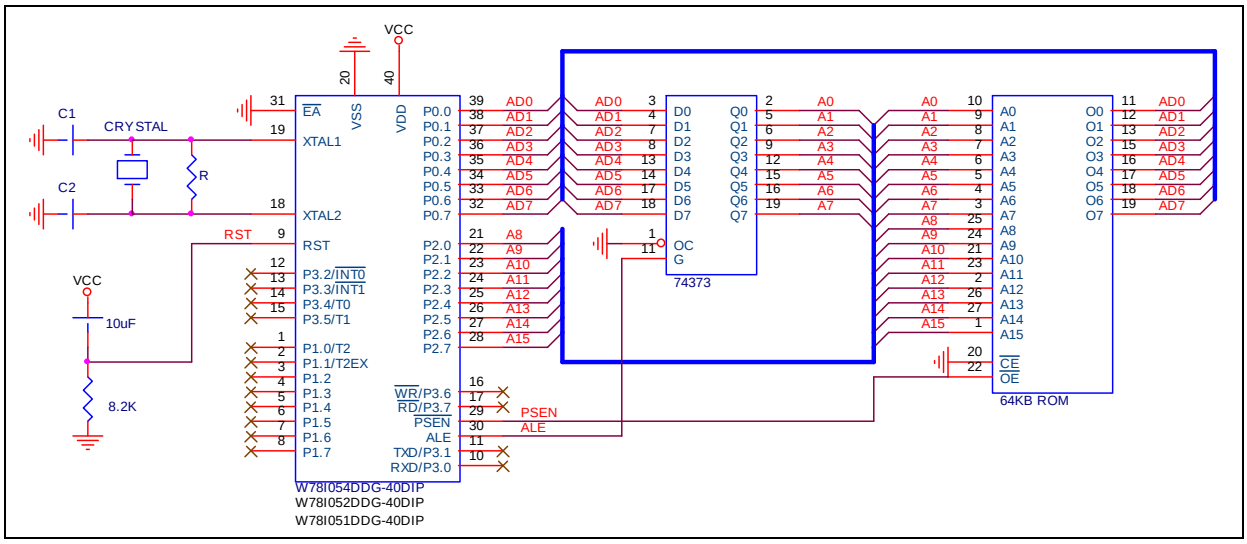


Figure A

Expanded External Data Memory and Oscillator

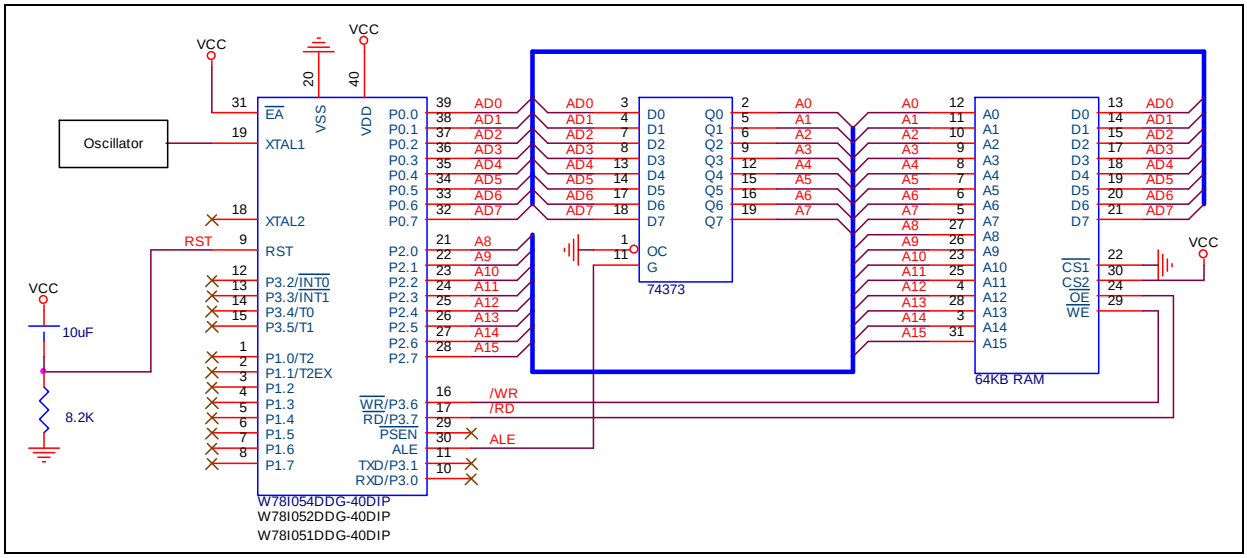


Figure B

21.2 DC ELECTRICAL CHARACTERISTICS

T_A =-40℃~+85℃, V_{DD}=2.4V~5.5V, V_{SS}=0V

Sym	Parameter	Test Condition	Min	Typ[*1]	Max	Unit
V_{IL}	Input Low Voltage (Ports 0~4, /EA, XTAL1, RST)	2.4 < V_{DD} < 5.5V	-0.5		0.2V_{DD} -0.1	V
V_{IH}	Input High Voltage (Ports 0~4, /EA)	2.4 < V_{DD} < 5.5V	0.2V_{DD} +0.9		V_{DD}+ 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.4 < V_{DD} < 5.5V	0.7V_{DD}		V_{DD}+ 0.5	V
V_{OL}	Output Low Voltage (Ports 0~4, ALE, /PSEN)	V_{DD}=4.5V, I_{OL}= 12.0mA[*3,*4] V_{DD}=2.4V, I_{OL}= 10mA[*3,*4]			0.4	V
V_{OH1}	Output High Voltage (Ports 1~4)	V_{DD}=4.5V, I_{OH}= -300μA[*4] V_{DD}=2.4V, I_{OH}= -35μA[*4]	2.4 2.0			V
V_{OH2}	Output High Voltage (Ports 0 & 2 in external bus mode, ALE, /PSEN)	V_{DD}=4.5V, I_{OH}= -8.0mA[*4] V_{DD}=2.4V, I_{OH}= -2.2mA[*4]	2.4 2.0			V
I_{IL}	Logical 0 Input Current (Ports 1~4)	V_{DD}=5.5V, V_{IN}=0.4V		-45	-50	μA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1~4) [*2]	V_{DD}=5.5V, V_{IN}=2.0V		-510	-650	μA
I_{LI}	Input Leakage Current (Port 0)	0 < V_{IN} < V_{DD}+0.5		±0.1	±10	μA
I_{DD}	Power Supply Current	Active mode[*5] @12MHz, V_{DD}=5.0V @40MHz, V_{DD}=5.0V @12MHz, V_{DD}=3.3V @20MHz, V_{DD}=3.3V		 9.5 16.0 3.1 3.7		mA
		Idle mode @12MHz, V_{DD}=5.0V @40MHz, V_{DD}=5.0V @12MHz, V_{DD}=3.3V @20MHz, V_{DD}=3.3V		 3.5 9.2 1.2 1.7		mA
		Power-down mode		<1	50	μA
R_{RST}	RST-pin Internal Pull-down Resistor	2.4 < V_{DD} < 5.5V	100		225	KΩ

Note:

*1: Typical values are not guaranteed. The values listed are tested at room temperature and based on a limited number of samples.

*2: Pins of ports 1~4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.

*3: Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20mA
Maximum I_{OL} per 8-bit port: 40mA
Maximum total I_{OL} for all outputs: 100mA

*4: If I_{OH} exceeds the test condition, V_{OH} will be lower than the listed specification.
If I_{OL} exceeds the test condition, V_{OL} will be higher than the listed specification.

*5: Tested while CPU is kept in reset state and EA=H, Port0=H.

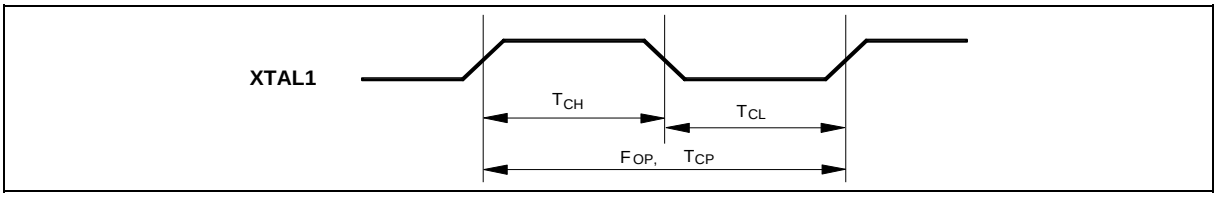
Voltage	**Max.** Frequency	6T/12T mode	Note
4.5-5.5V	40MHz	12T	
4.5-5.5V	20MHz	6T	
2.4V	20MHz	12T	
2.4V	10MHz	6T	

Frequency VS Voltage Table

21.3 AC ELECTRICAL CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation.

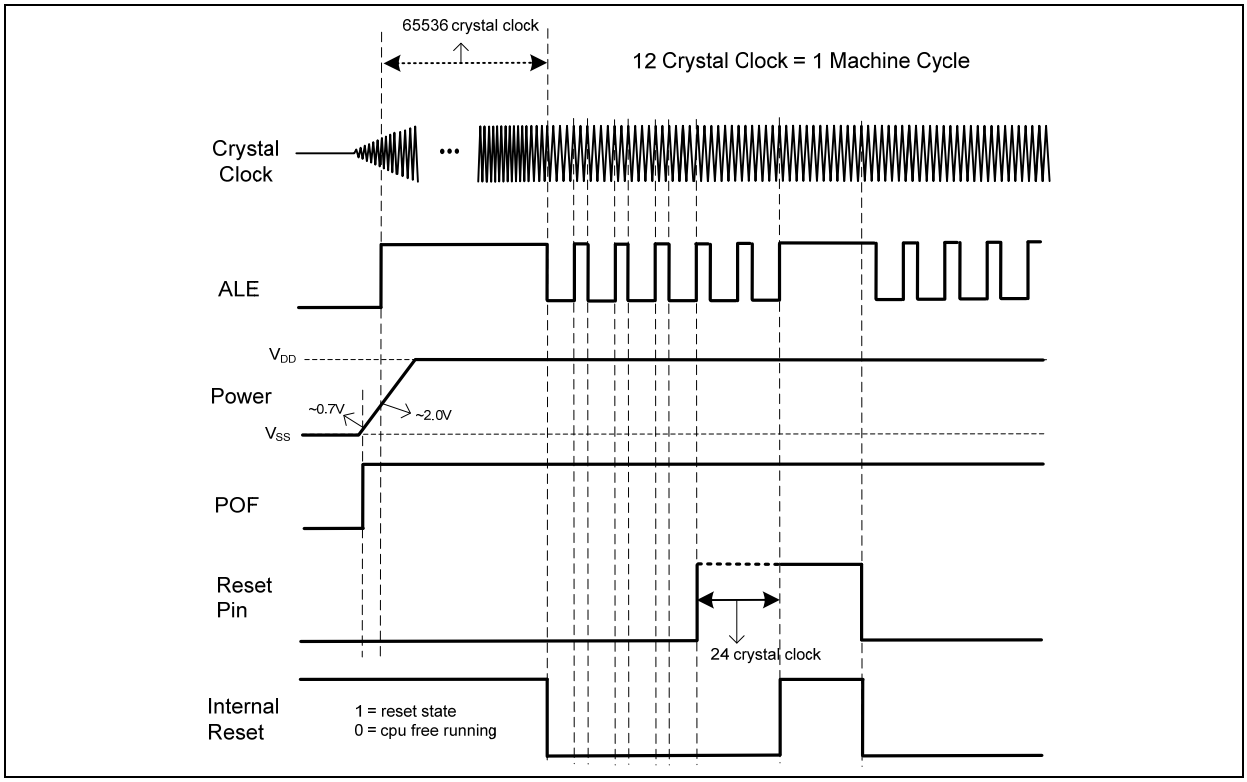
21.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	Tch	10	-	-	nS	3
Clock Low	Tcl	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.

21.4.5 Reset Pin Access Cycle



```
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    mov     A,SFRFD             ;read device id high byte
    ret
;*****************************************************************************
; * read device ID low
;*****************************************************************************
Read_Device_ID_LOW:
    mov     SFRAL,#0FEh
    mov     SFRAH,#0FFh
    mov     SFRCN,#READ_DID
    mov     TL0,#LOW (65536-READ_TIME)
    mov     TH0,#HIGH(65536-READ_TIME)
    setb    TR0
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    mov     A,SFRFD             ;read device id low byte
    ret
;*****************************************************************************
;*  Flash standby mode
;*****************************************************************************
Standby:
    mov     SFRCN,#FLASH_STANDBY
    mov     SFRFD,#0FFh
    mov     SFRAL,#0FFh
    mov     SFRAH,#0FFh
    setb    TR0
    mov     CHPCON,#00000011b
    clr     TF0
    clr     TR0
    ret
;*****************************************************************************
;*  Erase APROM
;*****************************************************************************
Erase_APROM:
    mov     EAPAGE,#01h         ;set EAPAGE is APROM
    mov     SFRCN,#ERASE_ROM
```