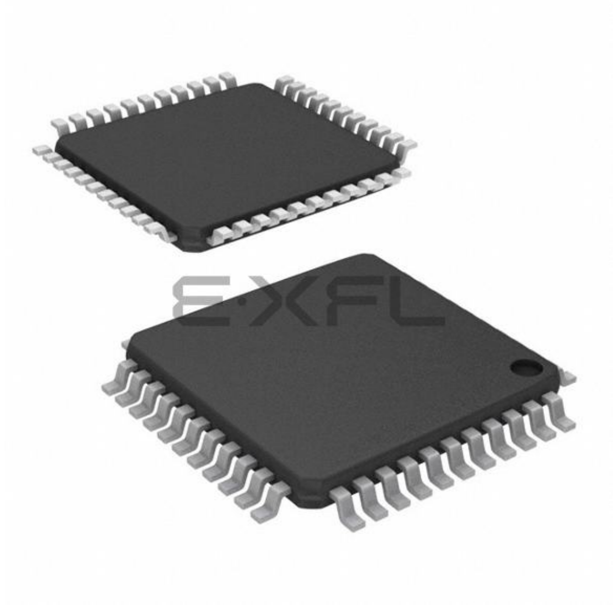


## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | S08 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa32vldr |

| Field | Description | Values |
|---|---|---|
| CC | Package designator | • QH = 64-pin QFP<br>• LH = 64-pin LQFP<br>• LF = 48-pin LQFP<br>• LD = 44-pin LQFP<br>• LC = 32-pin LQFP |

## 2.4 Example

This is an example part number:

MC9S08PA60VQH

# 3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 1. Parameter Classifications**

| | |
|---|---|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

**NOTE**

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

# 4 Ratings

## 4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -6000 | +6000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105°C | -100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

## 4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either $V_{SS}$ or $V_{DD}$) or the programmable pullup resistor associated with the pin is enabled.

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.3 | 5.8 | V |
| $I_{DD}$ | Maximum current into $V_{DD}$ | — | 120 | mA |
| $V_{DIO}$ | Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL) | –0.3 | $V_{DD}$ + 0.3 | V |

*Table continues on the next page...*

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{AIO}$ | Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

## 5.1 Nonswitching electrical specifications

### 5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 2. DC characteristics**

| Symbol | C | Descriptions | | | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| — | — | Operating voltage | | — | 2.7 | — | 5.5 | V |
| $V_{OH}$ | P | Output high voltage | All I/O pins, low-drive strength | 5 V, $I_{load}$ = -2 mA | $V_{DD}$ - 1.5 | — | — | V |
| | C | | | 3 V, $I_{load}$ = -0.6 mA | $V_{DD}$ - 0.8 | — | — | V |
| | P | | High current drive pins, high-drive strength | 5 V, $I_{load}$ = -20 mA | $V_{DD}$ - 1.5 | — | — | V |
| | C | | | 3 V, $I_{load}$ = -6 mA | $V_{DD}$ - 0.8 | — | — | V |
| $I_{OHT}$ | D | Output high current | Max total $I_{OH}$ for all ports | 5 V | — | — | -100 | mA |
| | | | | 3 V | — | — | -60 | |
| $V_{OL}$ | P | Output low voltage | All I/O pins, low-drive strength | 5 V, $I_{load}$ = 2 mA | — | — | 1.5 | V |
| | C | | | 3 V, $I_{load}$ = 0.6 mA | — | — | 0.8 | V |
| | P | | High current drive pins, high-drive strength[2] | 5 V, $I_{load}$ =20 mA | — | — | 1.5 | V |
| | C | | | 3 V, $I_{load}$ = 6 mA | — | — | 0.8 | V |
| $I_{OLT}$ | D | Output low current | Max total $I_{OL}$ for all ports | 5 V | — | — | 100 | mA |
| | | | | 3 V | — | — | 60 | |

*Table continues on the next page...*

## Table 2. DC characteristics (continued)

| Symbol | C | Descriptions | | | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | P | Input high voltage | All digital inputs | $V_{DD}$>4.1V | 0.70 × $V_{DD}$ | — | — | V |
| | | | | $V_{DD}$>2.7V | 0.85 × $V_{DD}$ | — | — | |
| $V_{IL}$ | P | Input low voltage | All digital inputs | $V_{DD}$>4.1V | — | — | 0.35 × $V_{DD}$ | V |
| | | | | $V_{DD}$>2.7V | — | — | 0.30 × $V_{DD}$ | |
| $V_{hys}$ | C | Input hysteresis | All digital inputs | — | 0.06 × $V_{DD}$ | — | — | mV |
| $\|I_{In}\|$ | P | Input leakage current | All input only pins (per pin) | $V_{IN} = V_{DD}$ or $V_{SS}$ | — | 0.1 | 1 | μA |
| $\|I_{OZ}\|$ | P | Hi-Z (off-state) leakage current | All input/output (per pin) | $V_{IN} = V_{DD}$ or $V_{SS}$ | — | 0.1 | 1 | μA |
| $\|I_{OZTOT}\|$ | C | Total leakage combined for all inputs and Hi-Z pins | All input only and I/O | $V_{IN} = V_{DD}$ or $V_{SS}$ | — | — | 2 | μA |
| $R_{PU}$ | P | Pullup resistors | All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/RESET | — | 17.5 | — | 52.5 | kΩ |
| $R_{PU}$[3] | P | Pullup resistors | PTA5/IRQ/TCLK/RESET | — | 17.5 | — | 52.5 | kΩ |
| $I_{IC}$ | D | DC injection current[4, 5, 6] | Single pin limit | $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ | -0.2 | — | 2 | mA |
| | | | Total MCU limit, includes sum of all stressed pins | | -5 | — | 25 | |
| $C_{In}$ | C | Input capacitance, all pins | | — | — | — | 8 | pF |
| $V_{RAM}$ | C | RAM retention voltage | | — | 2.0 | — | — | V |

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA5, are internally clamped to $V_{SS}$ and $V_{DD}$.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure that external $V_{DD}$ load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

## Table 3. LVD and POR Specification

| Symbol | C | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR}$ | D | POR re-arm voltage[1] | 1.5 | 1.75 | 2.0 | V |
| $V_{LVDH}$ | C | Falling low-voltage detect threshold - high range (LVDV = 1)[2] | 4.2 | 4.3 | 4.4 | V |

*Table continues on the next page...*

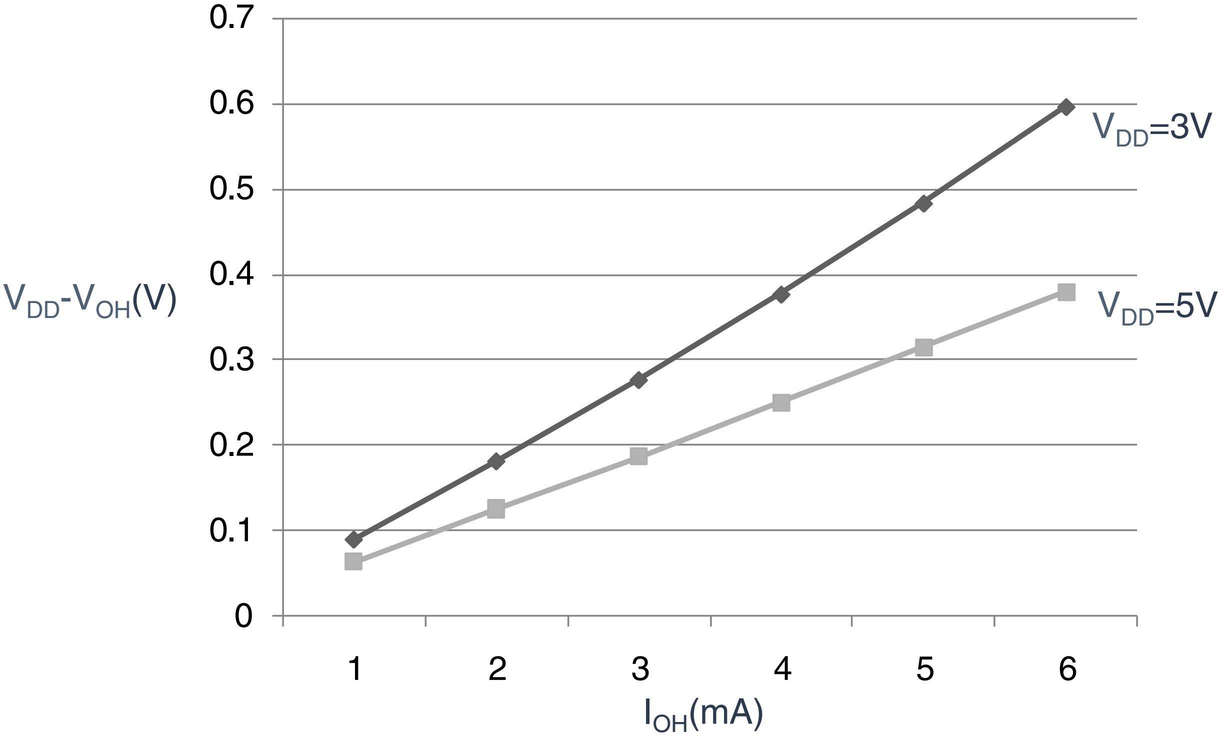


Figure 1. Typical $I_{OH}$ Vs. $V_{DD}$-$V_{OH}$

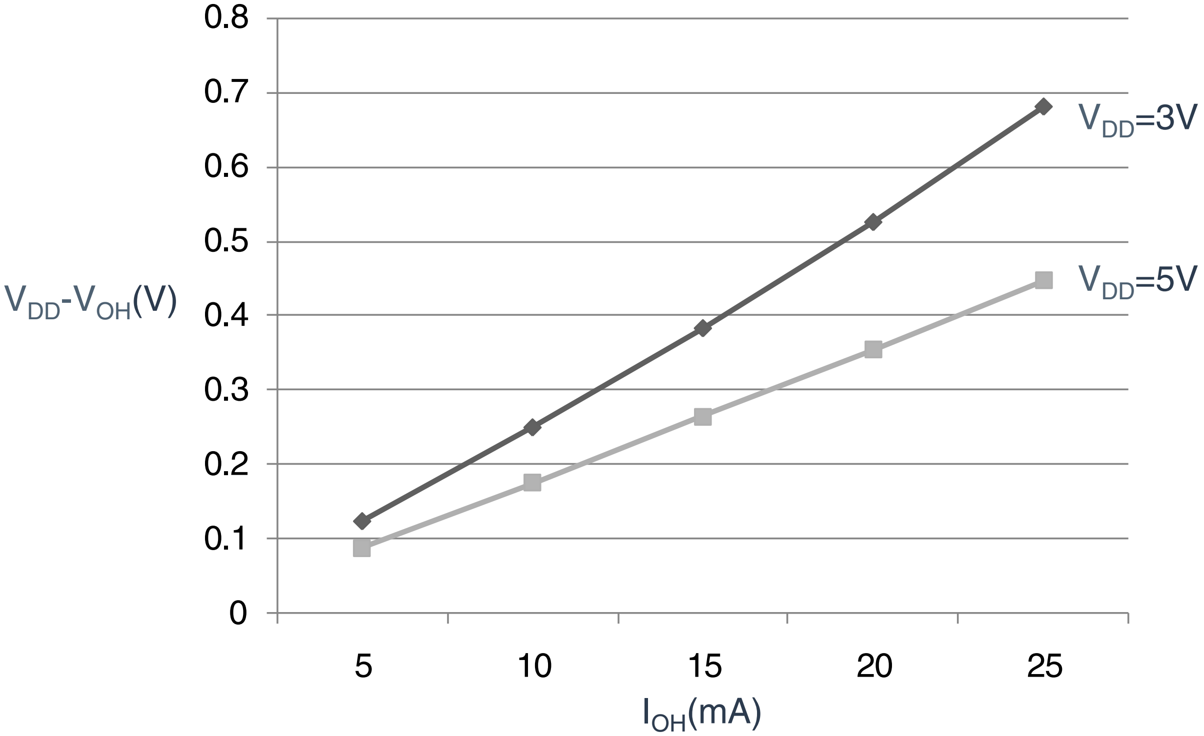


Figure 2. Typical $I_{OH}$ Vs. $V_{DD}$-$V_{OH}$ (High current drive)

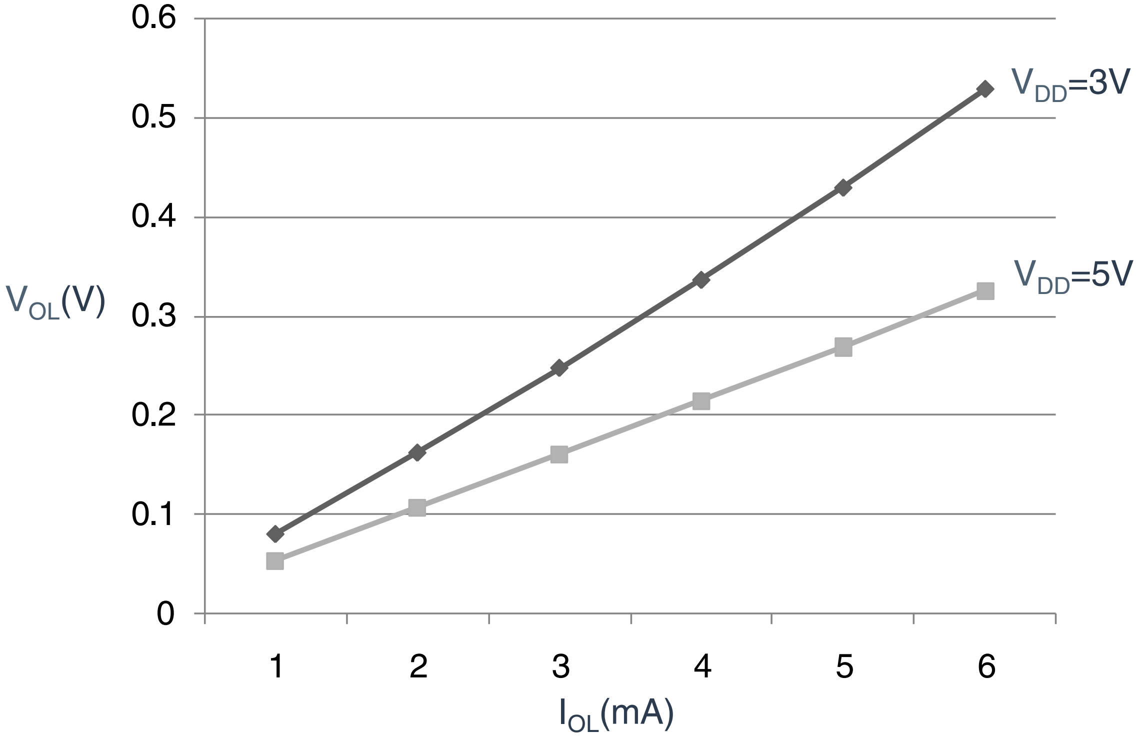


Figure 3. Typical $I_{OL}$ Vs. $V_{OL}$

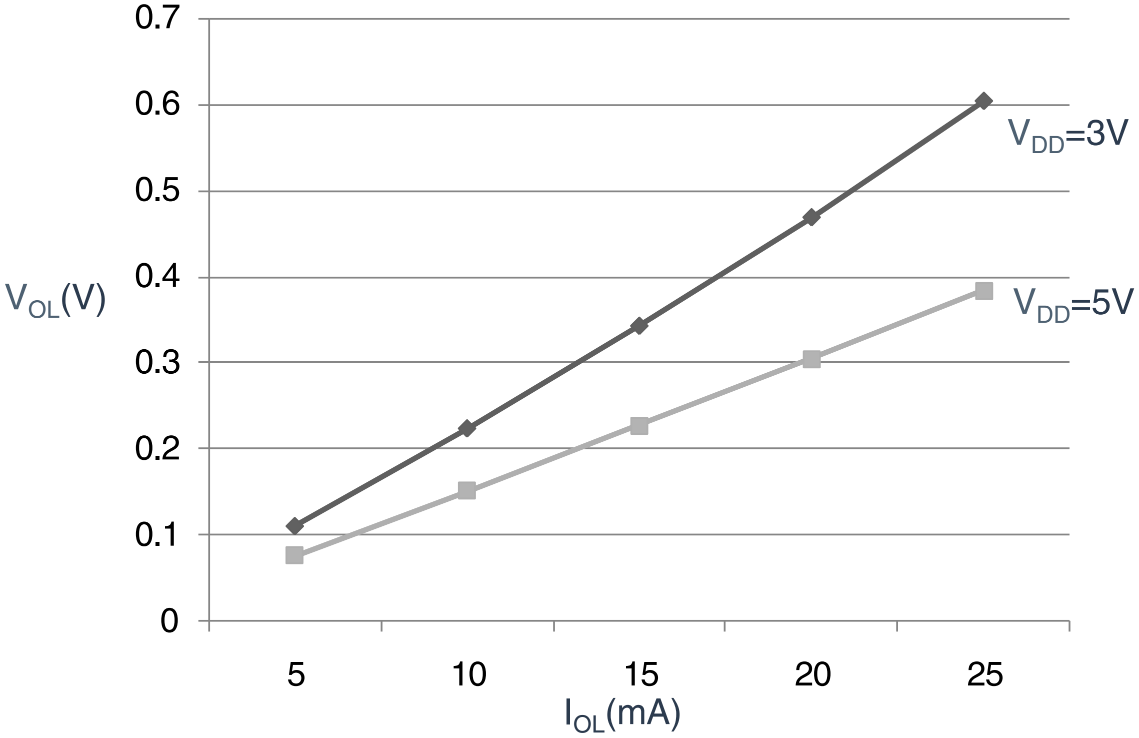


Figure 4. Typical $I_{OL}$ Vs. $V_{OL}$ (High current drive)

**Table 5. Control timing (continued)**

| Num | C | Rating | | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 7 | D | IRQ pulse width | Asynchronous path[2] | $t_{ILIH}$ | 100 | — | — | ns |
| | D | | Synchronous path | $t_{IHIL}$ | $1.5 \times t_{cyc}$ | — | — | ns |
| 8 | D | Keyboard interrupt pulse width | Asynchronous path[2] | $t_{ILIH}$ | 100 | — | — | ns |
| | D | | Synchronous path | $t_{IHIL}$ | $1.5 \times t_{cyc}$ | — | — | ns |
| 9 | C | Port rise and fall time - Normal drive strength (HDRVE_PTXx = 0) (load = 50 pF) | — | $t_{Rise}$ | — | 10.2 | — | ns |
| | C | | | $t_{Fall}$ | — | 9.5 | — | ns |
| | C | Port rise and fall time - Extreme high drive strength (HDRVE_PTXx = 1) (load = 50 pF)[4] | — | $t_{Rise}$ | — | 5.4 | — | ns |
| | C | | | $t_{Fall}$ | — | 4.6 | — | ns |

1. Typical values are based on characterization data at $V_{DD}$ = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of $t_{MSH}$ after $V_{DD}$ rises above $V_{LVD}$.
4. Timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ levels. Temperature range -40 °C to 105 °C.

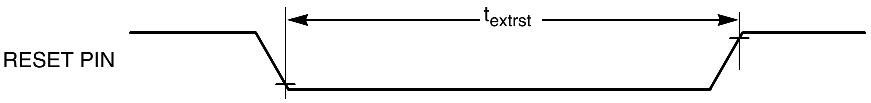


**Figure 5. Reset timing**

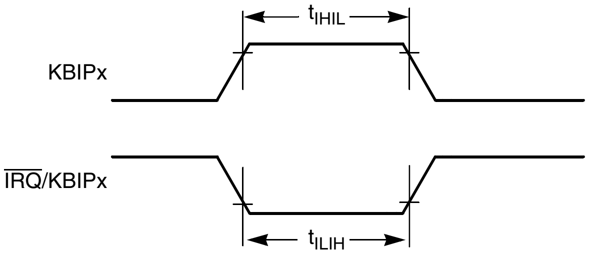


**Figure 6. IRQ/KBIPx timing**

## 5.2.2 Debug trace timing specifications

**Table 6. Debug trace operating behaviors**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{cyc}$ | Clock period | Frequency dependent | | MHz |
| $t_{wl}$ | Low pulse width | 2 | — | ns |
| $t_{wh}$ | High pulse width | 2 | — | ns |
| $t_r$ | Clock and data rise time | — | 3 | ns |
| $t_f$ | Clock and data fall time | — | 3 | ns |

*Table continues on the next page...*

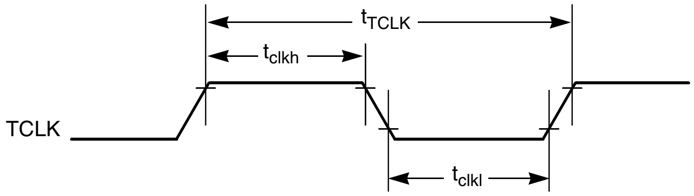


Figure 9. Timer external clock

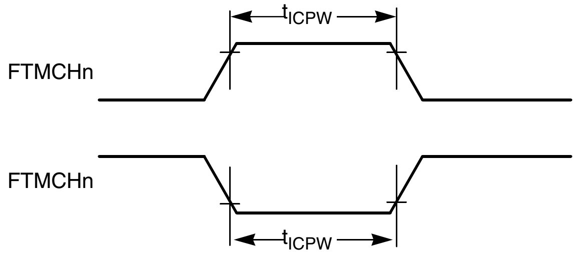


Figure 10. Timer input capture pulse

## 5.3 Thermal specifications

### 5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ will be very small.

Table 8. Thermal characteristics

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating temperature range (packaged) | $T_A$ | -40 to 105 | °C |
| Junction temperature range | $T_J$ | -40 to 150 | °C |
| Thermal resistance single-layer board | | | |
| 64-pin LQFP | $θ_{JA}$ | 71 | °C/W |
| 64-pin QFP | $θ_{JA}$ | 61 | °C/W |
| 48-pin LQFP | $θ_{JA}$ | 81 | °C/W |
| 44-pin LQFP | $θ_{JA}$ | 75 | °C/W |
| 32-pin LQFP | $θ_{JA}$ | 86 | °C/W |

*Table continues on the next page...*

## 6.1 External oscillator (XOSC) and ICS characteristics

### Table 9. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)

| Num | C | Characteristic | | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 1 | C | Oscillator crystal or resonator | Low range (RANGE = 0) | $f_{lo}$ | 32 | — | 40 | kHz |
| | C | | High range (RANGE = 1) FEE or FBE mode | $f_{hi}$ | 4 | — | 20 | MHz |
| | C | | High range (RANGE = 1), high gain (HGO = 1), FBELP mode | $f_{hi}$ | 4 | — | 20 | MHz |
| | C | | High range (RANGE = 1), low power (HGO = 0), FBELP mode | $f_{hi}$ | 4 | — | 20 | MHz |
| 2 | D | Load capacitors | | C1, C2 | See Note[3] | | | |
| 3 | D | Feedback resistor | Low Frequency, Low-Power Mode | $R_F$ | — | — | — | MΩ |
| | | | Low Frequency, High-Gain Mode | | — | 10 | — | MΩ |
| | | | High Frequency, Low-Power Mode | | — | 1 | — | MΩ |
| | | | High Frequency, High-Gain Mode | | — | 1 | — | MΩ |
| 4 | D | Series resistor - Low Frequency | Low-Power Mode [4] | $R_S$ | — | — | — | kΩ |
| | | | High-Gain Mode | | — | 200 | — | kΩ |
| 5 | D | Series resistor - High Frequency | Low-Power Mode[4] | $R_S$ | — | — | — | kΩ |
| | D | Series resistor - High Frequency, High-Gain Mode | 4 MHz | | — | 0 | — | kΩ |
| | D | | 8 MHz | | — | 0 | — | kΩ |
| | D | | 16 MHz | | — | 0 | — | kΩ |
| 6 | C | Crystal start-up time Low range = 32.768 KHz crystal; High range = 20 MHz crystal, [6] | Low range, low power | $t_{CSTL}$ | — | 1000 | — | ms |
| | C | | Low range, high power | | — | 800 | — | ms |
| | C | | High range, low power | $t_{CSTH}$ | — | 3 | — | ms |
| | C | | High range, high power | | — | 1.5 | — | ms |
| 7 | T | Internal reference start-up time | | $t_{IRST}$ | — | 20 | 50 | μs |
| 8 | D | Square wave input clock frequency | FEE or FBE mode[2] | $f_{extal}$ | 0.03125 | — | 5 | MHz |
| | D | | FBELP mode | | 0 | — | 20 | MHz |
| 9 | P | Average internal reference frequency - trimmed | | $f_{int\_t}$ | — | 32.768 | — | kHz |
| 10 | P | DCO output frequency range - trimmed | | $f_{dco\_t}$ | 16 | — | 20 | MHz |
| 11 | P | Total deviation of DCO output from trimmed frequency[5] | Over full voltage and temperature range | $\Delta f_{dco\_t}$ | — | — | ±2.0 | $\%f_{dco}$ |
| | C | | Over fixed voltage and temperature range of 0 to 70 °C | | | | ±1.0 | |
| 12 | C | FLL acquisition time[5], [7] | | $t_{Acquire}$ | — | — | 2 | ms |

*Table continues on the next page...*

### Table 9. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

| Num | C | Characteristic | Symbol | Min | Typical[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| 13 | C | Long term jitter of DCO output clock (averaged over 2 ms interval)[8] | $C_{Jitter}$ | — | 0.02 | 0.2 | $\%f_{dco}$ |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors ($C_1$,$C_2$), feedback resistor ($R_F$) and series resistor ($R_S$) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{Bus}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via $V_{DD}$ and $V_{SS}$ and variation in crystal oscillator frequency increase the $C_{Jitter}$ percentage for a given interval.

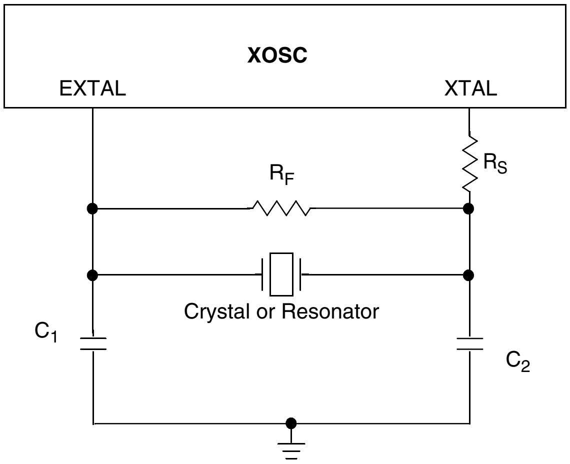


Figure 11. Typical crystal or resonator circuit

## 6.2 NVM specifications

This section provides details about program/erase times and program-erase endurance for the flash and EEPROM memories.

### Table 10. Flash characteristics

| C | Characteristic | Symbol | Min[1] | Typical[2] | Max[3] | Unit[4] |
|---|---|---|---|---|---|---|
| D | Supply voltage for program/erase -40 °C to 105 °C | $V_{prog/erase}$ | 2.7 | — | 5.5 | V |
| D | Supply voltage for read operation | $V_{Read}$ | 2.7 | — | 5.5 | V |

*Table continues on the next page...*

**Table 10. Flash characteristics (continued)**

| C | Characteristic | Symbol | Min[1] | Typical[2] | Max[3] | Unit[4] |
|---|---|---|---|---|---|---|
| D | NVM Bus frequency | $f_{NVMBUS}$ | 1 | — | 25 | MHz |
| D | NVM Operating frequency | $f_{NVMOP}$ | 0.8 | — | 1.05 | MHz |
| D | Erase Verify All Blocks | $t_{VFYALL}$ | — | — | 17030 | $t_{cyc}$ |
| D | Erase Verify Flash Block | $t_{RD1BLK}$ | — | — | 16977 | $t_{cyc}$ |
| D | Erase Verify EEPROM Block | $t_{RD1BLK}$ | — | — | 843 | $t_{cyc}$ |
| D | Erase Verify Flash Section | $t_{RD1SEC}$ | — | — | 517 | $t_{cyc}$ |
| D | Erase Verify EEPROM Section | $t_{DRD1SEC}$ | 0.10 | 0.10 | 0.11 | ms |
| D | Read Once | $t_{RDONCE}$ | — | — | 455 | $t_{cyc}$ |
| D | Program Flash (2 word) | $t_{PGM2}$ | 0.12 | 0.12 | 0.14 | ms |
| D | Program Flash (4 word) | $t_{PGM4}$ | 0.20 | 0.21 | 0.24 | ms |
| D | Program Once | $t_{PGMONCE}$ | 0.20 | 0.21 | 0.24 | ms |
| D | Program EEPROM (1 Byte) | $t_{DPGM1}$ | 0.02 | 0.02 | 0.02 | ms |
| D | Program EEPROM (2 Byte) | $t_{DPGM2}$ | 0.17 | 0.18 | 0.20 | ms |
| D | Erase All Blocks | $t_{ERSALL}$ | 96.01 | 100.78 | 125.80 | ms |
| D | Erase Flash Block | $t_{ERSBLK}$ | 95.98 | 100.75 | 125.76 | ms |
| D | Erase Flash Sector | $t_{ERSPG}$ | 19.10 | 20.05 | 25.05 | ms |
| D | Erase EEPROM Sector | $t_{DERSPG}$ | 4.81 | 5.05 | 6.30 | ms |
| D | Unsecure Flash | $t_{UNSECU}$ | 96.01 | 100.78 | 125.80 | ms |
| D | Verify Backdoor Access Key | $t_{VFYKEY}$ | — | — | 469 | $t_{cyc}$ |
| D | Set User Margin Level | $t_{MLOADU}$ | — | — | 442 | $t_{cyc}$ |
| C | FLASH Program/erase endurance $T_L$ to $T_H$ = -40 °C to 105 °C | $n_{FLPE}$ | 10 k | 100 k | — | Cycles |
| C | EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C | $n_{FLPE}$ | 50 k | 500 k | — | Cycles |
| C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C after up to 10,000 program/erase cycles | $t_{D\_ret}$ | 15 | 100 | — | years |

1. Minimun times are based on maxmum $f_{NVMOP}$ and maximum $f_{NVMBUS}$
2. Typical times are based on typical $f_{NVMOP}$ and maximum $f_{NVMBUS}$
3. Maximum times are based on minimum $f_{NVMOP}$ and maximum $f_{NVMBUS}$
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal $V_{DD}$ supply. For more detailed information about program/erase operations, see the Memory section.

## 6.3 Analog

## 6.3.1 ADC characteristics

### Table 11. 5 V 12-bit ADC operating conditions

| Characteristic | Conditions | Symb | Min | Typ[1] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| Supply voltage | Absolute | $V_{DDA}$ | 2.7 | — | 5.5 | V | — |
| | Delta to $V_{DD}$ ($V_{DD}$-$V_{DDAD}$) | $\Delta V_{DDA}$ | -100 | 0 | +100 | mV | |
| Ground voltage | Delta to $V_{SS}$ ($V_{SS}$-$V_{SSA}$)[1] | $\Delta V_{SSA}$ | -100 | 0 | +100 | mV | |
| Input voltage | | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| Input capacitance | | $C_{ADIN}$ | — | 4.5 | 5.5 | pF | |
| Input resistance | | $R_{ADIN}$ | — | 3 | 5 | kΩ | — |
| Analog source resistance | 12-bit mode<br>• $f_{ADCK}$ > 4 MHz<br>• $f_{ADCK}$ < 4 MHz | $R_{AS}$ | —<br>— | —<br>— | 2<br>5 | kΩ | External to MCU |
| | 10-bit mode<br>• $f_{ADCK}$ > 4 MHz<br>• $f_{ADCK}$ < 4 MHz | | —<br>— | —<br>— | 5<br>10 | | |
| | 8-bit mode<br>(all valid $f_{ADCK}$) | | — | — | 10 | | |
| ADC conversion clock frequency | High speed (ADLPC=0) | $f_{ADCK}$ | 0.4 | — | 8.0 | MHz | — |
| | Low power (ADLPC=1) | | 0.4 | — | 4.0 | | |

1. Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25°C, $f_{ADCK}$=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
1. DC potential difference.

**Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)**

| Characteristic | Conditions | C | Symb | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| ADC asynchronous clock source | High speed (ADLPC = 0) | P | $f_{ADACK}$ | 2 | 3.3 | 5 | MHz |
| | Low power (ADLPC = 1) | | | 1.25 | 2 | 3.3 | |
| Conversion time (including sample time) | Short sample (ADLSMP = 0) | T | $t_{ADC}$ | — | 20 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 40 | — | |
| Sample time | Short sample (ADLSMP = 0) | T | $t_{ADS}$ | — | 3.5 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 23.5 | — | |
| Total unadjusted Error | 12-bit mode | T | $E_{TUE}$ | — | ±5.0 | — | LSB |
| | 10-bit mode | P | | — | ±1.5 | ±2.0 | |
| | 8-bit mode | P | | — | ±0.7 | ±1.0 | |
| Differential Non-Liniarity | 12-bit mode | T | DNL | — | ±1.0 | — | LSB[2] |
| | 10-bit mode | P | | — | ±0.25 | ±0.5 | |
| | 8-bit mode[3] | P | | — | ±0.15 | ±0.25 | |
| Integral Non-Linearity | 12-bit mode | T | INL | — | ±1.0 | — | LSB[2] |
| | 10-bit mode | T | | — | ±0.3 | ±0.5 | |
| | 8-bit mode | T | | — | ±0.15 | ±0.25 | |
| Zero-scale error | 12-bit mode | C | $E_{ZS}$ | — | ±2.0 | — | LSB[2] |
| | 10-bit mode | P | | — | ±0.25 | ±1.0 | |
| | 8-bit mode | P | | — | ±0.65 | ±1.0 | |
| Full-scale error[5] | 12-bit mode | T | $E_{FS}$ | — | ±2.5 | — | LSB[2] |
| | 10-bit mode | T | | — | ±0.5 | ±1.0 | |
| | 8-bit mode | T | | — | ±0.5 | ±1.0 | |
| Quantization error | ≤12 bit modes | D | $E_Q$ | — | — | ±0.5 | LSB[2] |
| Input leakage error[6] | all modes | D | $E_{IL}$ | $I_{In} * R_{AS}$ | | | mV |
| Temp sensor slope | -40°C– 25°C | D | m | — | 3.266 | — | mV/°C |
| | 25°C– 125°C | | | — | 3.638 | — | |
| Temp sensor voltage | 25°C | D | $V_{TEMP25}$ | — | 1.396 | — | V |

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}$=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
3. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
3. $V_{ADIN} = V_{DDA}$
4. $I_{In}$ = leakage current (refer to DC characteristics)

### 6.3.2 Analog comparator (ACMP) electricals

**Table 13. Comparator electrical specifications**

| C | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| D | Supply voltage | $V_{DDA}$ | 2.7 | — | 5.5 | V |
| T | Supply current (Operation mode) | $I_{DDA}$ | — | 10 | 20 | μA |
| D | Analog input voltage | $V_{AIN}$ | $V_{SS}$ - 0.3 | — | $V_{DDA}$ | V |
| P | Analog input offset voltage | $V_{AIO}$ | — | — | 40 | mV |
| C | Analog comparator hysteresis (HYST=0) | $V_H$ | — | 15 | 20 | mV |
| C | Analog comparator hysteresis (HYST=1) | $V_H$ | — | 20 | 30 | mV |
| T | Supply current (Off mode) | $I_{DDAOFF}$ | — | 60 | — | nA |
| C | Propagation Delay | $t_D$ | — | 0.4 | 1 | μs |

## 6.4 Communication interfaces

### 6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% $V_{DD}$ and 70% $V_{DD}$, unless noted, and 100 pF load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

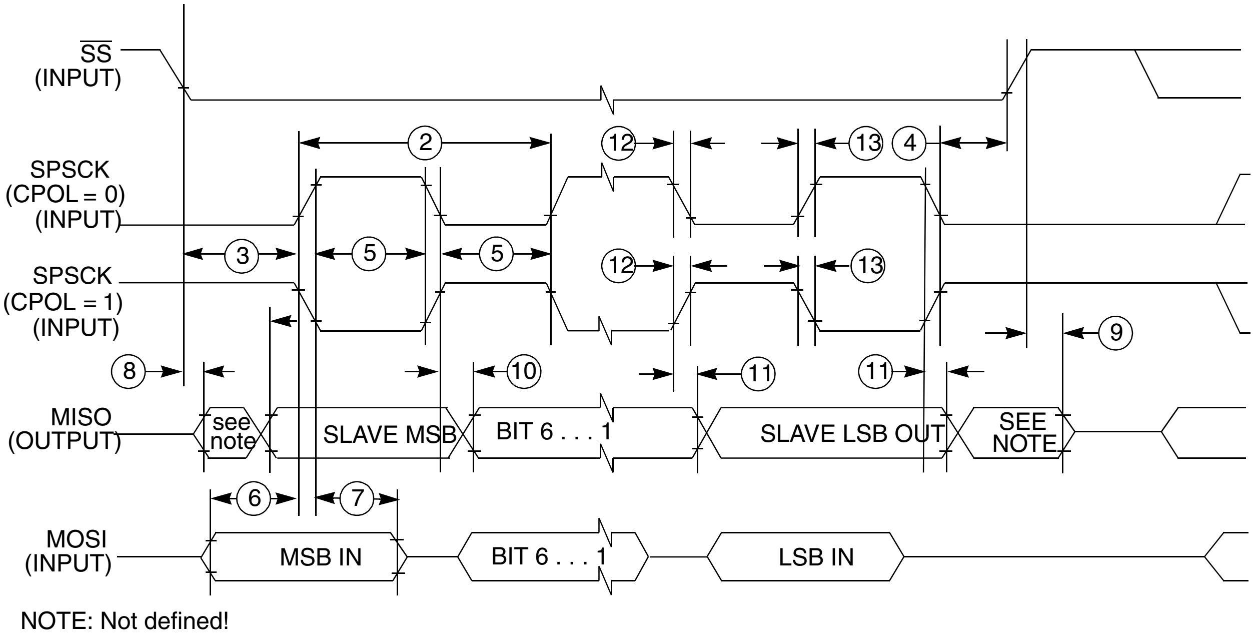
**Table 14. SPI master mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{Bus}$/2048 | $f_{Bus}$/2 | Hz | $f_{Bus}$ is the bus clock |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{Bus}$ | 2048 x $t_{Bus}$ | ns | $t_{Bus} = 1/f_{Bus}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{Bus}$ - 30 | 1024 x $t_{Bus}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 15 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |

*Table continues on the next page...*

## Table 15. SPI slave mode timing

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | 0 | $f_{Bus}/4$ | Hz | $f_{Bus}$ is the bus clock as defined in . |
| 2 | $t_{SPSCK}$ | SPSCK period | 4 x $t_{Bus}$ | — | ns | $t_{Bus} = 1/f_{Bus}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{Bus}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{Bus}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{Bus}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 15 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 25 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{Bus}$ | ns | Time to data active from high-impedance state |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{Bus}$ | ns | Hold time to high-impedance state |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{Bus}$ - 25 | ns | — |
|  | $t_{FI}$ | Fall time input |  |  |  |  |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
|  | $t_{FO}$ | Fall time output |  |  |  |  |



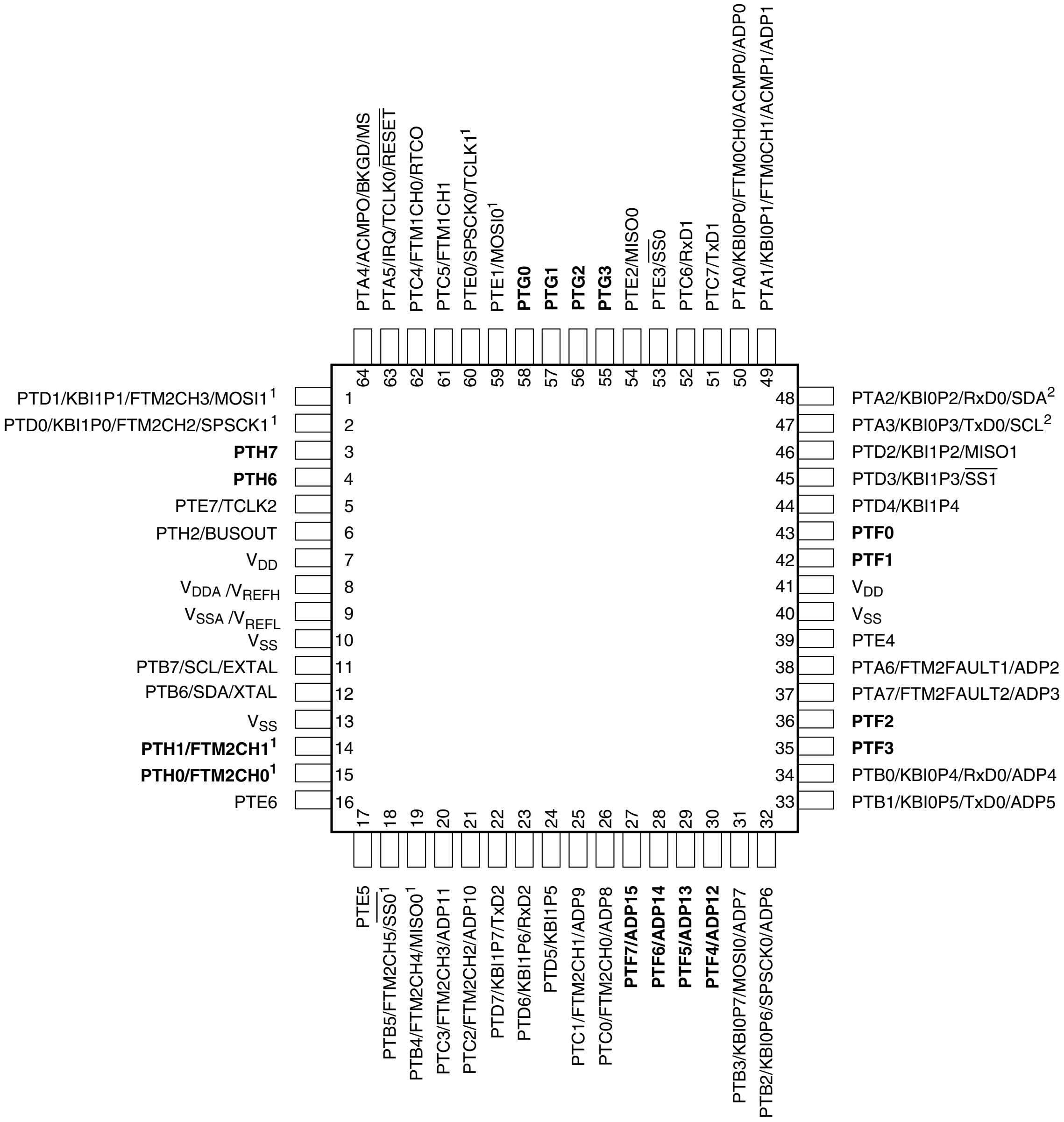
NOTE: Not defined!

Figure 15. SPI slave mode timing (CPHA = 0)

## Table 16. Pin availability by package pin-count (continued)

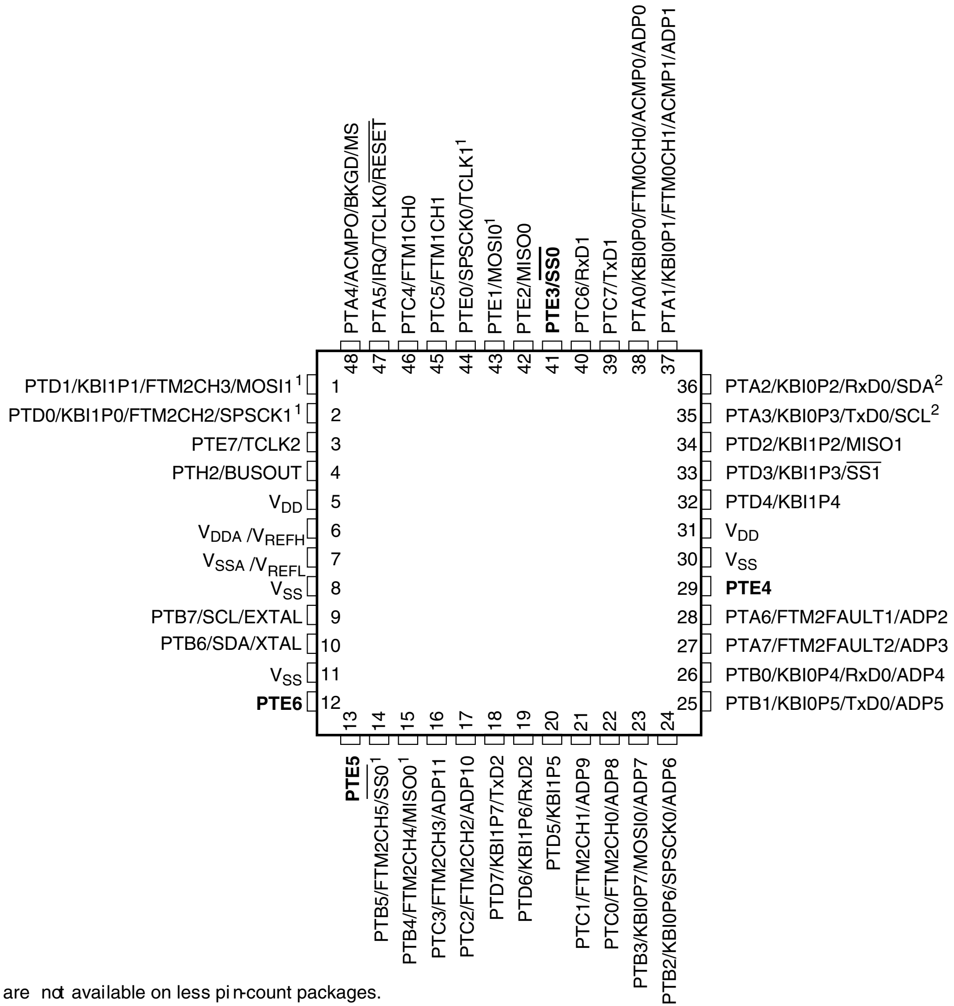
| Pin Number | | | | Lowest Priority <-- --> Highest | | | | |
|---|---|---|---|---|---|---|---|---|
| 64-LQFP<br>64-QFP | 48-LQFP | 44-LQFP | 32-LQFP | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 28 | — | — | — | PTF6 | — | — | ADP14 | — |
| 29 | — | — | — | PTF5 | — | — | ADP13 | — |
| 30 | — | — | — | PTF4 | — | — | ADP12 | — |
| 31 | 23 | 21 | 15 | PTB3 | KBI0P7 | MOSI0 | ADP7 | — |
| 32 | 24 | 22 | 16 | PTB2 | KBI0P6 | SPSCK0 | ADP6 | — |
| 33 | 25 | 23 | 17 | PTB1 | KBI0P5 | TXD0 | ADP5 | — |
| 34 | 26 | 24 | 18 | PTB0 | KBI0P4 | RXD0 | ADP4 | — |
| 35 | — | — | — | PTF3 | — | — | — | — |
| 36 | — | — | — | PTF2 | — | — | — | — |
| 37 | 27 | 25 | 19 | PTA7 | FTM2FAULT2 | — | ADP3 | — |
| 38 | 28 | 26 | 20 | PTA6 | FTM2FAULT1 | — | ADP2 | — |
| 39 | 29 | — | — | PTE4 | — | — | — | — |
| 40 | 30 | 27 | — | — | — | — | — | $V_{SS}$ |
| 41 | 31 | 28 | — | — | — | — | — | $V_{DD}$ |
| 42 | — | — | — | PTF1 | — | — | — | — |
| 43 | — | — | — | PTF0 | — | — | — | — |
| 44 | 32 | 29 | — | PTD4 | KBI1P4 | — | — | — |
| 45 | 33 | 30 | 21 | PTD3 | KBI1P3 | SS1 | — | — |
| 46 | 34 | 31 | 22 | PTD2 | KBI1P2 | MISO1 | — | — |
| 47 | 35 | 32 | 23 | PTA3 | KBI0P3 | TXD0 | SCL | — |
| 48 | 36 | 33 | 24 | PTA2[2] | KBI0P2 | RXD0 | SDA | — |
| 49 | 37 | 34 | 25 | PTA1 | KBI0P1 | FTM0CH1 | ACMP1 | ADP1 |
| 50 | 38 | 35 | 26 | PTA0 | KBI0P0 | FTM0CH0 | ACMP0 | ADP0 |
| 51 | 39 | 36 | 27 | PTC7 | — | TxD1 | — | — |
| 52 | 40 | 37 | 28 | PTC6 | — | RxD1 | — | — |
| 53 | 41 | — | — | PTE3 | — | SS0 | — | — |
| 54 | 42 | 38 | — | PTE2 | — | MISO0 | — | — |
| 55 | — | — | — | PTG3 | — | — | — | — |
| 56 | — | — | — | PTG2 | — | — | — | — |
| 57 | — | — | — | PTG1 | — | — | — | — |
| 58 | — | — | — | PTG0 | — | — | — | — |
| 59 | 43 | 39 | — | PTE1[1] | — | MOSI0 | — | — |
| 60 | 44 | 40 | — | PTE0[1] | — | SPSCK0 | TCLK1 | — |
| 61 | 45 | 41 | 29 | PTC5 | — | FTM1CH1 | — | — |
| 62 | 46 | 42 | 30 | PTC4 | — | FTM1CH0 | RTCO | — |
| 63 | 47 | 43 | 31 | PTA5 | IRQ | TCLK0 | — | RESET |
| 64 | 48 | 44 | 32 | PTA4 | — | ACMPO | BKGD | MS |

## 8.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

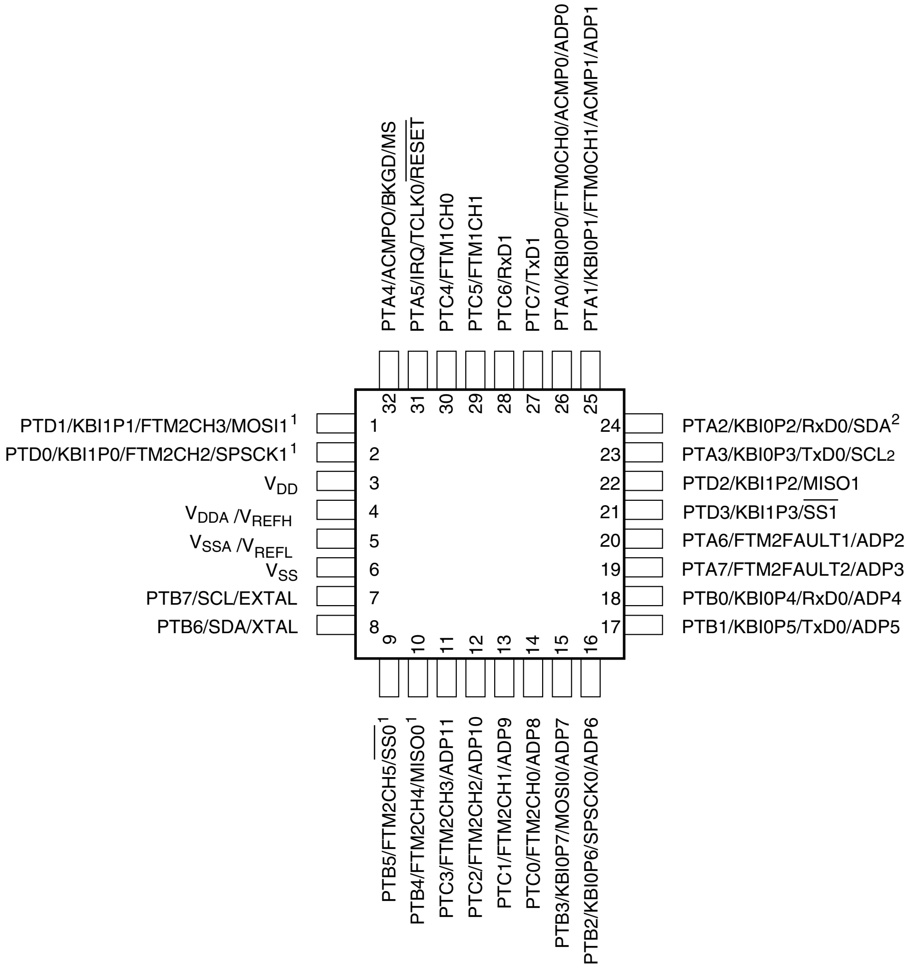
**Figure 17. MC9S08PA60 64-pin QFP and LQFP package**



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

Figure 18. MC9S08PA60 48-pin LQFP package



1. High source/sink current pins
2. True open drain pins

**Figure 20. MC9S08PA60 32-pin LQFP package**

# 9 Revision history

The following table provides a revision history for this document.

**Table 17. Revision history**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 1 | 10/2012 | Initial public release |

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