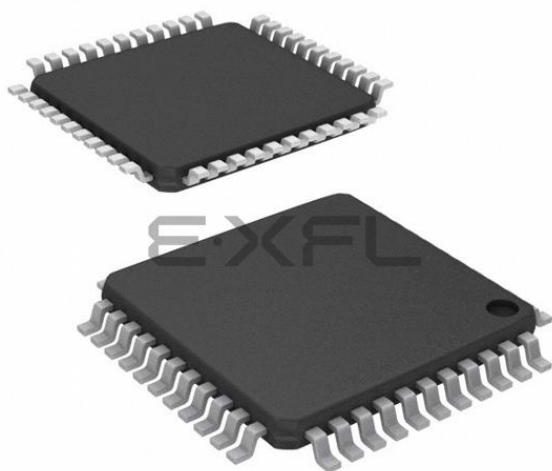




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa60vldr

- Input/Output
 - 57 GPIOs including one output-only pin
 - Two 8-bit keyboard interrupt modules (KBI)
 - Two true open-drain output pins
 - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 64-pin LQFP; 64-pin QFP
 - 48-pin LQFP
 - 44-pin LQFP
 - 32-pin LQFP

Table of Contents

1 Ordering parts.....	4	5.2.1 Control timing.....	13
1.1 Determining valid orderable parts.....	4	5.2.2 Debug trace timing specifications.....	14
2 Part identification.....	4	5.2.3 FTM module timing.....	15
2.1 Description.....	4	5.3 Thermal specifications.....	16
2.2 Format.....	4	5.3.1 Thermal characteristics.....	16
2.3 Fields.....	4	6 Peripheral operating requirements and behaviors.....	17
2.4 Example.....	5	6.1 External oscillator (XOSC) and ICS characteristics.....	17
3 Parameter Classification.....	5	6.2 NVM specifications.....	19
4 Ratings.....	5	6.3 Analog.....	20
4.1 Thermal handling ratings.....	5	6.3.1 ADC characteristics.....	20
4.2 Moisture handling ratings.....	6	6.3.2 Analog comparator (ACMP) electricals.....	23
4.3 ESD handling ratings.....	6	6.4 Communication interfaces.....	24
4.4 Voltage and current operating ratings.....	6	6.4.1 SPI switching specifications.....	24
5 General.....	7	7 Dimensions.....	27
5.1 Nonswitching electrical specifications.....	7	7.1 Obtaining package dimensions.....	27
5.1.1 DC characteristics.....	7	8 Pinout.....	28
5.1.2 Supply current characteristics.....	12	8.1 Signal multiplexing and pin assignments.....	28
5.1.3 EMC performance.....	13	8.2 Device pin assignment.....	31
5.2 Switching specifications.....	13	9 Revision history.....	34

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PA60 and PA32.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PA AA B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	MC = fully qualified, general market flow
9	Memory	
S08	Core	S08 = 8-bit CPU
PA	Device family	PA
AA	Approximate flash size in KB	60 = 60 KB 32 = 32 KB
B	Temperature range (°C)	V = -40 to 105

Table continues on the next page...

Field	Description	Values
CC	Package designator	• QH = 64-pin QFP • LH = 64-pin LQFP • LF = 48-pin LQFP • LD = 44-pin LQFP • LC = 32-pin LQFP

2.4 Example

This is an example part number:

MC9S08PA60VQH

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	–55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

Symbol	Description	Min.	Max.	Unit
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	All I/O pins, low-drive strength	5 V, $I_{load} = -2$ mA	$V_{DD} - 1.5$	—	—	V
	C			3 V, $I_{load} = -0.6$ mA	$V_{DD} - 0.8$	—	—	V
	P	Output high voltage	High current drive pins, high-drive strength	5 V, $I_{load} = -20$ mA	$V_{DD} - 1.5$	—	—	V
	C			3 V, $I_{load} = -6$ mA	$V_{DD} - 0.8$	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-60	
V_{OL}	P	Output low voltage	All I/O pins, low-drive strength	5 V, $I_{load} = 2$ mA	—	—	1.5	V
	C			3 V, $I_{load} = 0.6$ mA	—	—	0.8	V
	P	Output low voltage	High current drive pins, high-drive strength ²	5 V, $I_{load} = 20$ mA	—	—	1.5	V
	C			3 V, $I_{load} = 6$ mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	60	

Table continues on the next page...

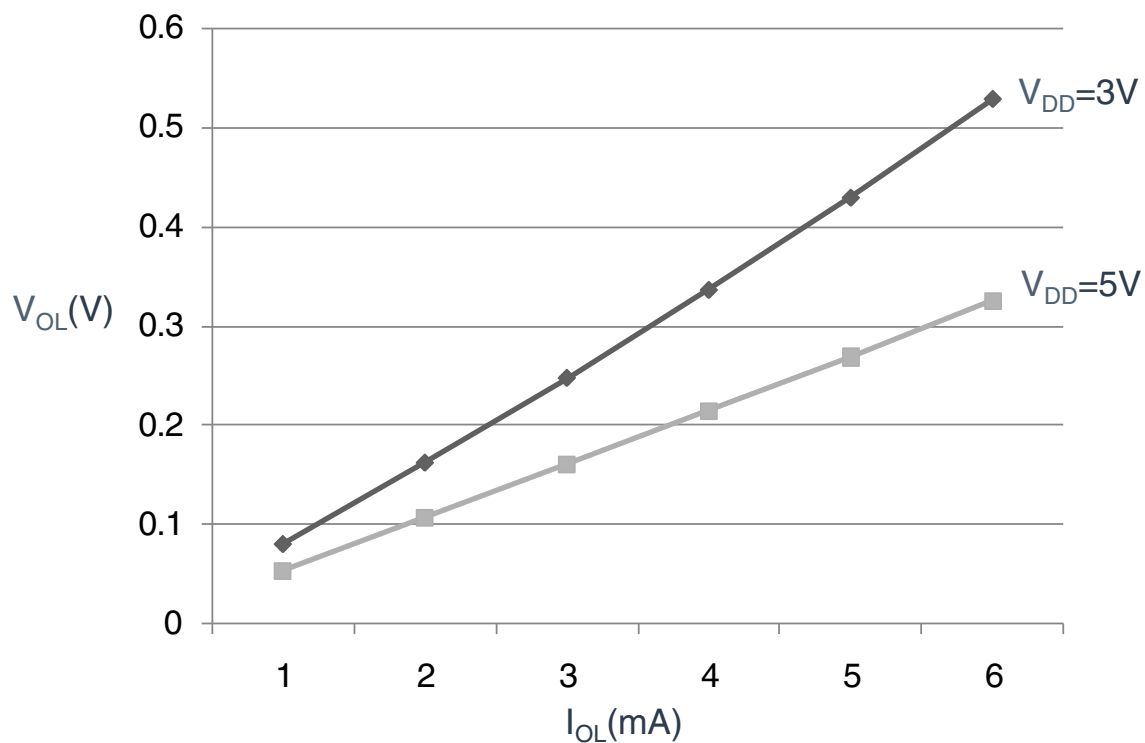


Figure 3. Typical I_{OL} Vs. V_{OL}

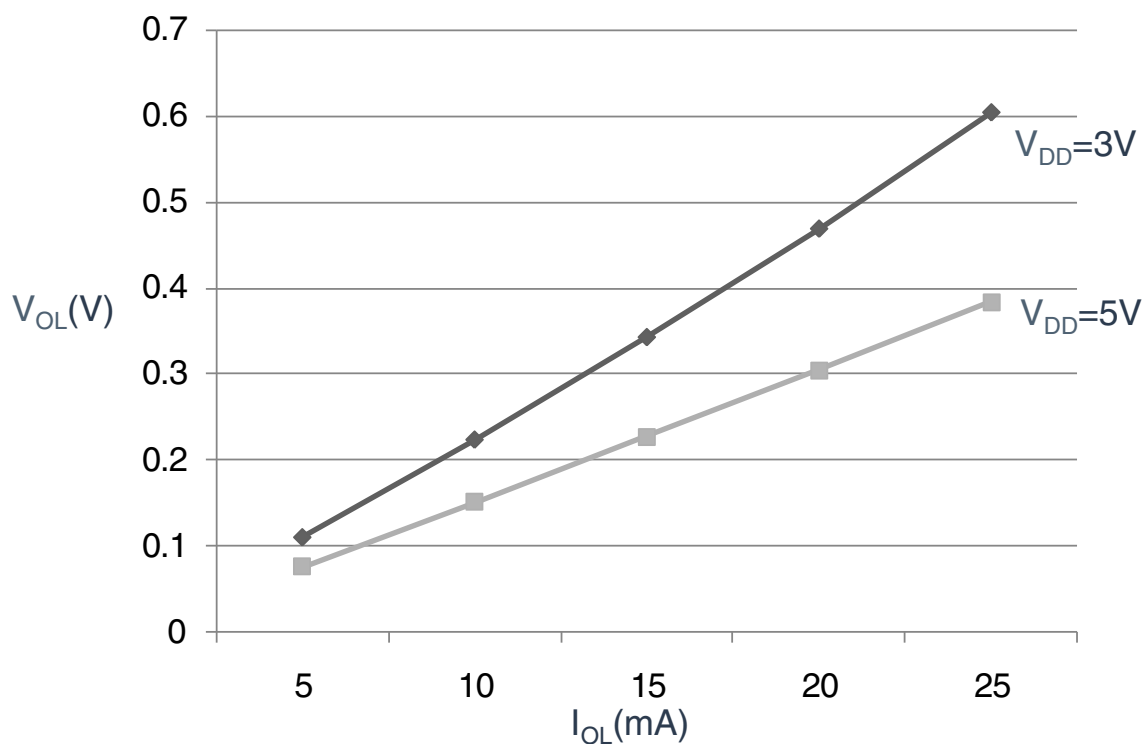


Figure 4. Typical I_{OL} Vs. V_{OL} (High current drive)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI _{DD}	20 MHz	5	12.6	—	mA	-40 to 105 °C
	C			10 MHz		7.2	—		
				1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
				1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI _{DD}	20 MHz	5	10.5	—	mA	-40 to 105 °C
	C			10 MHz		6.2	—		
				1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
				1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI _{DD}	20 MHz	5	12.1	14.8	mA	-40 to 105 °C
	C			10 MHz		6.5	—		
				1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
				1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI _{DD}	20 MHz	5	9.8	12.3	mA	-40 to 105 °C
	C			10 MHz		5.4	—		
				1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
				1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI _{DD}	20 MHz	5	7.8	—	mA	-40 to 105 °C
	C			10 MHz		4.5	—		
				1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
				10 MHz		3.5	—		
				1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock) ^{2, 3}	S3I _{DD}	—	5	3.8	—	μA	-40 to 105 °C
	C			—	3	3	—		-40 to 105 °C

Table continues on the next page...

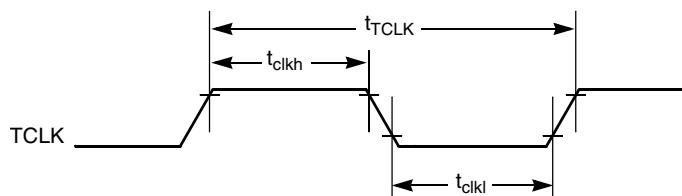


Figure 9. Timer external clock

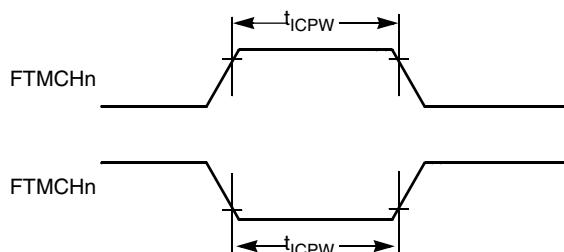


Figure 10. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	-40 to 105	$^{\circ}\text{C}$
Junction temperature range	T_J	-40 to 150	$^{\circ}\text{C}$
Thermal resistance single-layer board			
64-pin LQFP	θ_{JA}	71	$^{\circ}\text{C/W}$
64-pin QFP	θ_{JA}	61	$^{\circ}\text{C/W}$
48-pin LQFP	θ_{JA}	81	$^{\circ}\text{C/W}$
44-pin LQFP	θ_{JA}	75	$^{\circ}\text{C/W}$
32-pin LQFP	θ_{JA}	86	$^{\circ}\text{C/W}$

Table continues on the next page...

Table 8. Thermal characteristics (continued)

Rating	Symbol	Value	Unit
Thermal resistance four-layer board			
64-pin LQFP	θ_{JA}	53	°C/W
64-pin QFP	θ_{JA}	47	°C/W
48-pin LQFP	θ_{JA}	57	°C/W
44-pin LQFP	θ_{JA}	53	°C/W
32-pin LQFP	θ_{JA}	57	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$$P_D = P_{int} + P_{I/O}$$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273 \text{ °C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ °C}) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A .

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 9. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)

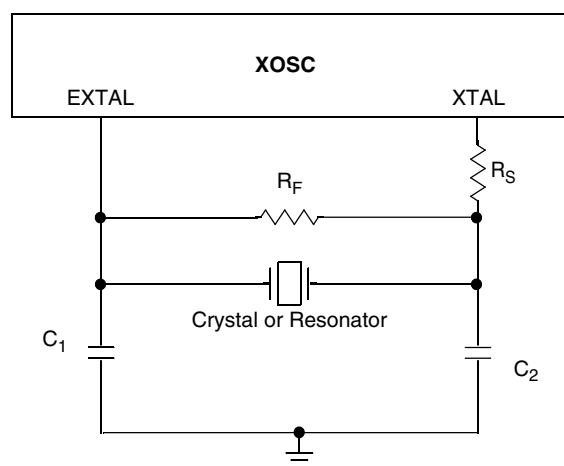
Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	32	—	40	kHz
	C		High range (RANGE = 1) FEE or FBE mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note ³			
3	D	Feedback resistor	Low Frequency, Low-Power Mode	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 KHz crystal; High range = 20 MHz crystal, ⁶	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode ²	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	32.768	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency ⁵	Over full voltage and temperature range	Δf_{dco_t}	—	—	±2.0	% f_{dco}
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time ^{5, 7}		$t_{Acquire}$	—	—	2	ms

Table continues on the next page...

**Table 9. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)
(continued)**

Num	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸	C_{Jitter}	—	0.02	0.2	% f_{dco}

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

**Figure 11. Typical crystal or resonator circuit**

6.2 NVM specifications

This section provides details about program/erase times and program-erase endurance for the flash and EEPROM memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	Supply voltage for program/erase -40 °C to 105 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V

Table continues on the next page...

Table 10. Flash characteristics (continued)

C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	NVM Bus frequency	f _{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f _{NVMOP}	0.8	—	1.05	MHz
D	Erase Verify All Blocks	t _{VFYALL}	—	—	17030	t _{cyc}
D	Erase Verify Flash Block	t _{RD1BLK}	—	—	16977	t _{cyc}
D	Erase Verify EEPROM Block	t _{RD1BLK}	—	—	843	t _{cyc}
D	Erase Verify Flash Section	t _{RD1SEC}	—	—	517	t _{cyc}
D	Erase Verify EEPROM Section	t _{DRD1SEC}	0.10	0.10	0.11	ms
D	Read Once	t _{RDONCE}	—	—	455	t _{cyc}
D	Program Flash (2 word)	t _{PGM2}	0.12	0.12	0.14	ms
D	Program Flash (4 word)	t _{PGM4}	0.20	0.21	0.24	ms
D	Program Once	t _{PGMONCE}	0.20	0.21	0.24	ms
D	Program EEPROM (1 Byte)	t _{DPGM1}	0.02	0.02	0.02	ms
D	Program EEPROM (2 Byte)	t _{DPGM2}	0.17	0.18	0.20	ms
D	Erase All Blocks	t _{ERSALL}	96.01	100.78	125.80	ms
D	Erase Flash Block	t _{ERSBLK}	95.98	100.75	125.76	ms
D	Erase Flash Sector	t _{ERSPG}	19.10	20.05	25.05	ms
D	Erase EEPROM Sector	t _{DERSPG}	4.81	5.05	6.30	ms
D	Unsecure Flash	t _{UNSECU}	96.01	100.78	125.80	ms
D	Verify Backdoor Access Key	t _{VFYKEY}	—	—	469	t _{cyc}
D	Set User Margin Level	t _{MLOADU}	—	—	442	t _{cyc}
C	FLASH Program/erase endurance T _L to T _H = -40 °C to 105 °C	n _{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance T _L to T _H = -40 °C to 105 °C	n _{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T _{Javg} = 85°C after up to 10,000 program/erase cycles	t _{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}

3. Maximum times are based on minimum f_{NVMOP} and maximum f_{NVMBUS}

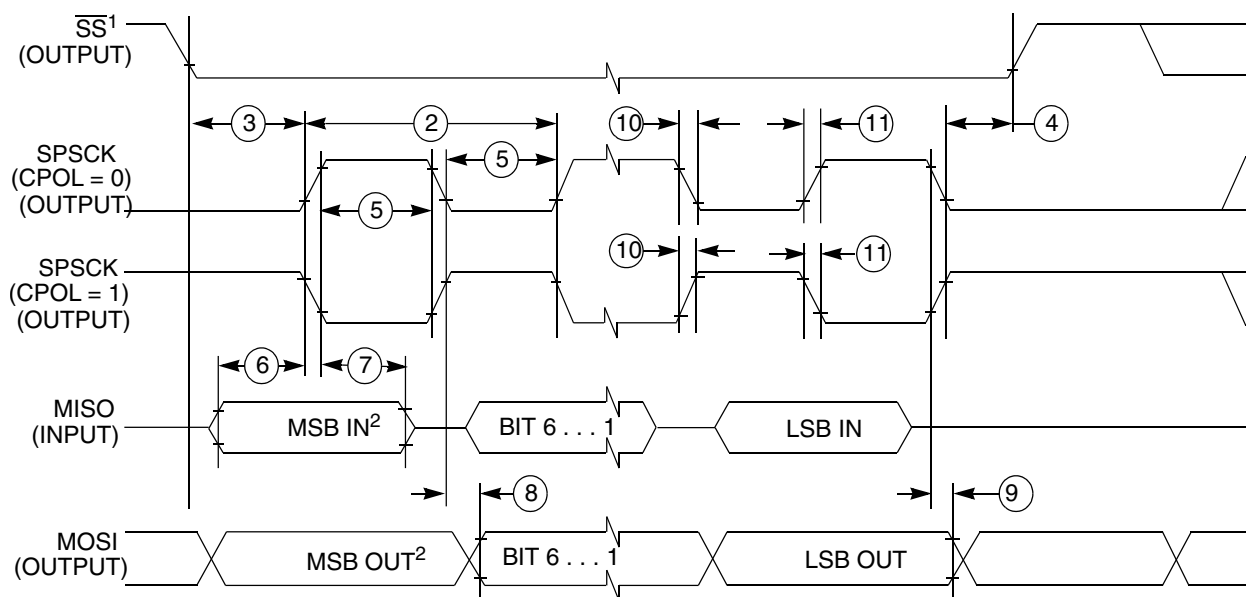
4. t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

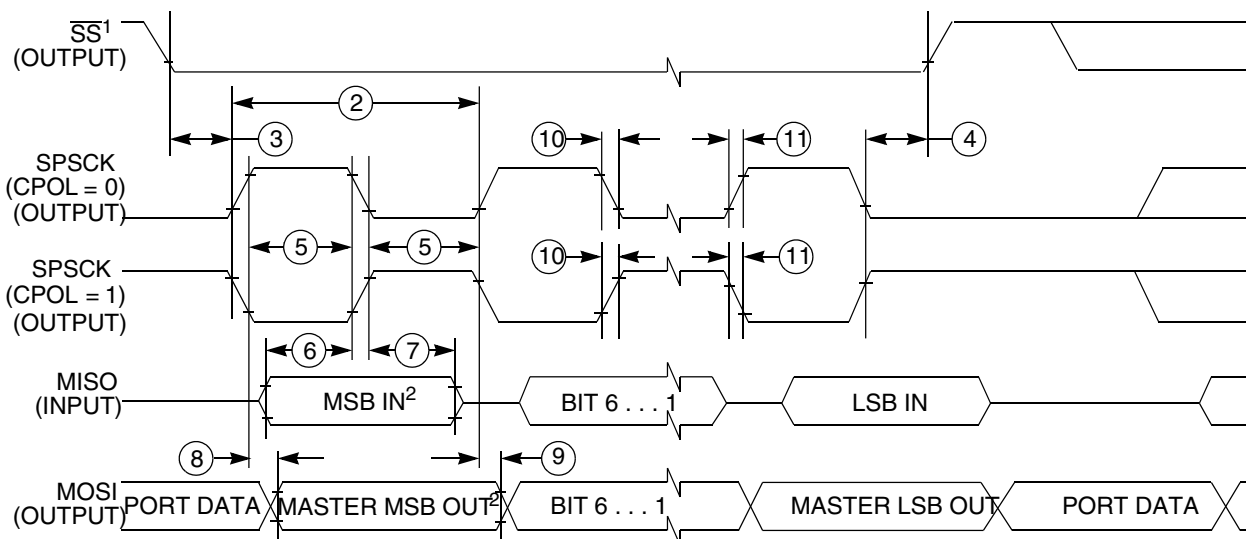
6.3 Analog

Table 14. SPI master mode timing (continued)

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
10	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

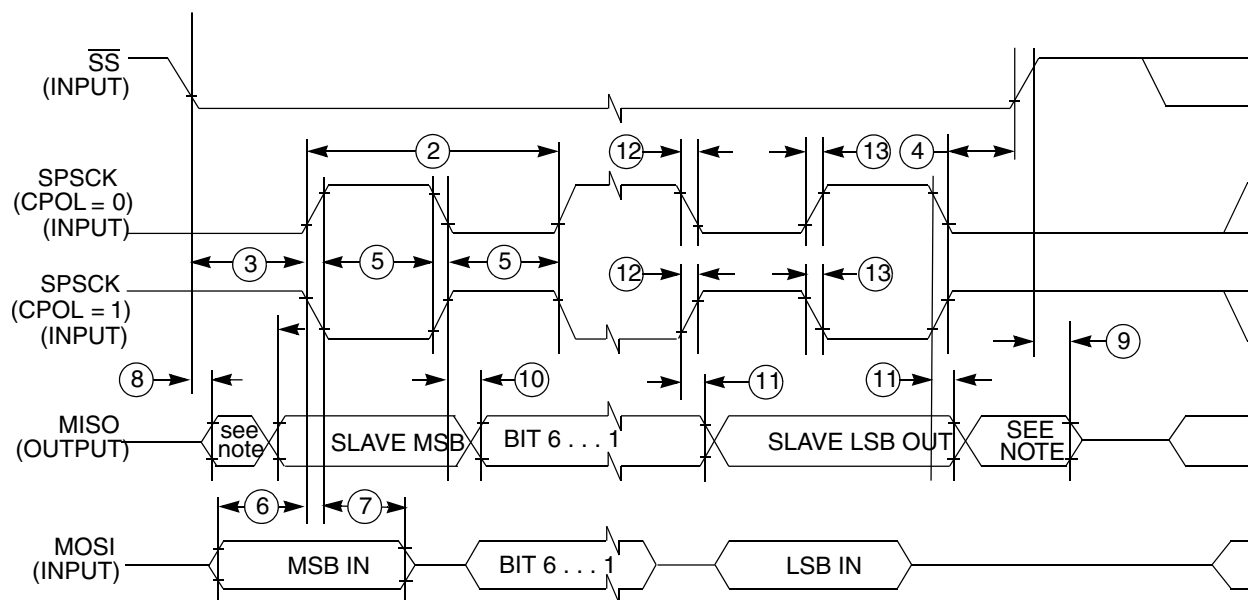
Figure 13. SPI master mode timing (CPHA=0)

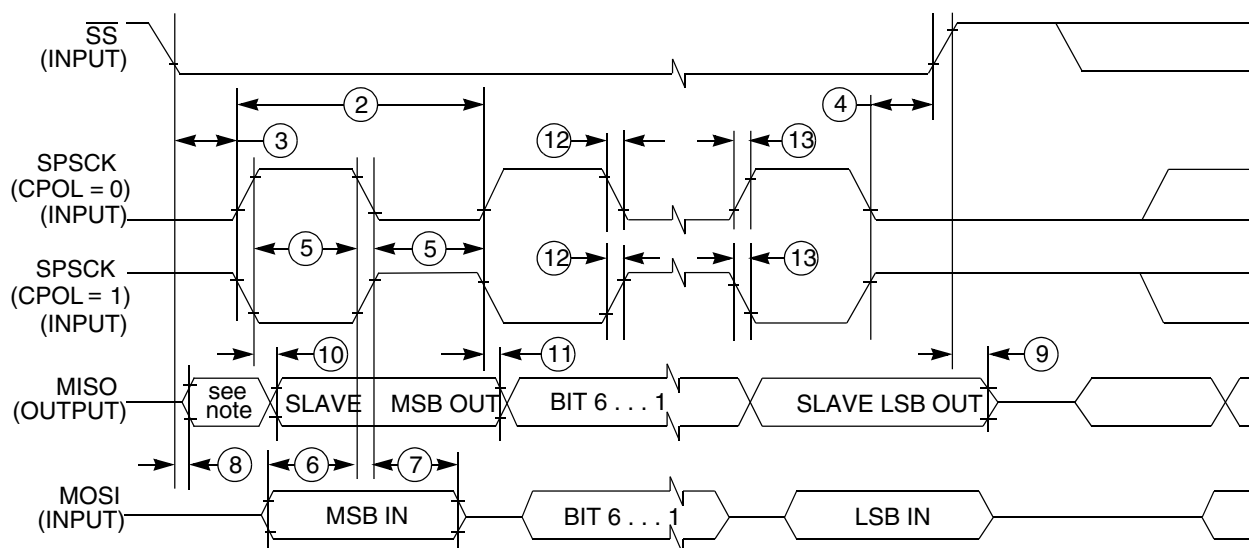
1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA=1)

Table 15. SPI slave mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

**Figure 15. SPI slave mode timing (CPHA = 0)**



NOTE: Not defined!

Figure 16. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
44-pin LQFP	98ASS23225W
48-pin LQFP	98ASH00962A
64-pin QFP	98ASB42844B
64-pin LQFP	98ASS23234W

Table 16. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
28	—	—	—	PTF6	—	—	ADP14	—
29	—	—	—	PTF5	—	—	ADP13	—
30	—	—	—	PTF4	—	—	ADP12	—
31	23	21	15	PTB3	KBI0P7	MOSI0	ADP7	—
32	24	22	16	PTB2	KBI0P6	SPSCK0	ADP6	—
33	25	23	17	PTB1	KBI0P5	TXD0	ADP5	—
34	26	24	18	PTB0	KBI0P4	RXD0	ADP4	—
35	—	—	—	PTF3	—	—	—	—
36	—	—	—	PTF2	—	—	—	—
37	27	25	19	PTA7	FTM2FAULT2	—	ADP3	—
38	28	26	20	PTA6	FTM2FAULT1	—	ADP2	—
39	29	—	—	PTE4	—	—	—	—
40	30	27	—	—	—	—	—	V _{SS}
41	31	28	—	—	—	—	—	V _{DD}
42	—	—	—	PTF1	—	—	—	—
43	—	—	—	PTF0	—	—	—	—
44	32	29	—	PTD4	KBI1P4	—	—	—
45	33	30	21	PTD3	KBI1P3	SS1	—	—
46	34	31	22	PTD2	KBI1P2	MISO1	—	—
47	35	32	23	PTA3	KBI0P3	TXD0	SCL	—
48	36	33	24	PTA2 ²	KBI0P2	RXD0	SDA	—
49	37	34	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	38	35	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	39	36	27	PTC7	—	TxD1	—	—
52	40	37	28	PTC6	—	RxD1	—	—
53	41	—	—	PTE3	—	SS0	—	—
54	42	38	—	PTE2	—	MISO0	—	—
55	—	—	—	PTG3	—	—	—	—
56	—	—	—	PTG2	—	—	—	—
57	—	—	—	PTG1	—	—	—	—
58	—	—	—	PTG0	—	—	—	—
59	43	39	—	PTE1 ¹	—	MOSI0	—	—
60	44	40	—	PTE0 ¹	—	SPSCK0	TCLK1	—
61	45	41	29	PTC5	—	FTM1CH1	—	—
62	46	42	30	PTC4	—	FTM1CH0	RTCO	—
63	47	43	31	PTA5	IRQ	TCLK0	—	RESET
64	48	44	32	PTA4	—	ACMPO	BKGD	MS

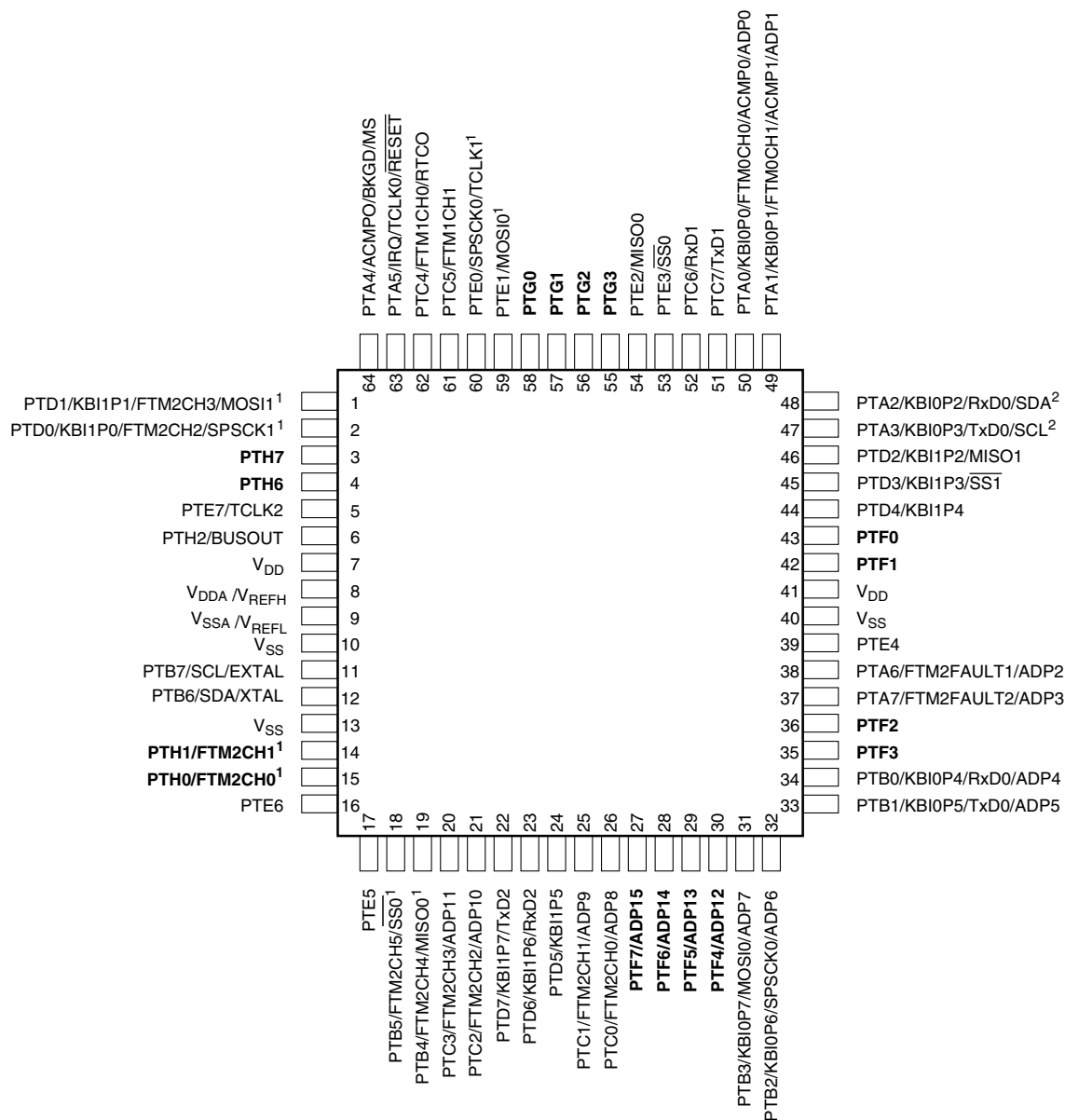
Pinout

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment

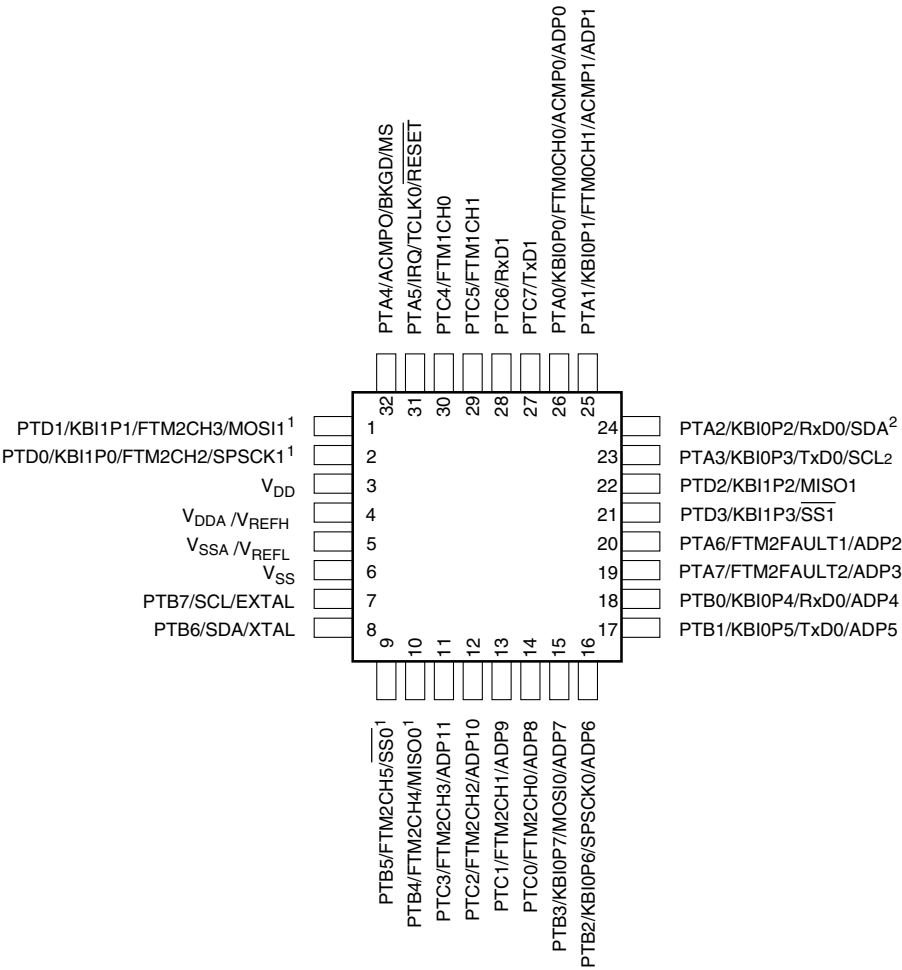


Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

2. True open drain pins

Figure 17. MC9S08PA60 64-pin QFP and LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 20. MC9S08PA60 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 17. Revision history

Rev. No.	Date	Substantial Changes
1	10/2012	Initial public release

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductors products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claims alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics as their non-RoHS-complaint and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2011–2012 Freescale Semiconductor, Inc.