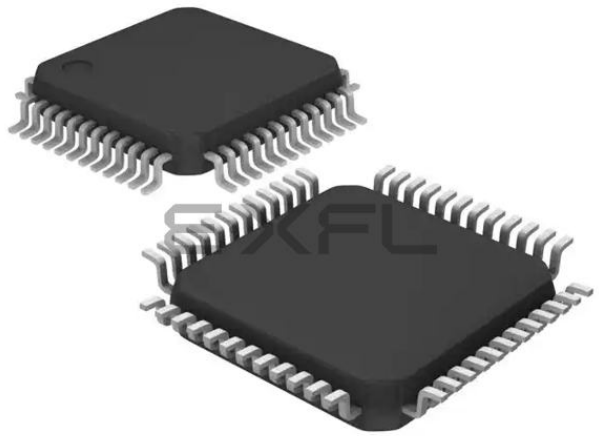

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa60vlfr

- Input/Output
  - 57 GPIOs including one output-only pin
  - Two 8-bit keyboard interrupt modules (KBI)
  - Two true open-drain output pins
  - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
  - 64-pin LQFP; 64-pin QFP
  - 48-pin LQFP
  - 44-pin LQFP
  - 32-pin LQFP

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PA60 and PA32.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PA AA B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	• MC = fully qualified, general market flow
9	Memory	
S08	Core	• S08 = 8-bit CPU
PA	Device family	• PA
AA	Approximate flash size in KB	• 60 = 60 KB • 32 = 32 KB
B	Temperature range (°C)	• V = –40 to 105

Table continues on the next page...

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	–0.3	5.8	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	All I/O pins, low-drive strength	5 V, I_{load} = -2 mA	V_{DD} - 1.5	—	—	V
	C			3 V, I_{load} = -0.6 mA	V_{DD} - 0.8	—	—	V
	P		High current drive pins, high-drive strength	5 V, I_{load} = -20 mA	V_{DD} - 1.5	—	—	V
	C			3 V, I_{load} = -6 mA	V_{DD} - 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-60	
V_{OL}	P	Output low voltage	All I/O pins, low-drive strength	5 V, I_{load} = 2 mA	—	—	1.5	V
	C			3 V, I_{load} = 0.6 mA	—	—	0.8	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	1.5	V
	C			3 V, I_{load} = 6 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	60	

Table continues on the next page...

Table 3. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V_{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

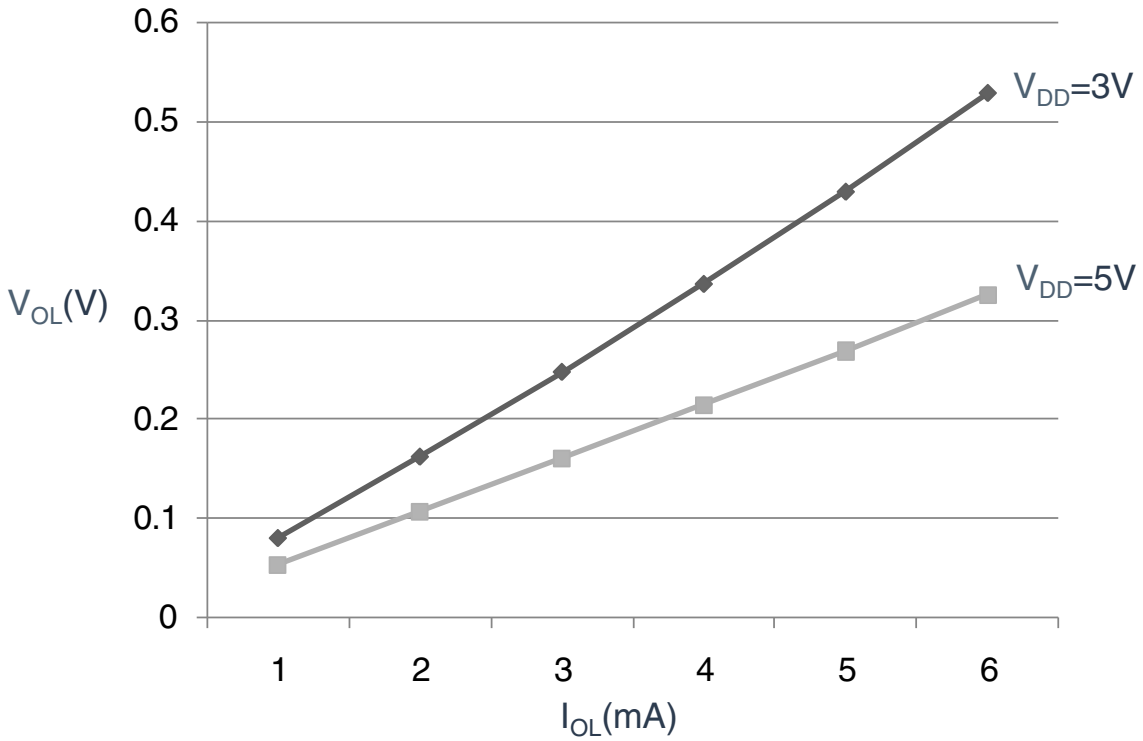


Figure 3. Typical I_{OL} Vs. V_{OL}

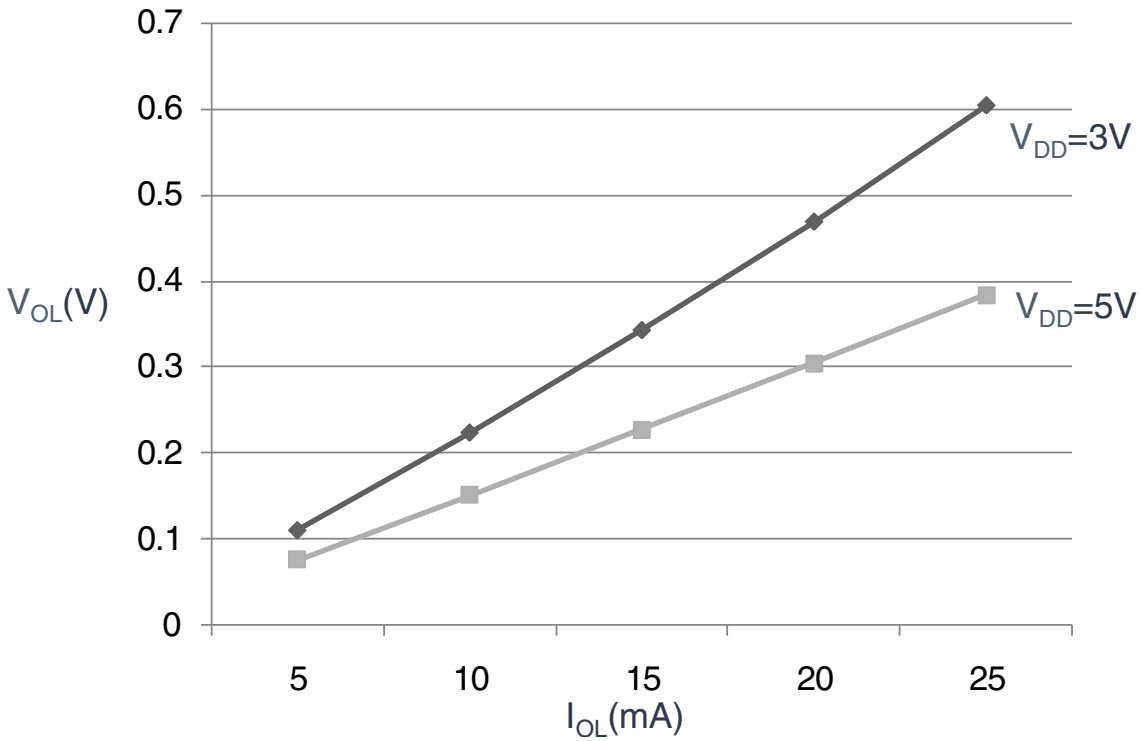


Figure 4. Typical I_{OL} Vs. V_{OL} (High current drive)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	12.6	—	mA	-40 to 105 °C
	C			10 MHz		7.2	—		
				1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
				1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI_{DD}	20 MHz	5	10.5	—	mA	-40 to 105 °C
	C			10 MHz		6.2	—		
				1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
				1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	12.1	14.8	mA	-40 to 105 °C
	C			10 MHz		6.5	—		
				1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
				1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI_{DD}	20 MHz	5	9.8	12.3	mA	-40 to 105 °C
	C			10 MHz		5.4	—		
				1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
				1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	7.8	—	mA	-40 to 105 °C
	C			10 MHz		4.5	—		
				1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
				10 MHz		3.5	—		
				1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	3.8	—	µA	-40 to 105 °C
	C			—	3	3	—		-40 to 105 °C

Table continues on the next page...

Table 6. Debug trace operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

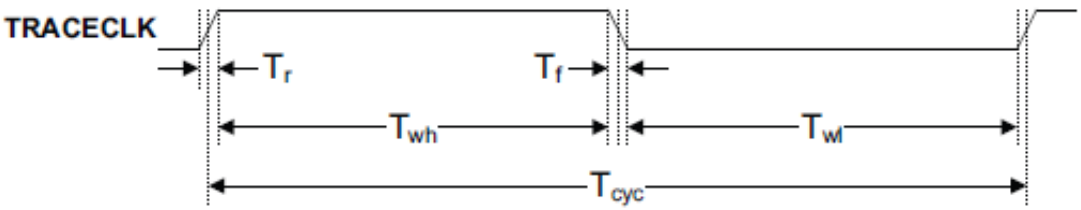


Figure 7. TRACE_CLKOUT specifications

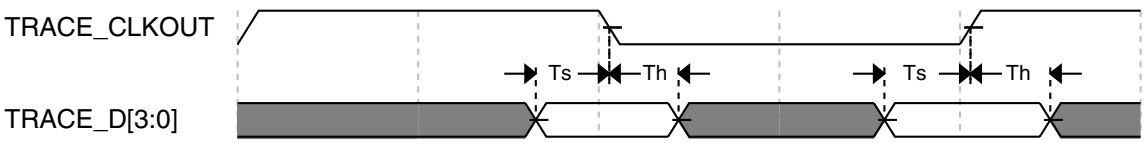


Figure 8. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 7. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

Table 8. Thermal characteristics (continued)

Rating	Symbol	Value	Unit
Thermal resistance four-layer board			
64-pin LQFP	θ_{JA}	53	°C/W
64-pin QFP	θ_{JA}	47	°C/W
48-pin LQFP	θ_{JA}	57	°C/W
44-pin LQFP	θ_{JA}	53	°C/W
32-pin LQFP	θ_{JA}	57	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 9. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	32	—	40	kHz
	C		High range (RANGE = 1) FEE or FBE mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note[3]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [4]	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[4]	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 KHz crystal; High range = 20 MHz crystal, [6]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	D	Square wave input clock frequency	FEE or FBE mode[2]	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	32.768	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency[5]	Over full voltage and temperature range	Δf_{dco_t}	—	—	±2.0	$\%f_{dco}$
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time[5, 7]		$t_{Acquire}$	—	—	2	ms

Table continues on the next page...

Table 10. Flash characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	—	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17030	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16977	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	843	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	517	t_{cyc}
D	Erase Verify EEPROM Section	$t_{DRD1SEC}$	0.10	0.10	0.11	ms
D	Read Once	t_{RDONCE}	—	—	455	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.14	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.24	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.24	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.02	0.02	0.02	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.20	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	125.80	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	125.76	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	25.05	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	6.30	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	125.80	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	469	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	442	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimun times are based on maxmum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on minimum f_{NVMOP} and maximum f_{NVMBUS}
4. t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

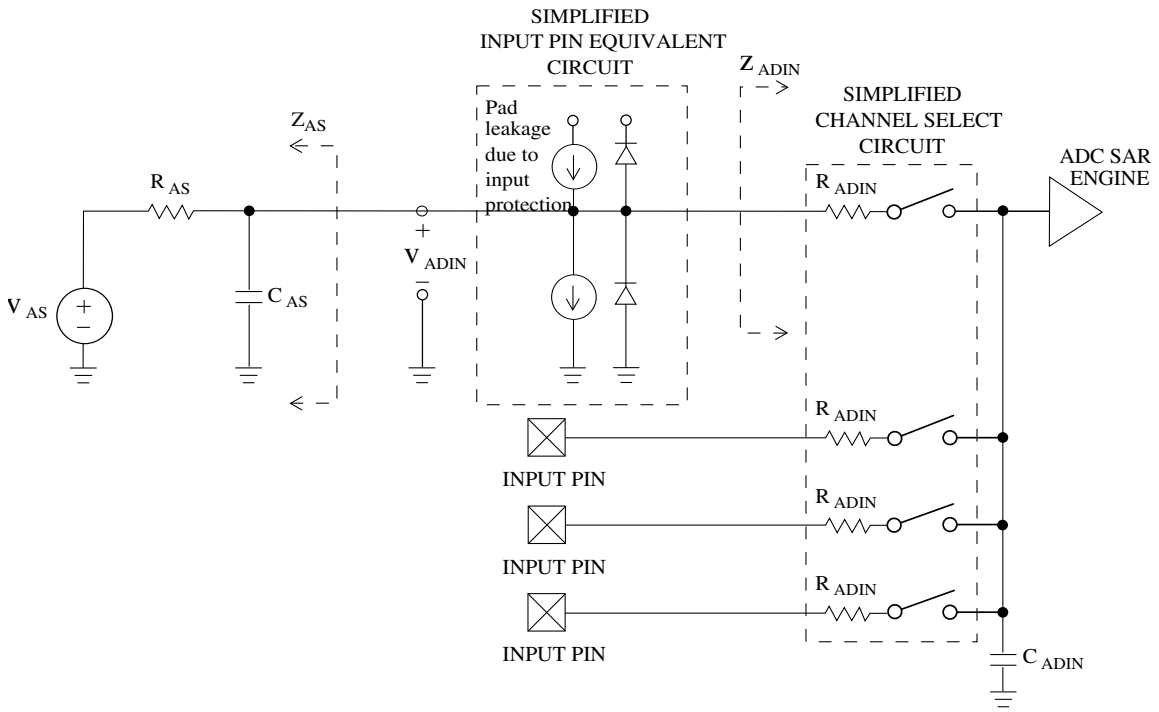


Figure 12. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA

Table continues on the next page...

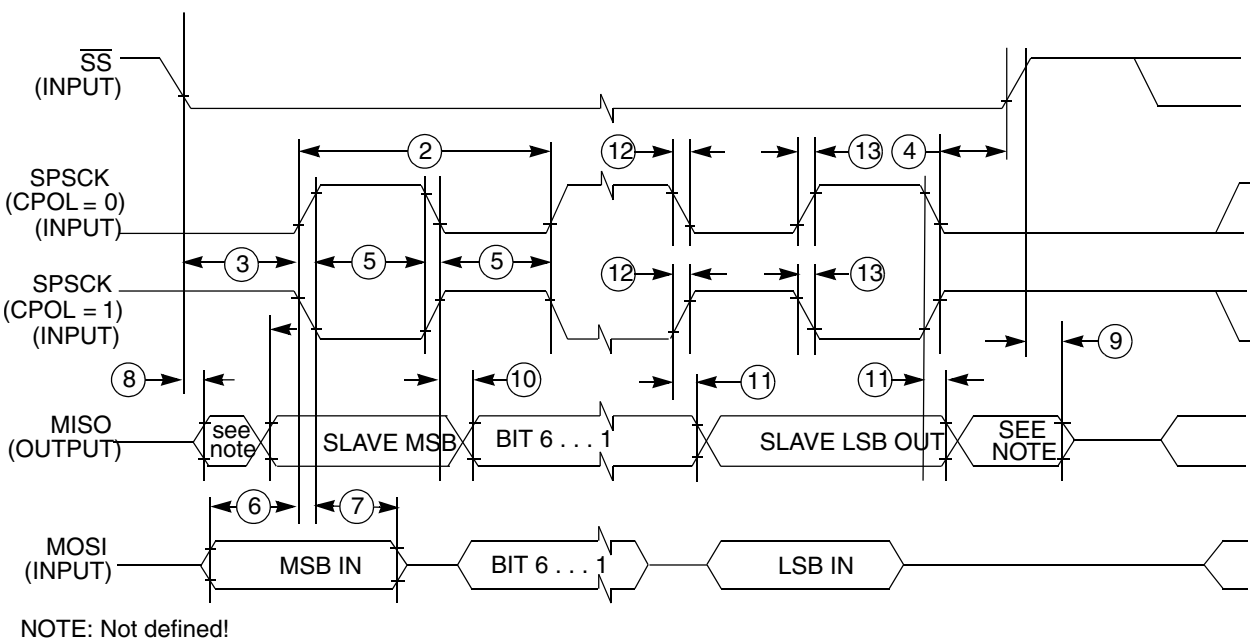
Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Liniarity	12-bit mode	T	DNL	—	±1.0	—	LSB[2]
	10-bit mode	P		—	±0.25	±0.5	
	8-bit mode[3]	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB[2]
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB[2]
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error[5]	12-bit mode	T	E_{FS}	—	±2.5	—	LSB[2]
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[2]
Input leakage error[6]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. 1 LSB = (V_{REFH} - V_{REFL})/2^N
3. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
3. V_{ADIN} = V_{DDA}
4. I_{In} = leakage current (refer to DC characteristics)

Table 15. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

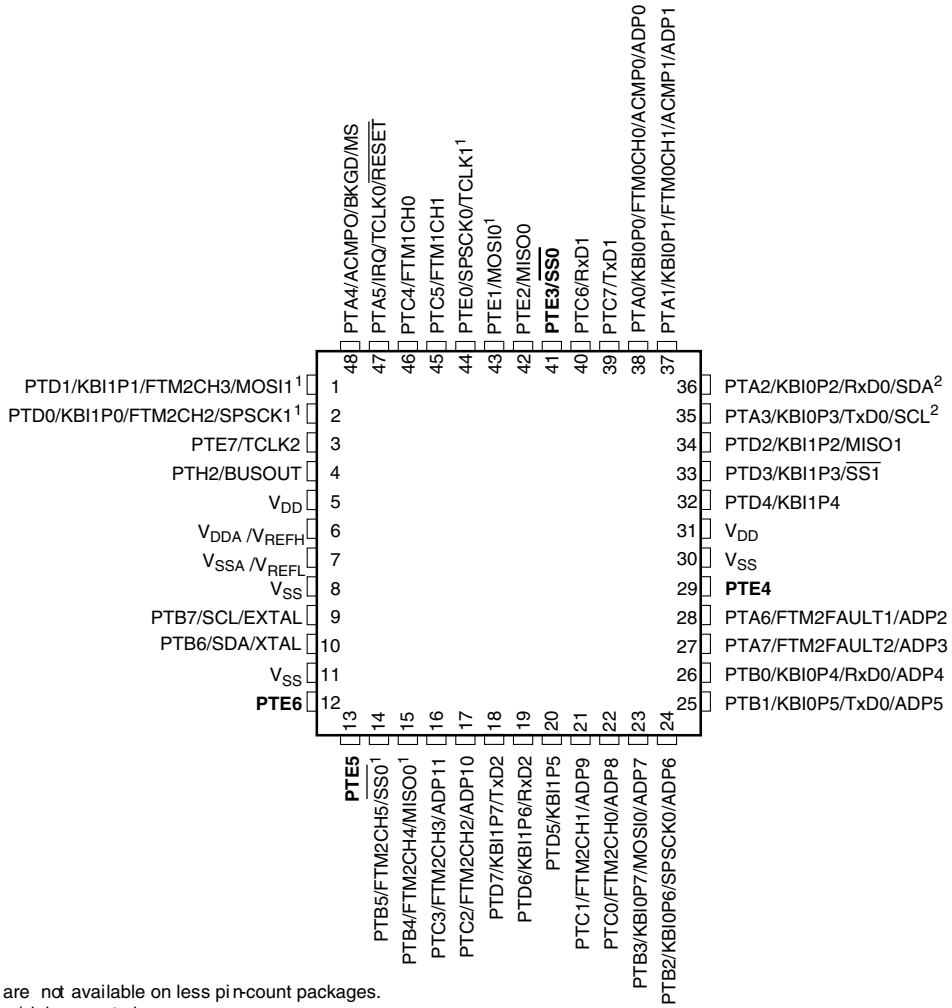


NOTE: Not defined!

Figure 15. SPI slave mode timing (CPHA = 0)

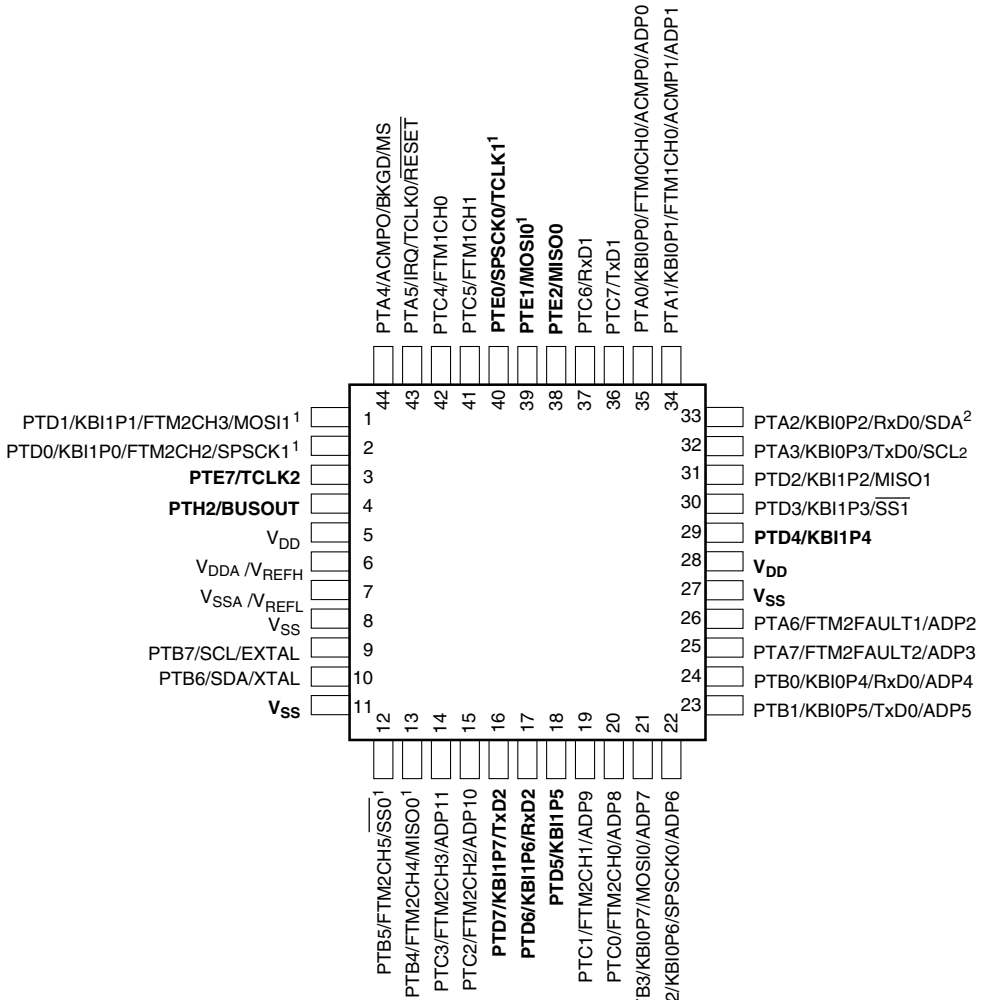
Table 16. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
28	—	—	—	PTF6	—	—	ADP14	—
29	—	—	—	PTF5	—	—	ADP13	—
30	—	—	—	PTF4	—	—	ADP12	—
31	23	21	15	PTB3	KBI0P7	MOSI0	ADP7	—
32	24	22	16	PTB2	KBI0P6	SPSCK0	ADP6	—
33	25	23	17	PTB1	KBI0P5	TXD0	ADP5	—
34	26	24	18	PTB0	KBI0P4	RXD0	ADP4	—
35	—	—	—	PTF3	—	—	—	—
36	—	—	—	PTF2	—	—	—	—
37	27	25	19	PTA7	FTM2FAULT2	—	ADP3	—
38	28	26	20	PTA6	FTM2FAULT1	—	ADP2	—
39	29	—	—	PTE4	—	—	—	—
40	30	27	—	—	—	—	—	V_{SS}
41	31	28	—	—	—	—	—	V_{DD}
42	—	—	—	PTF1	—	—	—	—
43	—	—	—	PTF0	—	—	—	—
44	32	29	—	PTD4	KBI1P4	—	—	—
45	33	30	21	PTD3	KBI1P3	SS1	—	—
46	34	31	22	PTD2	KBI1P2	MISO1	—	—
47	35	32	23	PTA3	KBI0P3	TXD0	SCL	—
48	36	33	24	PTA2[2]	KBI0P2	RXD0	SDA	—
49	37	34	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	38	35	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	39	36	27	PTC7	—	TxD1	—	—
52	40	37	28	PTC6	—	RxD1	—	—
53	41	—	—	PTE3	—	SS0	—	—
54	42	38	—	PTE2	—	MISO0	—	—
55	—	—	—	PTG3	—	—	—	—
56	—	—	—	PTG2	—	—	—	—
57	—	—	—	PTG1	—	—	—	—
58	—	—	—	PTG0	—	—	—	—
59	43	39	—	PTE1[1]	—	MOSI0	—	—
60	44	40	—	PTE0[1]	—	SPSCK0	TCLK1	—
61	45	41	29	PTC5	—	FTM1CH1	—	—
62	46	42	30	PTC4	—	FTM1CH0	RTCO	—
63	47	43	31	PTA5	IRQ	TCLK0	—	RESET
64	48	44	32	PTA4	—	ACMPO	BKGD	MS



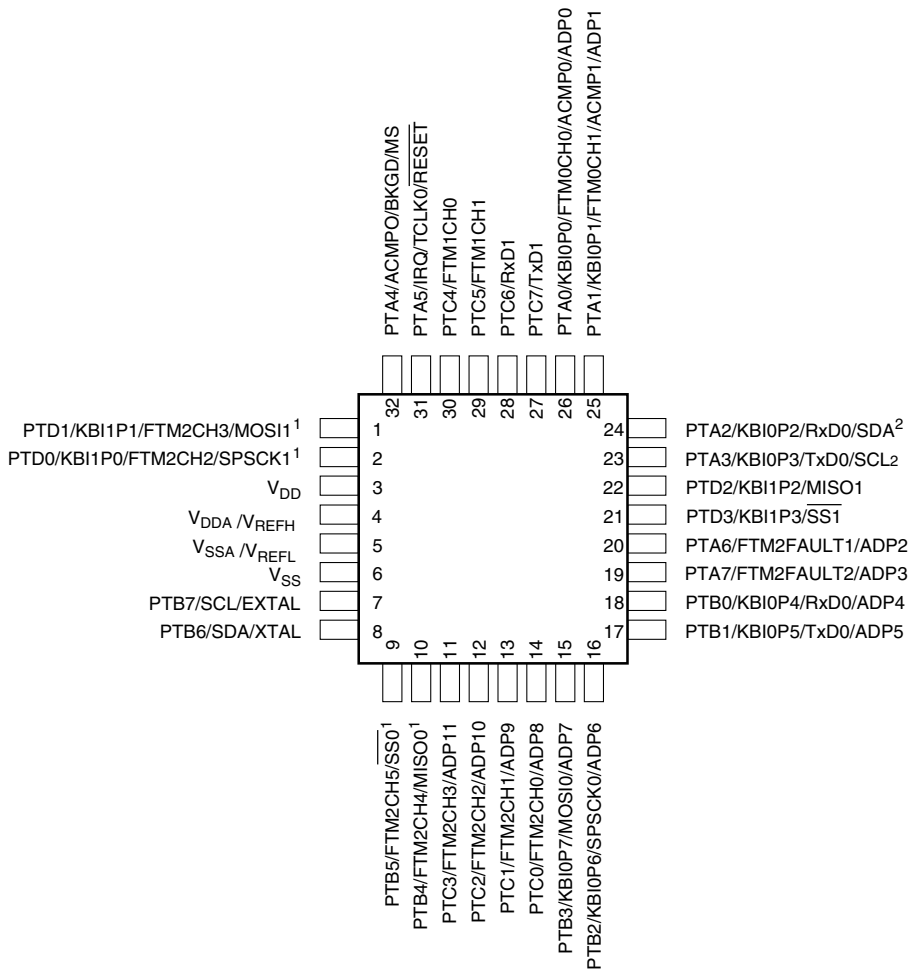
Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 18. MC9S08PA60 48-pin LQFP package



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 19. MC9S08PA60 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 20. MC9S08PA60 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 17. Revision history

Rev. No.	Date	Substantial Changes
1	10/2012	Initial public release

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Document Number: MC9S08PA60
Rev. 1, 10/9/2012