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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pa60vlh

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PA60 and PA32.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PA AA B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	• MC = fully qualified, general market flow
9	Memory	
S08	Core	• S08 = 8-bit CPU
PA	Device family	• PA
AA	Approximate flash size in KB	• 60 = 60 KB • 32 = 32 KB
B	Temperature range (°C)	• V = –40 to 105

Table continues on the next page...

Field	Description	Values
CC	Package designator	• QH = 64-pin QFP • LH = 64-pin LQFP • LF = 48-pin LQFP • LD = 44-pin LQFP • LC = 32-pin LQFP

2.4 Example

This is an example part number:

MC9S08PA60VQH

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

Symbol	Description	Min.	Max.	Unit
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	All I/O pins, low-drive strength	5 V, I_{load} = -2 mA	V_{DD} - 1.5	—	—	V
	C			3 V, I_{load} = -0.6 mA	V_{DD} - 0.8	—	—	V
	P		High current drive pins, high-drive strength	5 V, I_{load} = -20 mA	V_{DD} - 1.5	—	—	V
	C			3 V, I_{load} = -6 mA	V_{DD} - 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-60	
V_{OL}	P	Output low voltage	All I/O pins, low-drive strength	5 V, I_{load} = 2 mA	—	—	1.5	V
	C			3 V, I_{load} = 0.6 mA	—	—	0.8	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	1.5	V
	C			3 V, I_{load} = 6 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	60	

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
V_{IH}	P	Input high voltage	All digital inputs	V_{DD}>4.1V	0.70 × V_{DD}	—	—	V
				V_{DD}>2.7V	0.85 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DD}>4.1V	—	—	0.35 × V_{DD}	V
				V_{DD}>2.7V	—	—	0.30 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\lvert I_{In}\rvert$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZ}\rvert$	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZTOT}\rvert$	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DD} or V_{SS}	—	—	2	µA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA5/ IRQ/TCLK/RESET	—	17.5	—	52.5	kΩ
R_{PU}[3]	P	Pullup resistors	PTA5/IRQ/TCLK/ RESET	—	17.5	—	52.5	kΩ
I_{IC}	D	DC injection current[4, 5, 6]	Single pin limit	V_{IN} < V_{SS}, V_{IN} > V_{DD}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	8	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA5, are internally clamped to V_{SS} and V_{DD}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current (V_{In} > V_{DD}) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description	Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1]	1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1)[2]	4.2	4.3	4.4	V

Table continues on the next page...

Table 3. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V_{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

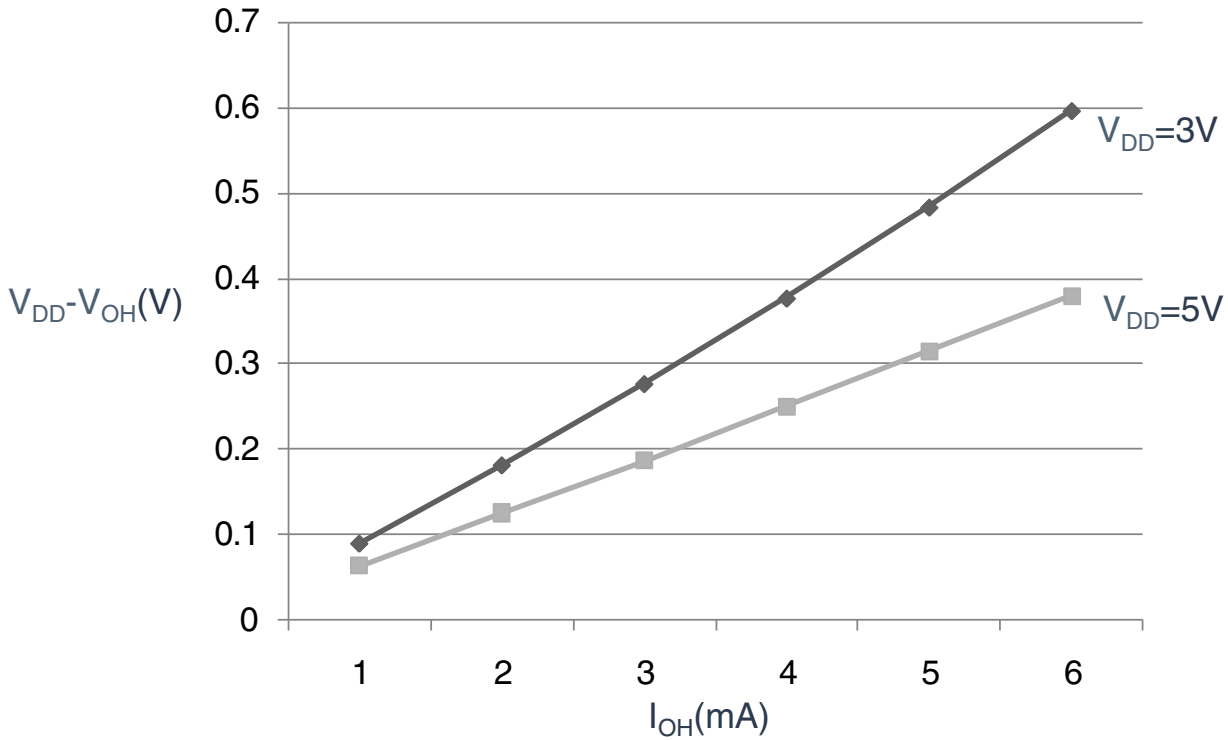


Figure 1. Typical I_{OH} Vs. V_{DD}-V_{OH}

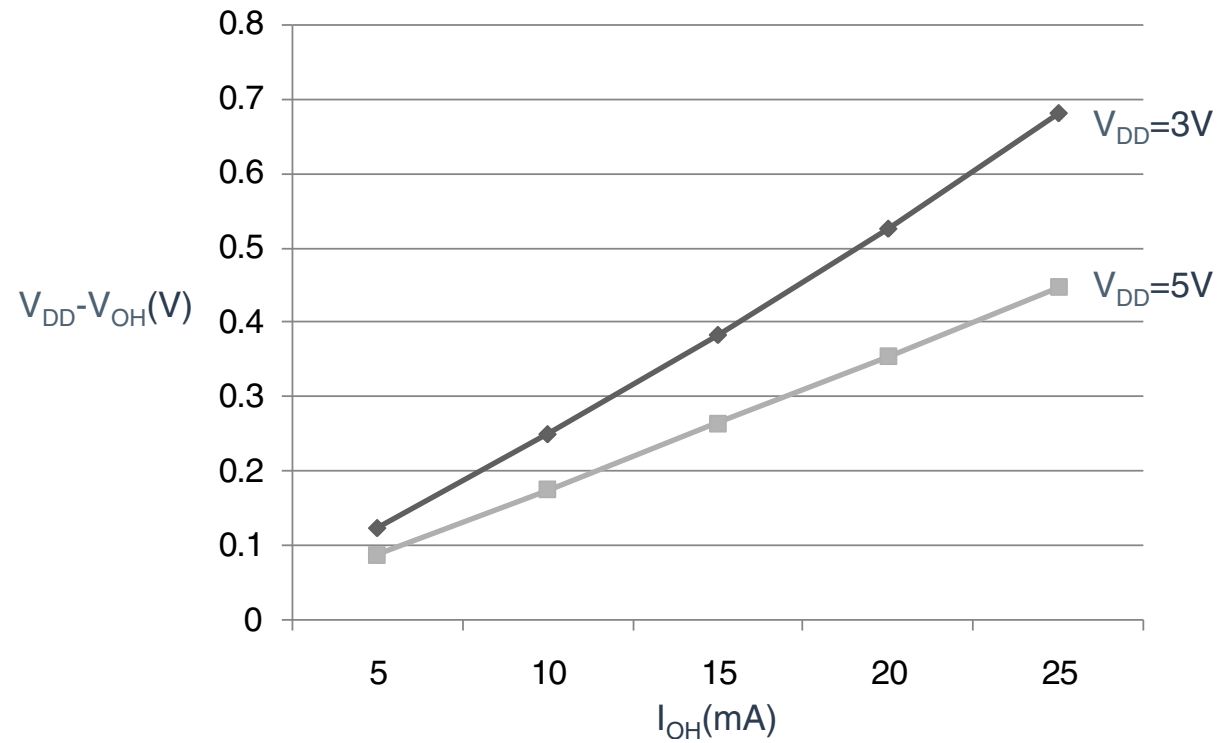


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (High current drive)

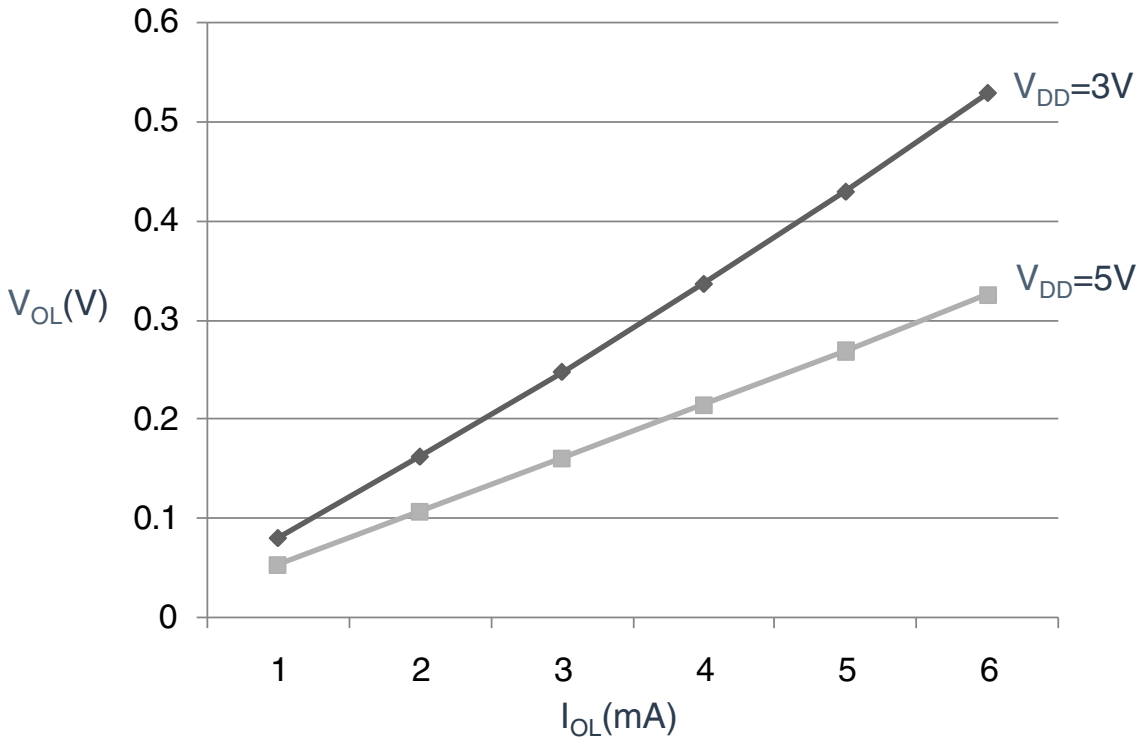


Figure 3. Typical I_{OL} Vs. V_{OL}

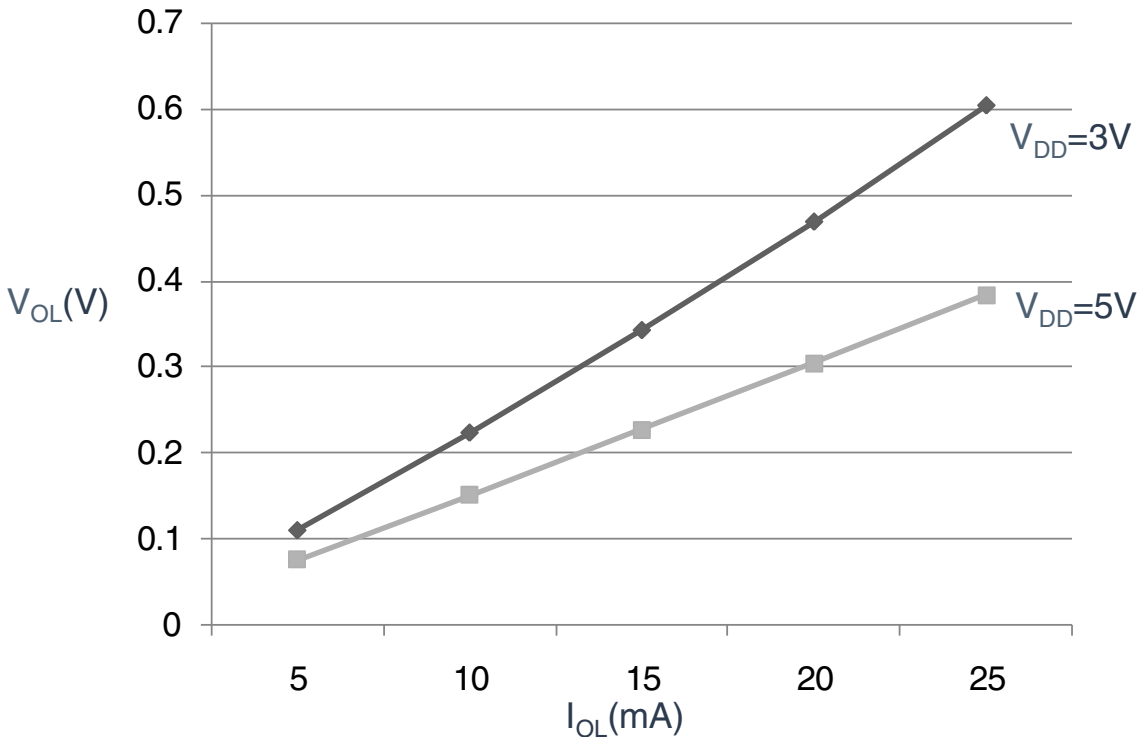


Figure 4. Typical I_{OL} Vs. V_{OL} (High current drive)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	12.6	—	mA	-40 to 105 °C
	C			10 MHz		7.2	—		
				1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
				1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI_{DD}	20 MHz	5	10.5	—	mA	-40 to 105 °C
	C			10 MHz		6.2	—		
				1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
				1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	12.1	14.8	mA	-40 to 105 °C
	C			10 MHz		6.5	—		
				1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
				1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI_{DD}	20 MHz	5	9.8	12.3	mA	-40 to 105 °C
	C			10 MHz		5.4	—		
				1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
				1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	7.8	—	mA	-40 to 105 °C
	C			10 MHz		4.5	—		
				1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
				10 MHz		3.5	—		
				1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	3.8	—	µA	-40 to 105 °C
	C			—	3	3	—		-40 to 105 °C

Table continues on the next page...

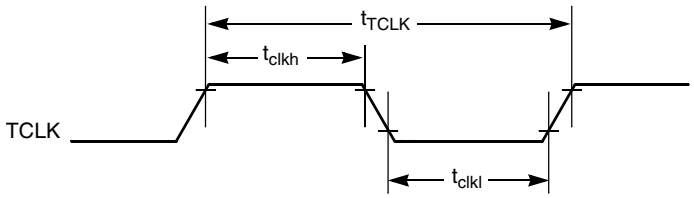


Figure 9. Timer external clock

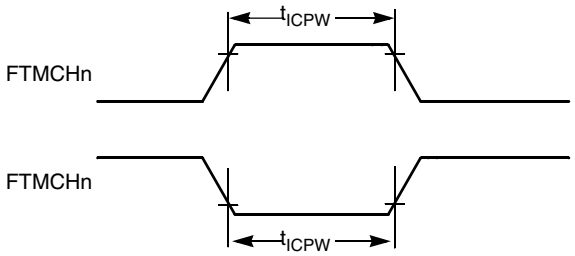


Figure 10. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	-40 to 105	°C
Junction temperature range	T_J	-40 to 150	°C
Thermal resistance single-layer board			
64-pin LQFP	θ_{JA}	71	°C/W
64-pin QFP	θ_{JA}	61	°C/W
48-pin LQFP	θ_{JA}	81	°C/W
44-pin LQFP	θ_{JA}	75	°C/W
32-pin LQFP	θ_{JA}	86	°C/W

Table continues on the next page...

Table 10. Flash characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	—	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17030	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16977	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	843	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	517	t_{cyc}
D	Erase Verify EEPROM Section	$t_{DRD1SEC}$	0.10	0.10	0.11	ms
D	Read Once	t_{RDONCE}	—	—	455	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.14	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.24	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.24	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.02	0.02	0.02	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.20	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	125.80	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	125.76	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	25.05	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	6.30	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	125.80	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	469	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	442	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimun times are based on maxmum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on minimum f_{NVMOP} and maximum f_{NVMBUS}
4. t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

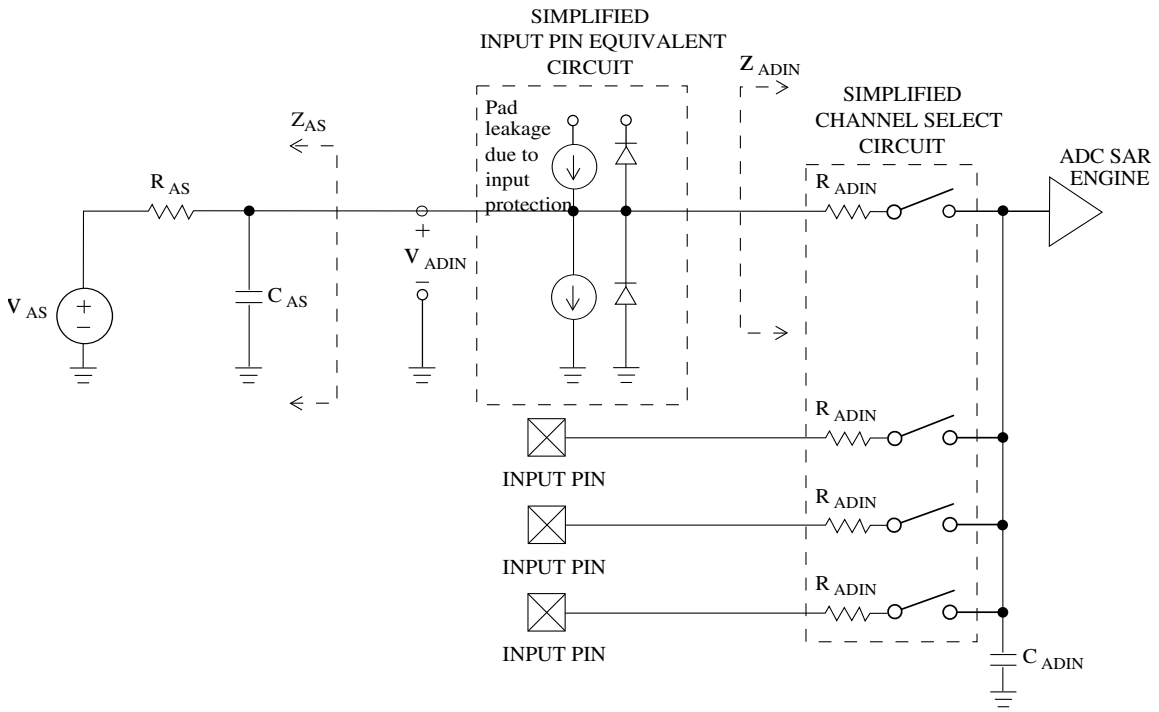


Figure 12. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA

Table continues on the next page...

6.3.2 Analog comparator (ACMP) electricals

Table 13. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	µs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted, and 100 pF load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

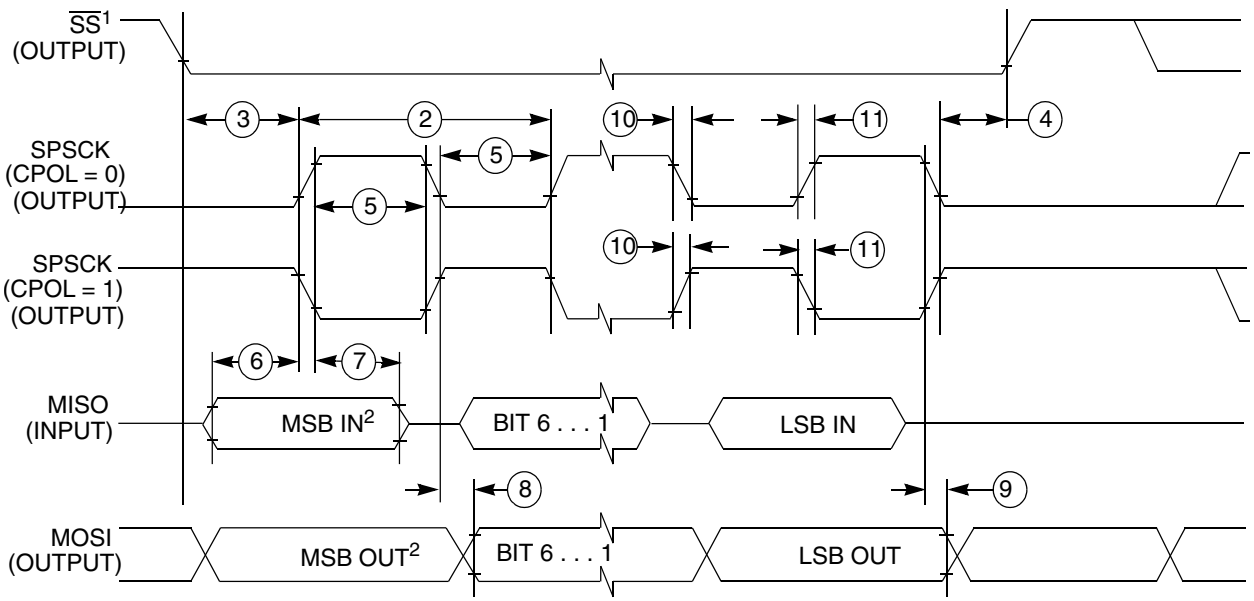
Table 14. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	f_{Bus}/2048	f_{Bus}/2	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	2 x t_{Bus}	2048 x t_{Bus}	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	1024 x t_{Bus}	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—

Table continues on the next page...

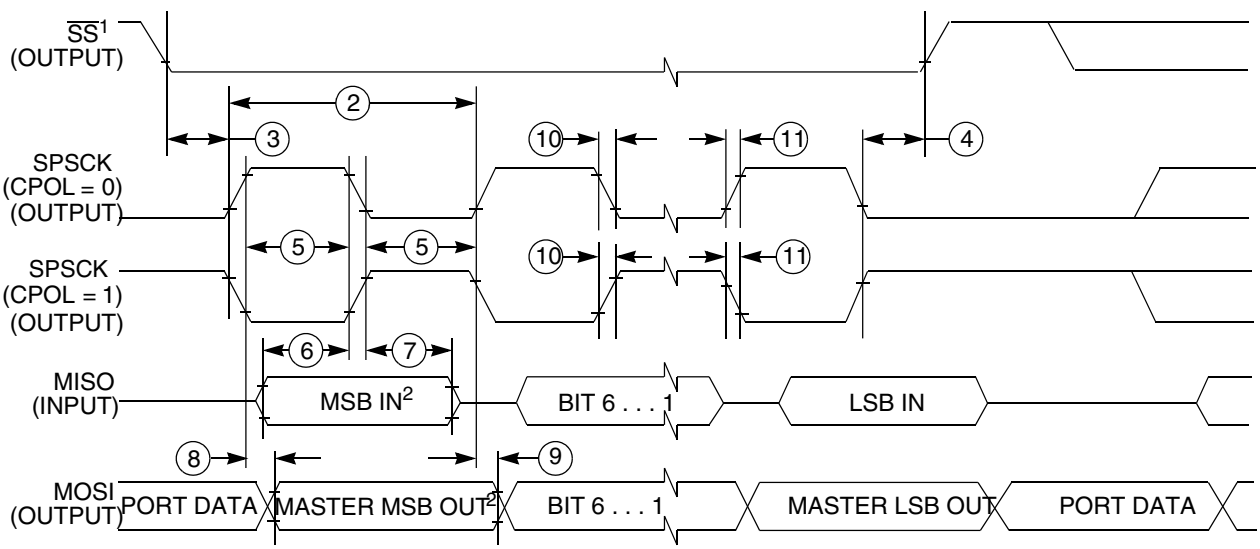
Table 14. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
10	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 13. SPI master mode timing (CPHA=0)



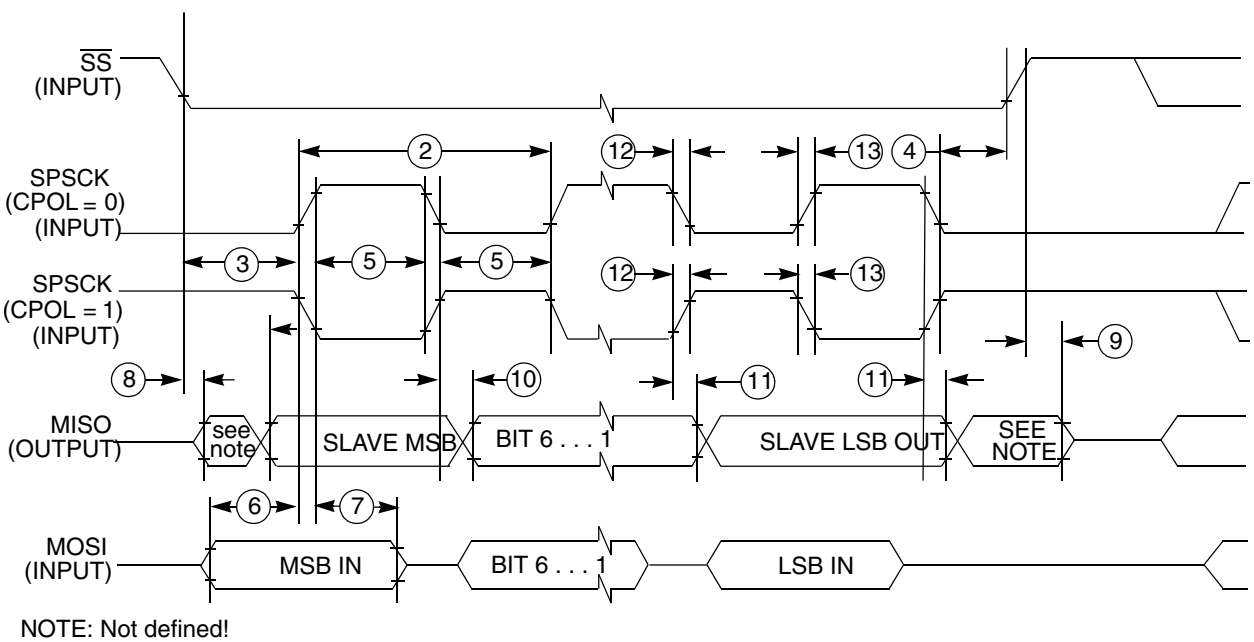
1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA=1)

Table 15. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined!

Figure 15. SPI slave mode timing (CPHA = 0)

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 16. Pin availability by package pin-count

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	1	PTD1	KBI1P1	FTM2CH3	MOSI1	—
2	2	2	2	PTD0[1]	KBI1P0	FTM2CH2	SPSCK1	—
3	—	—	—	PTH7	—	—	—	—
4	—	—	—	PTH6	—	—	—	—
5	3	3	—	PTE7	—	TCLK2	—	—
6	4	4	—	PTH2	—	BUSOUT	—	—
7	5	5	3	—	—	—	—	V_{DD}
8	6	6	4	—	—	—	V_{DDA}	V_{REFH}
9	7	7	5	—	—	—	V_{SSA}	V_{REFL}
10	8	8	6	—	—	—	—	V_{SS}
11	9	9	7	PTB7	—	SCL	—	EXTAL
12	10	10	8	PTB6	—	SDA	—	XTAL
13	11	11	—	—	—	—	—	V_{SS}
14	—	—	—	PTH1[1]	—	FTM2CH1	—	—
15	—	—	—	PTH0[1]	—	FTM2CH0	—	—
16	12	—	—	PTE6	—	—	—	—
17	13	—	—	PTE5	—	—	—	—
18	14	12	9	PTB5[1]	FTM2CH5	SS0	—	—
19	15	13	10	PTB4[1]	FTM2CH4	MISO0	—	—
20	16	14	11	PTC3	FTM2CH3	—	ADP11	—
21	17	15	12	PTC2	FTM2CH2	—	ADP10	—
22	18	16	—	PTD7	KBI1P7	TXD2	—	—
23	19	17	—	PTD6	KBI1P6	RXD2	—	—
24	20	18	—	PTD5	KBI1P5	—	—	—
25	21	19	13	PTC1	—	FTM2CH1	ADP9	—
26	22	20	14	PTC0	—	FTM2CH0	ADP8	—
27	—	—	—	PTF7	—	—	ADP15	—

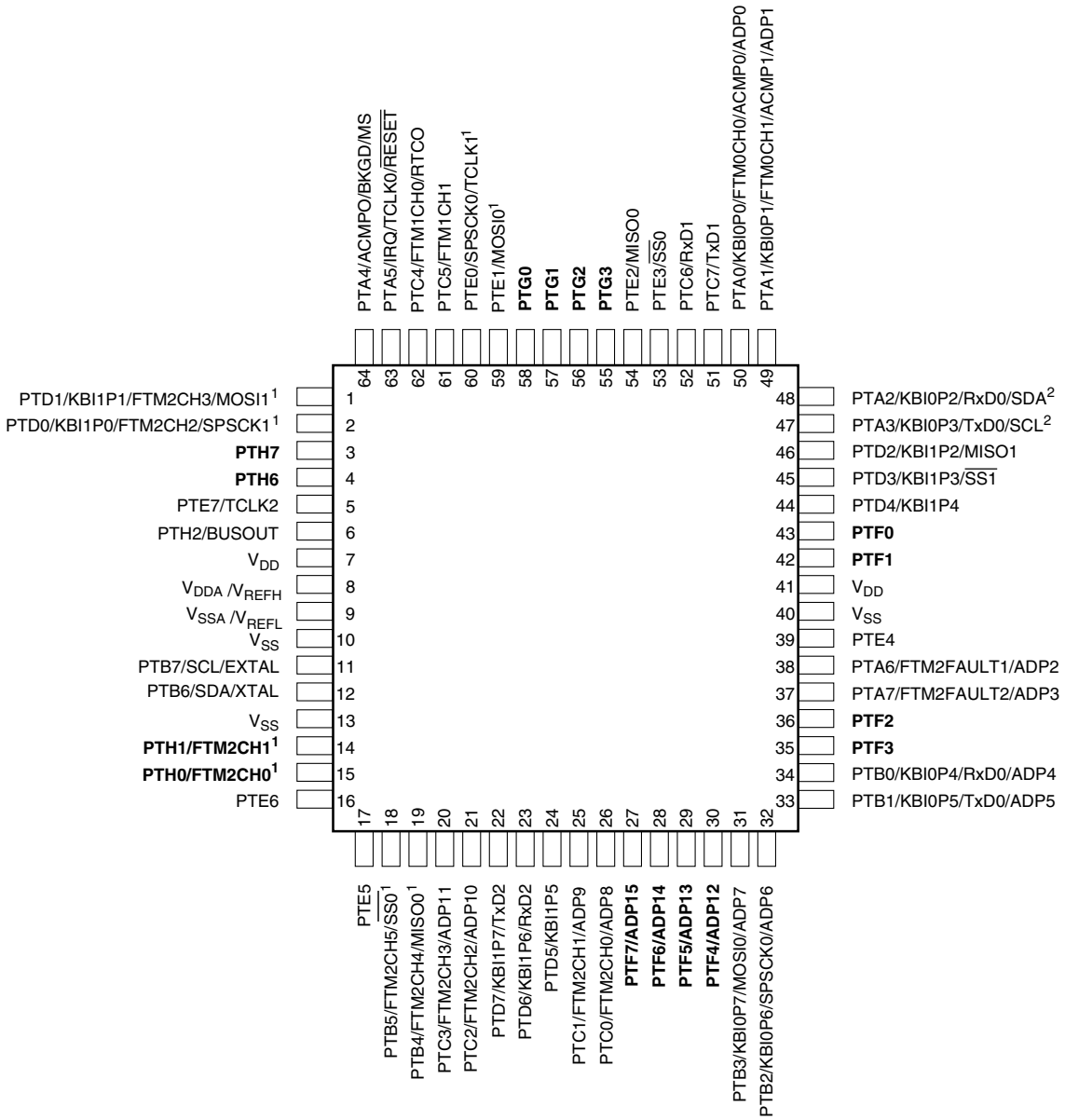
Table continues on the next page...

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

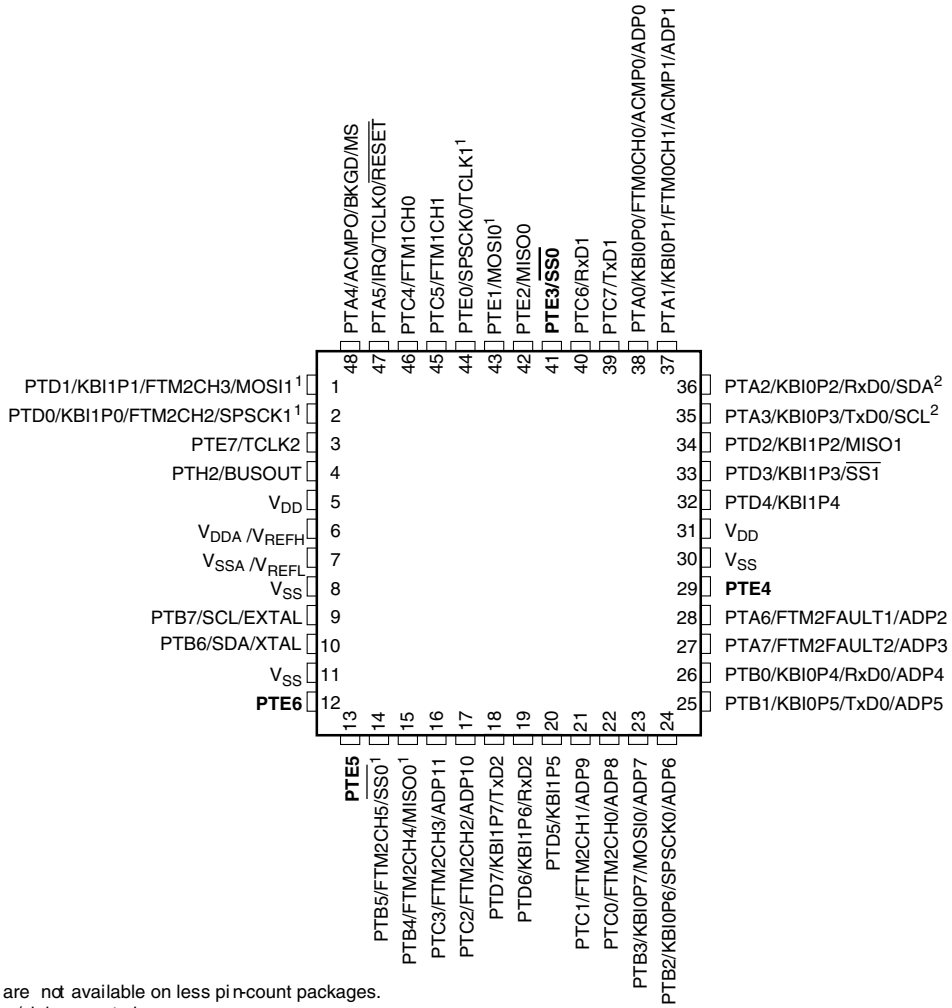
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment



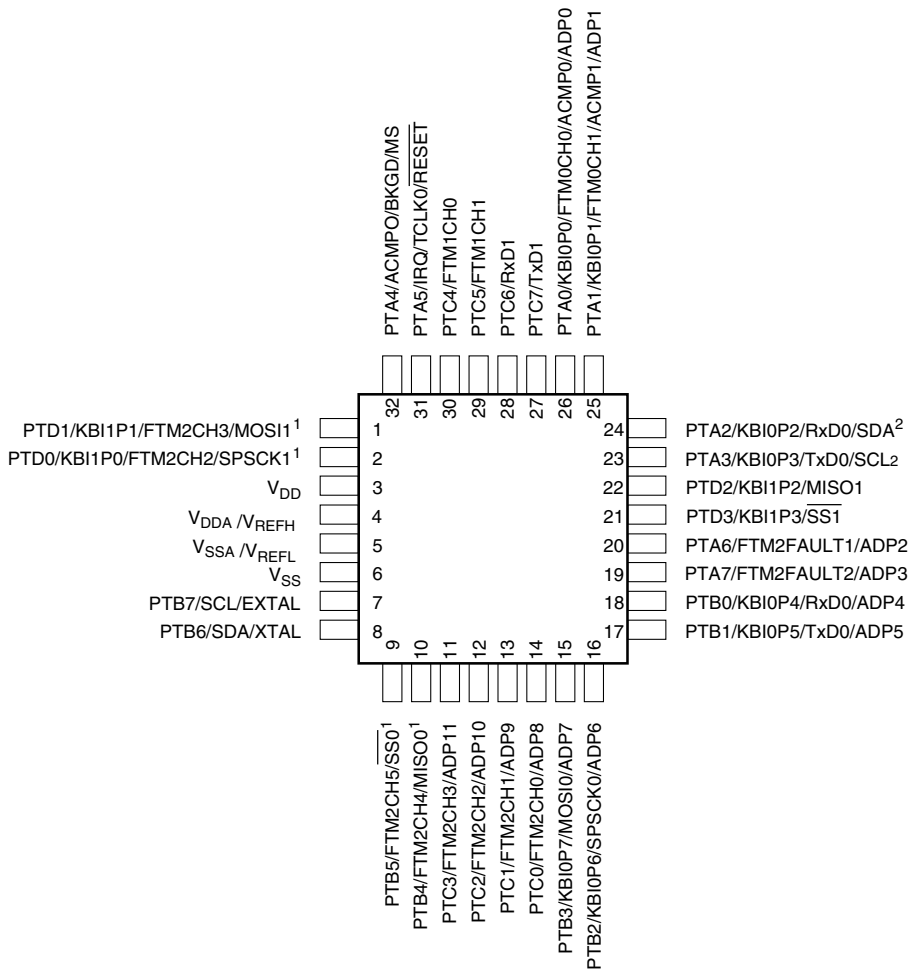
Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 17. MC9S08PA60 64-pin QFP and LQFP package



Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

Figure 18. MC9S08PA60 48-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 20. MC9S08PA60 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 17. Revision history

Rev. No.	Date	Substantial Changes
1	10/2012	Initial public release

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