Renesas Electronics America Inc - DE71464RN80FPV Datasheet

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Applications of "Embedded - Microcontrollers"

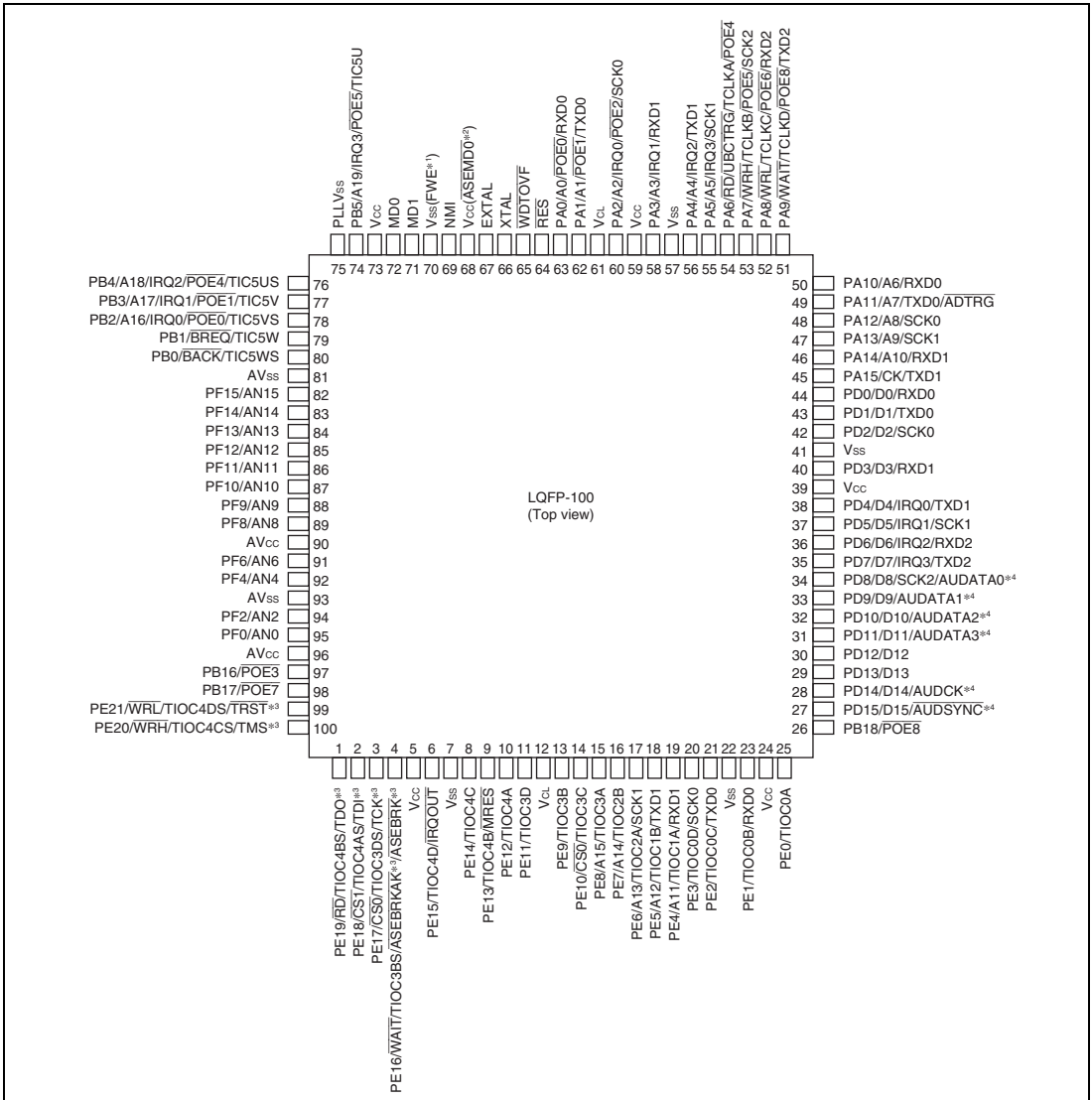
Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/de71464rn80fpv

Section 16 Compare Match Timer (CMT)

Section 17 Pin Function Controller (PFC)

Section 18 I/O Ports

Section 19 Flash Memory



Notes: 1. Fixed to V_{SS} in the masked ROM version, and used as the FWE input pin in the F-ZTAT version.
2. A pin for the E10A emulator. Fixed to V_{CC} in the masked ROM version, and used as the $\overline{\text{ASEMD0}}$ input pin in the F-ZTAT version.
3. This pin function is available only in the F-ZTAT version. (Not available in the masked ROM version.)
4. This pin function is available only in F-ZTAT version supporting full functions of E10A.
(Not available in the normal F-ZTAT version and the masked ROM version.)

Figure 1.3 Pin Assignments of SH7149 (LQFP Version)

2.5.5 Shift Instructions

Table 2.14 Shift Instructions

Instruction		Operation	Code	Execution Cycles	T Bit
ROTL	Rn	T ← Rn ← MSB	0100nnnn00000100	1	MSB
ROTR	Rn	LSB → Rn → T	0100nnnn00000101	1	LSB
ROTCL	Rn	T ← Rn ← T	0100nnnn00100100	1	MSB
ROTCR	Rn	T → Rn → T	0100nnnn00100101	1	LSB
SHAL	Rn	T ← Rn ← 0	0100nnnn00100000	1	MSB
SHAR	Rn	MSB → Rn → T	0100nnnn00100001	1	LSB
SHLL	Rn	T ← Rn ← 0	0100nnnn00000000	1	MSB
SHLR	Rn	0 → Rn → T	0100nnnn00000001	1	LSB
SHLL2	Rn	Rn << 2 → Rn	0100nnnn00001000	1	—
SHLR2	Rn	Rn >> 2 → Rn	0100nnnn00001001	1	—
SHLL8	Rn	Rn << 8 → Rn	0100nnnn00011000	1	—
SHLR8	Rn	Rn >> 8 → Rn	0100nnnn00011001	1	—
SHLL16	Rn	Rn << 16 → Rn	0100nnnn00101000	1	—
SHLR16	Rn	Rn >> 16 → Rn	0100nnnn00101001	1	—

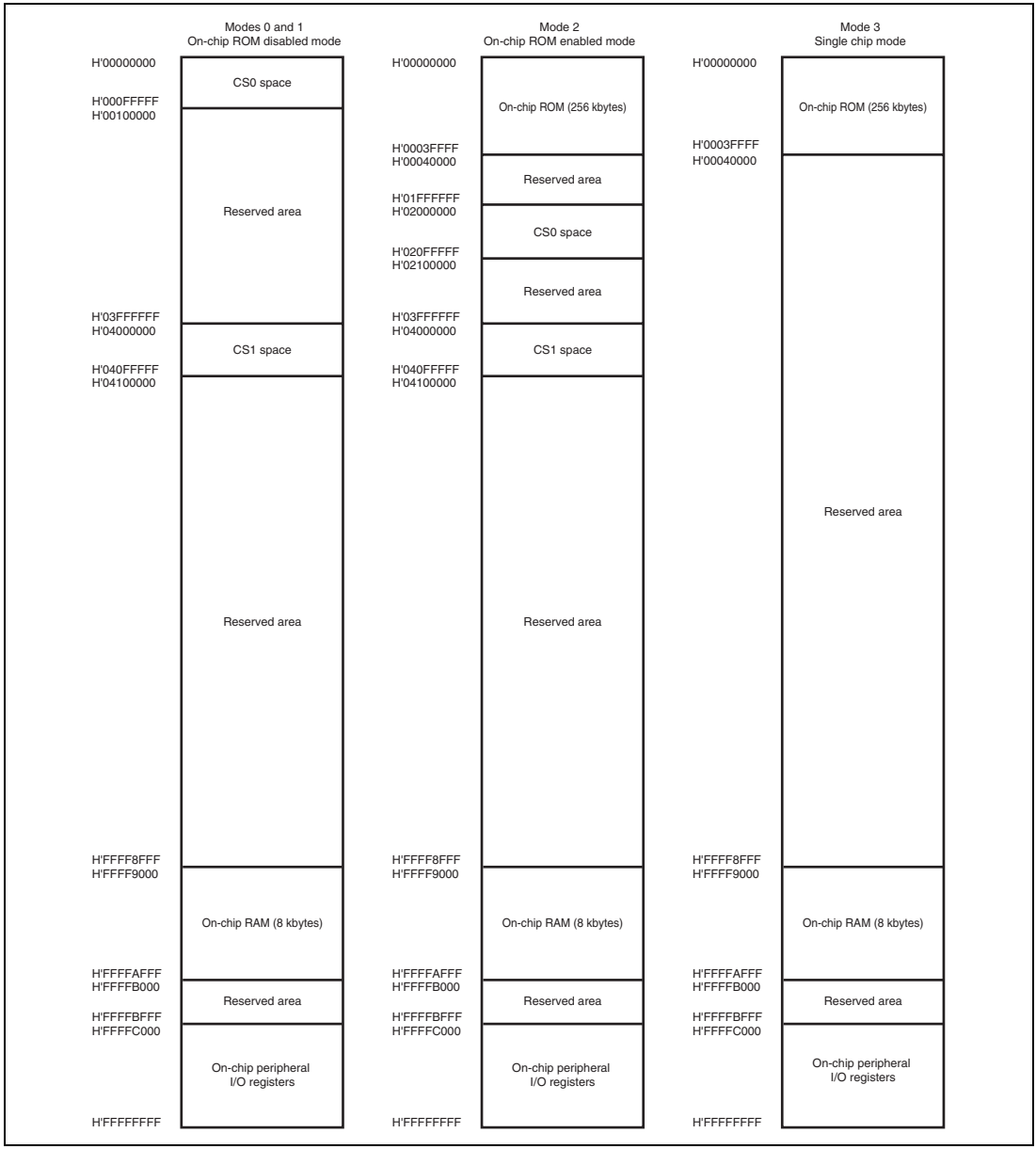


Figure 3.2 Address Map for Each Operating Mode in SH7149

Origin of Activation Source	Activation Source	Vector Number	DTC Vector Address Offset	DTCE*1	Transfer Source	Transfer Destination	Priority
MTU2S_3	TGIA_3S	160	H'680	DTCERC3	Arbitrary*2	Arbitrary*2	High
	TGIB_3S	161	H'684	DTCERC2	Arbitrary*2	Arbitrary*2	
	TGIC_3S	162	H'688	DTCERC1	Arbitrary*2	Arbitrary*2	
	TGID_3S	163	H'68C	DTCERC0	Arbitrary*2	Arbitrary*2	
MTU2S_4	TGIA_4S	168	H'6A0	DTCERD15	Arbitrary*2	Arbitrary*2	
	TGIB_4S	169	H'6A4	DTCERD14	Arbitrary*2	Arbitrary*2	
	TGIC_4S	170	H'6A8	DTCERD13	Arbitrary*2	Arbitrary*2	
	TGID_4S	171	H'6AC	DTCERD12	Arbitrary*2	Arbitrary*2	
	TCIV_4S	172	H'6B0	DTCERD11	Arbitrary*2	Arbitrary*2	
MTU2S_5	TGIU_5S	176	H'6C0	DTCERD10	Arbitrary*2	Arbitrary*2	
	TGIV_5S	177	H'6C4	DTCERD9	Arbitrary*2	Arbitrary*2	
	TGIW_5S	178	H'6C8	DTCERD8	Arbitrary*2	Arbitrary*2	
CMT_0	CMI_0	184	H'6E0	DTCERD7	Arbitrary*2	Arbitrary*2	
CMT_1	CMI_1	188	H'6F0	DTCERD6	Arbitrary*2	Arbitrary*2	
A/D_0, A/D_1	ADI_0	200	H'720	DTCERD5	ADDR0 to ADDR3	Arbitrary*2	
	ADI_1	201	H'724	DTCERD4	ADDR4 to ADDR7	Arbitrary*2	
A/D_2	ADI_2	204	H'730	DTCERD3	ADDR8 to ADDR15	Arbitrary*2	
SCI_0	RXI_0	217	H'764	DTCERE15	SCRDR_0	Arbitrary*2	
	TXI_0	218	H'768	DTCERE14	Arbitrary*2	SCTDR_0	
SCI_1	RXI_1	221	H'774	DTCERE13	SCRDR_1	Arbitrary*2	
	TXI_1	222	H'778	DTCERE12	Arbitrary*2	SCTDR_1	
SCI_2	RXI_2	225	H'784	DTCERE11	SCRDR_2	Arbitrary*2	
	TXI_2	226	H'788	DTCERE10	Arbitrary*2	SCTDR_2	Low

Notes: 1. The DTCE bits with no corresponding interrupt are reserved, and the write value should always be 0. To leave software standby mode with an interrupt, write 0 to the corresponding DTCE bit.

2. An external memory, a memory-mapped external device, an on-chip memory, or an on-chip peripheral module (except DTC, BSC, UBC, and FLASH) can be selected as the source or destination. Note that at least either the source or destination must be an on-chip peripheral module; transfer cannot be done among an external memory, a memory-mapped external device, and an on-chip memory.

Table 10.1 MTU2 Functions

Item		Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Count clock		MPϕ/1 MPϕ/4 MPϕ/16 MPϕ/64 TCLKA TCLKB TCLKC TCLKD	MPϕ/1 MPϕ/4 MPϕ/16 MPϕ/64 MPϕ/256 TCLKA TCLKB	MPϕ/1 MPϕ/4 MPϕ/16 MPϕ/64 MPϕ/1024 TCLKA TCLKB TCLKC	MPϕ/1 MPϕ/4 MPϕ/16 MPϕ/64 MPϕ/256 MPϕ/1024 TCLKA TCLKB	MPϕ/1 MPϕ/4 MPϕ/16 MPϕ/64 MPϕ/256 MPϕ/1024 TCLKA TCLKB	MPϕ/1 MPϕ/4 MPϕ/16 MPϕ/64
General registers		TGRA_0 TGRB_0 TGRE_0	TGRA_1 TGRB_1	TGRA_2 TGRB_2	TGRA_3 TGRB_3	TGRA_4 TGRB_4	TGRU_5 TGRV_5 TGRW_5
General registers/ buffer registers		TGRC_0 TGRD_0 TGRF_0	—	—	TGRC_3 TGRD_3	TGRC_4 TGRD_4	—
I/O pins		TIOC0A TIOC0B TIOC0C TIOC0D	TIOC1A TIOC1B	TIOC2A TIOC2B	TIOC3A TIOC3B TIOC3C TIOC3D	TIOC4A TIOC4B TIOC4C TIOC4D	Input pins TIC5U TIC5V TIC5W
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	0 output	√	√	√	√	√	—
	1 output	√	√	√	√	√	—
	Toggle output	√	√	√	√	√	—
Input capture function		√	√	√	√	√	√
Synchronous operation		√	√	√	√	√	—
PWM mode 1		√	√	√	√	√	—
PWM mode 2		√	√	√	—	—	—
Complementary PWM mode		—	—	—	√	√	—
Reset PWM mode		—	—	—	√	√	—
AC synchronous motor drive mode		√	—	—	√	√	—

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Phase counting mode	—	√	√	—	—	—
Buffer operation	√	—	—	√	√	—
Dead time compensation counter function	—	—	—	—	—	√
DTC activation	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture and TCNT overflow or underflow	TGR compare match or input capture
A/D converter start trigger	TGRA_0 compare match or input capture TGRE_0 compare match	TGRA_1 compare match or input capture	TGRA_2 compare match or input capture	TGRA_3 compare match or input capture	TGRA_4 compare match or input capture TCNT_4 underflow (trough) in complementary PWM mode	—

10.3.6 Timer Status Register (TSR)

The TSR registers are 8-bit readable/writable registers that indicate the status of each channel. The MTU2 has seven TSR registers, two for channel 0 and one each for channels 1 to 5.

- TSR_0, TSR_1, TSR_2, TSR_3, TSR_4

Bit:	7	6	5	4	3	2	1	0
	TCFD	-	TCFU	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value:	1	1	0	0	0	0	0	0
R/W:	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

Bit	Bit Name	Initial Value	R/W	Description
7	TCFD	1	R	Count Direction Flag Status flag that shows the direction in which TCNT counts in channels 1 to 4. In channel 0, bit 7 is reserved. It is always read as 1 and the write value should always be 1. 0: TCNT counts down 1: TCNT counts up
6	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
5	TCFU	0	R/(W)*[1]	Underflow Flag Status flag that indicates that TCNT underflow has occurred when channels 1 and 2 are set to phase counting mode. Only 0 can be written, for flag clearing. In channels 0, 3, and 4, bit 5 is reserved. It is always read as 0 and the write value should always be 0. [Setting condition] • When the TCNT value underflows (changes from H'0000 to H'FFFF) [Clearing condition] • When 0 is written to TCFU after reading TCFU = 1*[2]

10.5.3 A/D Converter Activation

The A/D converter can be activated by one of the following three methods in the MTU2. Table 10.58 shows the relationship between interrupt sources and A/D converter start request signals.

A/D Converter Activation by TGRA Input Capture/Compare Match or at TCNT_4 Trough in Complementary PWM Mode: The A/D converter can be activated by the occurrence of a TGRA input capture/compare match in each channel. In addition, if complementary PWM operation is performed while the TTGE2 bit in TIER_4 is set to 1, the A/D converter can be activated at the trough of TCNT_4 count (TCNT_4 = H'0000).

A/D converter start request signal TRGAN is issued to the A/D converter under either one of the following conditions.

- When the TGFA flag in TSR is set to 1 by the occurrence of a TGRA input capture/compare match on a particular channel while the TTGE bit in TIER is set to 1
- When the TCNT_4 count reaches the trough (TCNT_4 = H'0000) during complementary PWM operation while the TTGE2 bit in TIER_4 is set to 1

When either condition is satisfied, if A/D converter start signal TRGAN from the MTU2 is selected as the trigger in the A/D converter, A/D conversion will start.

A/D Converter Activation by Compare Match between TCNT_0 and TGRE_0: The A/D converter can be activated by generating A/D converter start request signal TRG0N when a compare match occurs between TCNT_0 and TGRE_0 in channel 0.

When the TGFE flag in TSR2_0 is set to 1 by the occurrence of a compare match between TCNT_0 and TGRE_0 in channel 0 while the TTGE2 bit in TIER2_0 is set to 1, A/D converter start request TGR0N is issued to the A/D converter. If A/D converter start signal TGR0N from the MTU2 is selected as the trigger in the A/D converter, A/D conversion will start.

A/D Converter Activation by A/D Converter Start Request Delaying Function: The A/D converter can be activated by generating A/D converter start request signal TRG4AN or TRG4BN when the TCNT_4 count matches the TADCORA or TADCORB value if the TAD4AE or TAD4BE bit in the A/D converter start request control register (TADCR) is set to 1. For details, refer to section 10.4.9, A/D Converter Start Request Delaying Function.

A/D conversion will start if A/D converter start signal TRG4AN from the MTU2 is selected as the trigger in the A/D converter when TRG4AN is generated or if TRG4BN from the MTU2 is selected as the trigger in the A/D converter when TRG4BN is generated.

Bit	Bit Name	Initial value	R/W	Description
2	MTU2PE2ZE	0	R/W*	MTU2 PE2 High-Impedance Enable This bit specifies whether to place the PE2/TIOC0C pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state
1	MTU2PE1ZE	0	R/W*	MTU2 PE1 High-Impedance Enable This bit specifies whether to place the PE1/TIOC0B pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state
0	MTU2PE0ZE	0	R/W*	MTU2 PE0 High-Impedance Enable This bit specifies whether to place the PE0/TIOC0A pin for channel 0 in the MTU2 in high-impedance state when either POE8F or MTU2CH0HIZ bit is set to 1. 0: Does not place the pin in high-impedance state 1: Places the pin in high-impedance state

Note: * Can be modified only once after a power-on reset.

13.3.2 Watchdog Timer Control/Status Register (WTCSR)

WTCSR is an 8-bit readable/writable register composed of bits to select the clock used for the count, bits to select the timer mode, and overflow flags. WTCSR holds its value in an internal reset due to the WDT overflow. WTCSR is initialized to H'00 only by a power-on reset using the $\overline{\text{RES}}$ pin.

When used to count the clock settling time for revoking a software standby, it retains its value after counter overflow. Use a word access to write to WTCSR, with H'A5 in the upper byte. Use a byte access to read WTCSR.

Note: WTCSR differs from other registers in that it is more difficult to write to. See section 13.3.3, Notes on Register Access, for details.

Bit:	7	6	5	4	3	2	1	0
	TME	WT/IT	RSTS	WOVF	IOVF	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TME	0	R/W	Timer Enable Starts and stops timer operation. Clear this bit to 0 when using the WDT to revoke software standby mode. 0: Timer disabled: Count-up stops and WTCNT value is retained 1: Timer enabled
6	WT/IT	0	R/W	Timer Mode Select Selects whether to use the WDT as a watchdog timer or an interval timer. 0: Interval timer mode 1: Watchdog timer mode Note: If WT/IT is modified when the WDT is operating, the up-count may not be performed correctly.

Bit	Bit Name	Initial Value	R/W	Description
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PB2MD2	0*[1]	R/W	PB2 Mode
9	PB2MD1	0	R/W	Select the function of the
8	PB2MD0	0*[1]	R/W	PB2/A16/IRQ0/$\overline{\text{POE0}}$/TIC5VS pin. 000: PB2 I/O (port) 001: IRQ0 input (INTC) 010: $\overline{\text{POE0}}$ input (POE) 011: TIC5VS input (MTU2S) 101: A16 output (BSC)*[2] Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PB1MD2	0	R/W	PB1 Mode
5	PB1MD1	0	R/W	Select the function of the PB1/$\overline{\text{BREQ}}$/TIC5W pin.
4	PB1MD0	0	R/W	000: PB1 I/O (port) 011: TIC5W input (MTU2) 101: $\overline{\text{BREQ}}$ input (BSC)*[2] Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PB0MD2	0	R/W	PB0 Mode
1	PB0MD1	0	R/W	Select the function of the PB0/$\overline{\text{BACK}}$/TIC5WS pin.
0	PB0MD0	0	R/W	000: PB0 I/O (port) 011: TIC5WS input (MTU2S) 101: $\overline{\text{BACK}}$ output (BSC)*[2] Other than above: Setting prohibited

Notes: 1. The initial value is 1 in the on-chip ROM disabled external-extension mode.
2. This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

(1) SCI Interface Setting by Host

When boot mode is initiated, this LSI measures the low period of asynchronous SCI-communication data (H'00), which is transmitted consecutively by the host. The SCI transmit/receive format is set to 8-bit data, 1 stop bit, and no parity. This LSI calculates the bit rate of transmission by the host by means of the measured low period and transmits the bit adjustment end sign (1 byte of H'00) to the host. The host must confirm that this bit adjustment end sign (H'00) has been received normally and transmits 1 byte of H'55 to this LSI. When reception is not executed normally, boot mode is initiated again (reset) and the operation described above must be executed. The bit rate between the host and this LSI is not matched because of the bit rate of transmission by the host and system clock frequency of this LSI. To operate the SCI normally, the transfer bit rate of the host must be set to 9,600 bps or 19,200 bps.

The system clock frequency which can automatically adjust the transfer bit rate of the host and the bit rate of this LSI is shown in table 19.8. Boot mode must be initiated in the range of this system clock. Note that the internal clock division ratio of ×1/3 is not supported in boot mode.

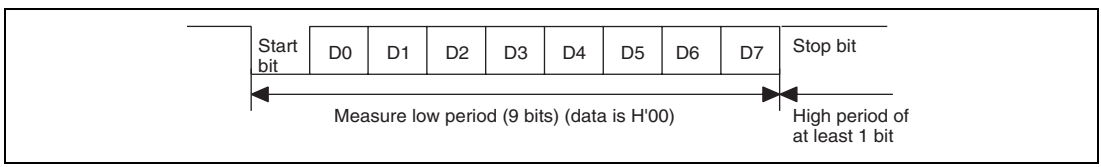


Figure 19.7 Automatic Adjustment Operation of SCI Bit Rate

Table 19.8 Peripheral Clock (Pϕ) Frequency that Can Automatically Adjust Bit Rate of This LSI

Host Bit Rate	Peripheral Clock (Pϕ) Frequency Which Can Automatically Adjust LSI's Bit Rate
9,600 bps	10 to 40 MHz
19,200 bps	10 to 40 MHz

Note: The internal clock division ratio of ×1/3 is not supported in boot mode.

19.8.3 Other Notes

1. Download time of on-chip program

   The programming program that includes the initialization routine and the erasing program that includes the initialization routine are each 3 kbytes or less. Accordingly, when the CPU clock frequency is 20 MHz, the download for each program takes approximately 10 ms at maximum.

2. User branch processing intervals

   The intervals for executing the user branch processing differs in programming and erasing. The processing phase also differs. Table 19.11 lists the maximum intervals for initiating the user branch processing when the CPU clock frequency is 80 MHz.

Table 19.11 Initiation Intervals of User Branch Processing

Processing Name	Maximum Interval
Programming	Approximately 2 ms
Erasing	Approximately 15 ms

However, when operation is done with CPU clock of 80 MHz, maximum values of the time until first user branch processing are as shown in table 19.12.

Table 19.12 Initial User Branch Processing Time

Processing Name	Max.
Programming	Approximately 2 ms
Erasing	Approximately 15 ms

3. Write to flash-memory related registers by DTC

   While an instruction in on-chip RAM is being executed, the DTC can write to the SCO bit in FCCS that is used for a download request or FMATS that is used for MAT switching. Make sure that these registers are not accidentally written to, otherwise an on-chip program may be downloaded and destroy RAM or a MAT switchover may occur and the CPU get out of control.

4. State in which interrupts are ignored

   In the following modes or period, interrupt requests are ignored; they are not executed and the interrupt sources are not retained.

   — Boot mode

   — Programmer mode

(1) Selection of user boot MAT programming

In response to the command for selecting programming of the user boot MAT, the boot program transfers the corresponding flash-writing program, i.e. the program for writing to the user boot MAT.

Command	H'42

— Command H'42 (1 byte): Selects programming of the user boot MAT.

Response	H'06

— Response H'06 (1 byte): Response to selection of user boot MAT programming
This ACK code is returned after transfer of the program that performs writing to the user boot MAT.

Error response	H'C2	ERROR

— Error response H'C2 (1 byte): Error response to selection of user boot MAT programming
— ERROR (1 byte): Error code
H'54: Error in selection processing (processing was not completed because of a transfer error)

(2) Selection of user MAT programming

In response to the command for selecting programming of the user MAT, the boot program transfers the corresponding flash-writing program, i.e. the program for writing to the user MAT.

Command	H'43

— Command H'43 (1 byte): Selects programming of the user MAT.

Response	H'06

— Response H'06 (1 byte): Response to selection of user MAT programming
This ACK code is returned after transfer of the program that performs writing to the user MAT.

Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access States	Connected Bus Width
Timer counter U_5S	TCNTU_5S	16	H'FFFFC880	MTU2S	16, 32	MIϕ reference	16 bits
Timer general register U_5S	TGRU_5S	16	H'FFFFC882		16	B:2	
Timer control register U_5S	TCRU_5S	8	H'FFFFC884		8	W:2	
Timer I/O control register U_5S	TIORU_5S	8	H'FFFFC886		8	L:4	
Timer counter V_5S	TCNTV_5S	16	H'FFFFC890		16, 32		
Timer general register V_5S	TGRV_5S	16	H'FFFFC892		16		
Timer control register V_5S	TCRV_5S	8	H'FFFFC894		8		
Timer I/O control register V_5S	TIORV_5S	8	H'FFFFC896		8		
Timer counter W_5S	TCNTW_5S	16	H'FFFFC8A0		16, 32		
Timer general register W_5S	TGRW_5S	16	H'FFFFC8A2		16		
Timer control register W_5S	TCRW_5S	8	H'FFFFC8A4		8		
Timer I/O control register W_5S	TIORW_5S	8	H'FFFFC8A6		8		
Timer status register_5S	TSR_5S	8	H'FFFFC8B0		8		
Timer interrupt enable register_5S	TIER_5S	8	H'FFFFC8B2		8		
Timer start register_5S	TSTR_5S	8	H'FFFFC8B4		8		
Timer compare match clear register S	TCNTCMPCLRS	8	H'FFFFC8B6		8		
A/D data register 0	ADDR0	16	H'FFFFC900	A/D	16	Pϕ reference	16 bits
A/D data register 2	ADDR2	16	H'FFFFC904	(Channel 0)	16	B:2	
A/D control/status register_0	ADCSR_0	16	H'FFFFC910		16	W:2	
A/D control register_0	ADCR_0	16	H'FFFFC912		16		
A/D data register 4	ADDR4	16	H'FFFFC980	A/D	16	Pϕ reference	16 bits
A/D data register 6	ADDR6	16	H'FFFFC984	(Channel 1)	16	B:2	
A/D control/status register_1	ADCSR_1	16	H'FFFFC990		16	W:2	
A/D control register_1	ADCR_1	16	H'FFFFC992		16		
A/D data register 8	ADDR8	16	H'FFFFCA00	A/D	16	Pϕ reference	16 bits
A/D data register 9	ADDR9	16	H'FFFFCA02	(Channel 2)	16	B:2	
A/D data register 10	ADDR10	16	H'FFFFCA04		16	W:2	
A/D data register 11	ADDR11	16	H'FFFFCA06		16		
A/D data register 12	ADDR12	16	H'FFFFCA08		16		
A/D data register 13	ADDR13	16	H'FFFFCA0A		16		
A/D data register 14	ADDR14	16	H'FFFFCA0C		16		

23.3 Register States in Each Operating Mode

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Deep Software Standby	Module Standby	Sleep	Module
SCSMR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	SCI (Channel 0)
SCBRR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSCR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCTDR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSSR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCRDR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSDCR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSPTR_0	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSMR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	SCI (Channel 1)
SCBRR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSCR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCTDR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSSR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCRDR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSDCR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSPTR_1	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSMR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	SCI (Channel 2)
SCBRR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSCR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCTDR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSSR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCRDR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSDCR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
SCSPTR_2	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
TCR_3	Initialized	Retained	Initialized	Initialized	Initialized	Retained	MTU2
TCR_4	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
TMDR_3	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
TMDR_4	Initialized	Retained	Initialized	Initialized	Initialized	Retained	
TIORH_3	Initialized	Retained	Initialized	Initialized	Initialized	Retained	

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current Only in F-ZTAT version supporting full functions of E10A.	Normal operation	I_{CC}	—	150	165	mA	Iϕ = 80 MHz Bϕ = 40 MHz Pϕ = 40 MHz MPϕ = 40 MHz MIϕ = 80 MHz
	Sleep		—	140	150	mA	Bϕ = 40 MHz Pϕ = 40 MHz MPϕ = 40 MHz MIϕ = 80 MHz
	Software standby		—	20	60	mA	$T_a \leq 50°C$
			—	—	120	mA	$50°C < T_a$
	Deep software standby		—	20	50	µA	$T_a \leq 50°C$
			—	—	120	µA	$50°C < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	3	6	mA	The value per A/D converter module.
	Waiting for A/D conversion		—	—	3.5	mA	
	Standby		—	—	10	µA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	V_{CC}

[Operating Precautions]

1. When the A/D converter is not used, do not leave the AV_{CC} and AV_{SS} pins open.
2. The current consumption is measured when V_{IH} (Min.) = V_{CC} – 0.5 V, V_{IL} (Max.) = 0.5 V, with all output pins unloaded.

Note: * When the $\overline{\text{POE8}}$ function is selected for the PB18/$\overline{\text{POE8}}$ pin by the PFC.