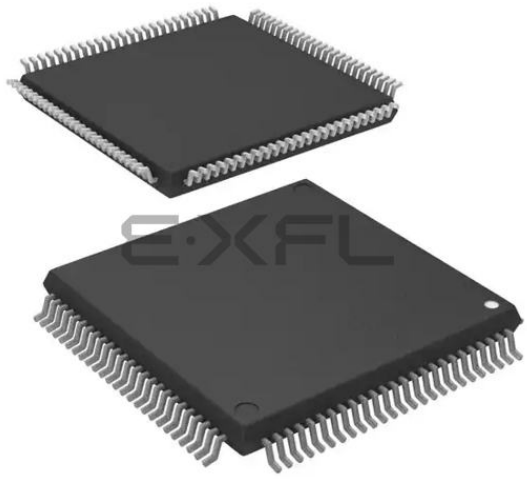
Renesas Electronics America Inc - DE71494RN80FPV Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	63
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/de71494rn80fpv

Items	Specification
On-chip ROM	• 256 kbytes
On-chip RAM	• 8 kbytes
Bus state controller (BSC)	• Address space: A maximum 64 Mbytes for each of two areas (CS0 and CS1) (only in SH7149) • 8-bit external bus (only in SH7149) • 16-bit external bus (only in SH7149) • The following features settable for each area independently — Bus size (8 or 16 bits) — Number of access wait cycles — Idle wait cycle insertion — Supports SRAM • Outputs a chip select signal according to the target area
Data transfer controller (DTC) (only in F-ZTAT version)	• Data transfer activated by an on-chip peripheral module interrupt can be done independently of the CPU transfer. • Transfer mode selectable for each interrupt source (transfer mode is specified in memory) • Multiple data transfer enabled for one activation source • Various transfer modes Normal mode, repeat mode, or block transfer mode can be selected. • Data transfer size can be specified as byte, word, or longword • The interrupt that activated the DTC can be issued to the CPU. A CPU interrupt can be requested after one data transfer completion. • A CPU interrupt can be requested after all specified data transfer completion.
Interrupt controller (INTC)	• Five external interrupt pins (NMI and IRQ3 to IRQ0) • On-chip peripheral interrupts: Priority level set for each module • Vector addresses: A vector address for each interrupt source
User debugging interface (H-UDI) (only in F-ZTAT version)	• E10A emulator support
Advanced user debugger (AUD) (only in F-ZTAT version supporting full functions of E10A)	• E10A emulator support

7.3.11 Break Control Register (BRCR)

BRCR sets the following conditions:

1. Channels A and B are used in two independent channel conditions or under the sequential condition.
2. A user break is set before or after instruction execution.
3. Specify whether to include the number of execution times on channel B in comparison conditions.
4. Determine whether to include data bus on channels A and B in comparison conditions.
5. Enable PC trace.
6. Select the $\overline{\text{UBCTRG}}$ output pulse width.
7. Specify whether to request the user break interrupt when channels A and B match with comparison conditions.

BRCR is a 32-bit readable/writable register that has break conditions match flags and bits for setting a variety of break conditions.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	UTRGW[1:0]		UBIDB	-	UBIDA	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCM FCA	SCM FCB	SCM FDA*	SCM FDB*	PCTE*	PCBA	-	-	DBEA*	PCBB	DBEB*	-	SEQ*	-	-	ETBE*
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R/W	R	R	R/W

Note: * In the masked ROM version, this bit is used as a reserved bit. This bit is always read as 0. The write value should always be 0.

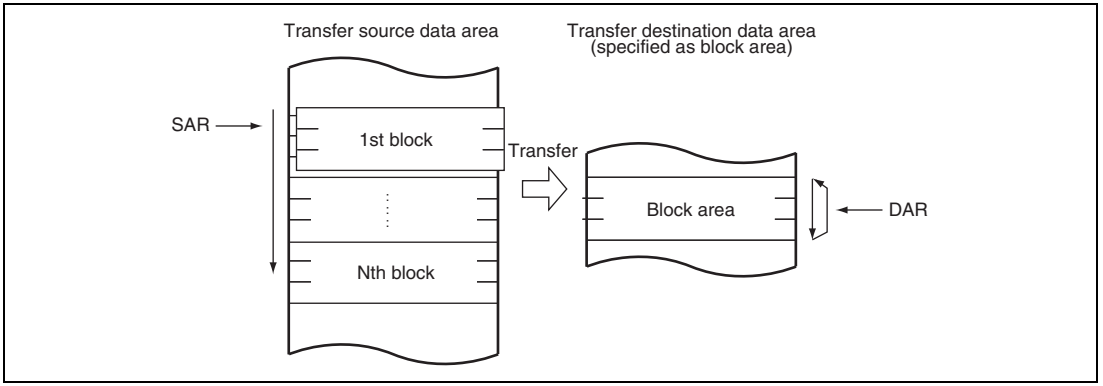

Figure 8.8 Memory Map in Block Transfer Mode (When Transfer Destination Is Specified as Block Area)

8.5.6 Chain Transfer

Setting the CHNE bit in MRB to 1 enables a number of data transfers to be performed consecutively in response to a single transfer request. Setting the CHNE and CHNS bits in MRB set to 1 enables a chain transfer only when the transfer counter reaches 0. SAR, DAR, CRA, CRB, MRA, and MRB, which define data transfers, can be set independently. Figure 8.9 shows the chain transfer operation.

In the case of transfer with CHNE set to 1, an interrupt request to the CPU is not generated at the end of the specified number of transfers or by setting the DISEL bit to 1, and the interrupt source flag for the activation source and DTCER are not affected.

In repeat transfer mode, setting the RCHNE bit in DTCCR and the CHNE and CHNS bits in MRB to 1 enables a chain transfer after transfer with transfer counter = 1 has been completed.

Bit	Bit Name	Initial Value	R/W	Description
11	DTBST	0	R/W	DTC Burst Enable Selects whether or not the DTC retains the bus mastership and remains continuously active until all transfer operations are complete when multiple DTC activation requests have been generated. 0: Release the bus on the completion of transfer for each individual DTC activation source. 1: Keep the DTC continuously active, i.e. only release the bus on completion of processing for all DTC activation sources. Notes: When this bit is set to 1, the following restrictions apply. 1. Clock setting with the frequency control register (FRQCR) must be Iϕ: Bϕ: Pϕ: MIϕ: MPϕ: = 8: 4: 4: 4: 4, 4: 2: 2: 2: 2, or 2: 1: 1: 1: 1 2. The vector information must be in on-chip ROM or on-chip RAM. 3. The transfer information must be in on-chip RAM. 4. Transfer must be between the on-chip RAM and an on-chip peripheral module or between external memory and an on-chip peripheral module.
10	DTSA	0	R/W	DTC Short Address Mode In this mode, the information that specifies a DTC transfer takes up only 3 longwords. 0: Transfer information is read out as 4 longwords. The transfer information is arranged as shown in figure 8.2 (normal address mode). 1: Transfer information is read out as 3 longwords. The transfer information is arranged as shown in figure 8.2 (short address mode). Note: Transfer in short address mode is only available between on-chip peripheral modules and on-chip RAM, because the higher-order 8 bits of the SAR and DAR are considered to be all 1.

Input Capture Function:

The TCNT value can be transferred to TGR on detection of the TIOC pin input edge.

Rising edge, falling edge, or both edges can be selected as the detected edge. For channels 0 and 1, it is also possible to specify another channel's counter input clock or compare match signal as the input capture source.

Note: When another channel's counter input clock is used as the input capture input for channels 0 and 1, MPϕ/1 should not be selected as the counter input clock used for input capture input. Input capture will not be generated if MPϕ/1 is selected.

1. Example of Input Capture Operation Setting Procedure
   Figure 10.10 shows an example of the input capture operation setting procedure.

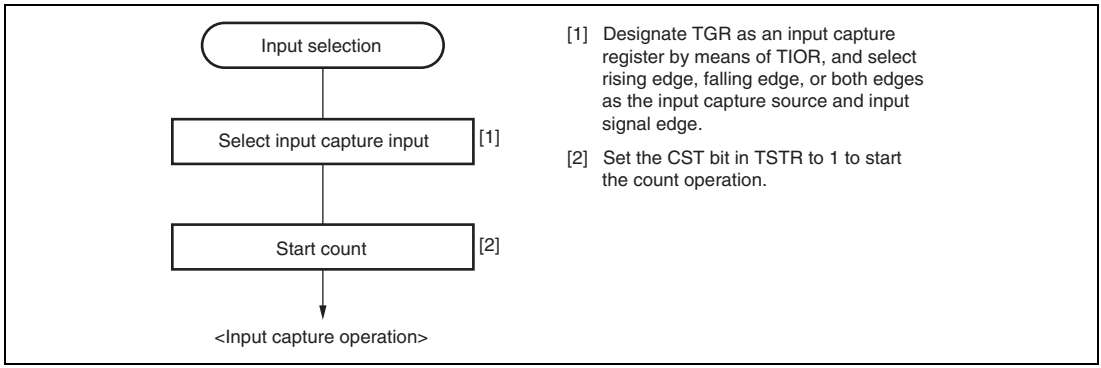

Figure 10.10 Example of Input Capture Operation Setting Procedure

Note: This function must be used in combination with interrupt skipping.
When interrupt skipping is disabled (the T3AEN and T4VEN bits in the timer interrupt skipping set register (TITCR) are cleared to 0 or the skipping count set bits (3ACOR and 4VCOR) in TITCR are cleared to 0), make sure that A/D converter start requests are not linked with interrupt skipping (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the timer A/D converter start request control register (TADCR) to 0).

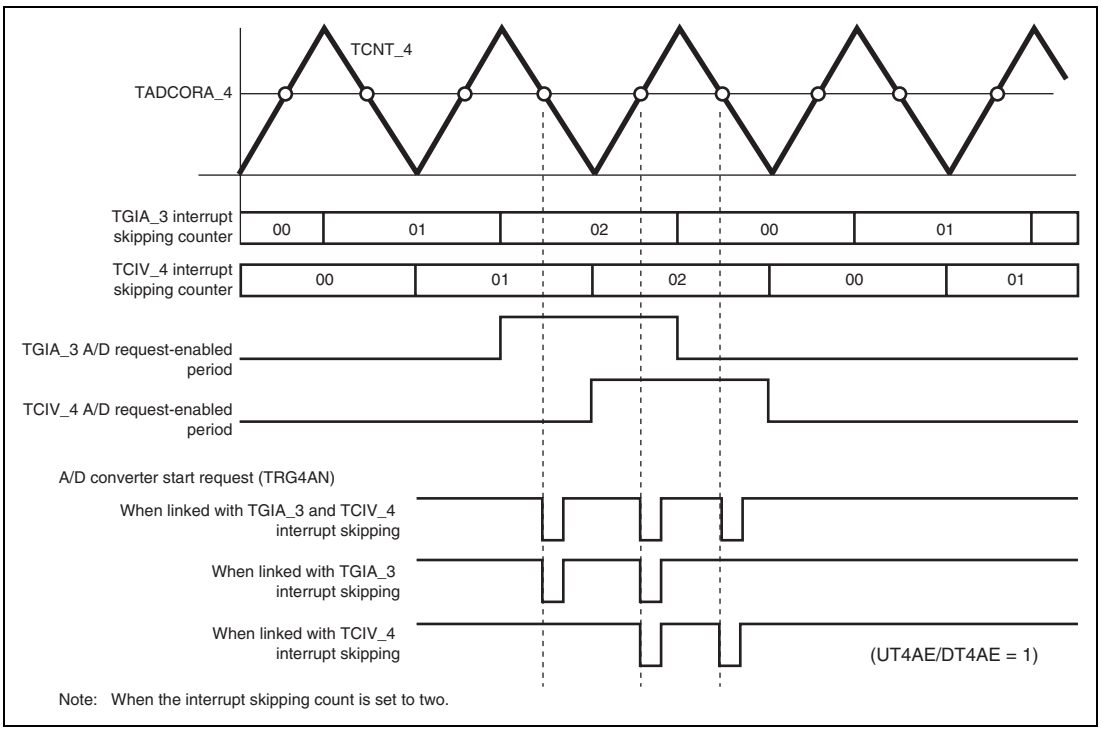

Figure 10.81 Example of A/D Converter Start Request Signal (TRG4AN) Operation Linked with Interrupt Skipping

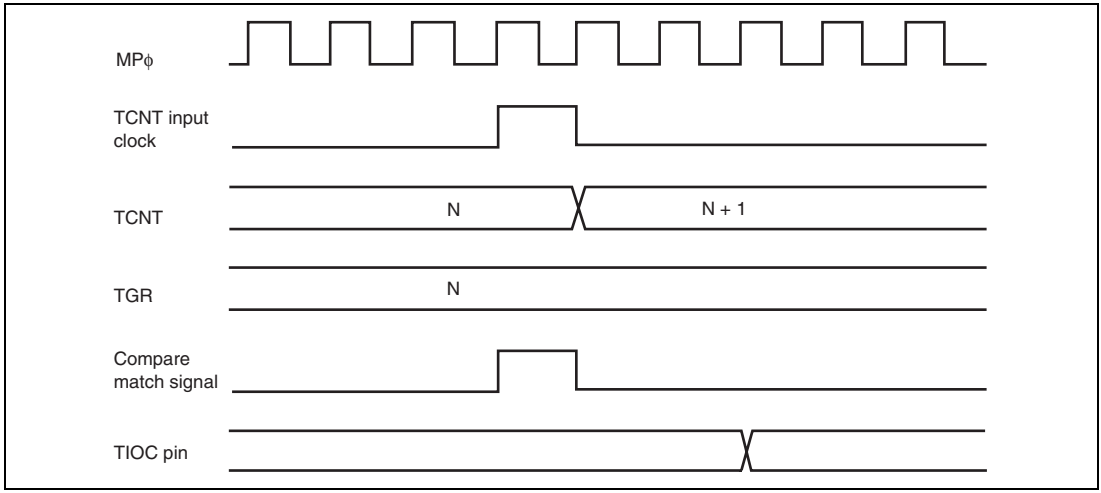

Figure 10.98 Output Compare Output Timing (Complementary PWM Mode/Reset Synchronous PWM Mode)

Input Capture Signal Timing: Figure 10.99 shows input capture signal timing.

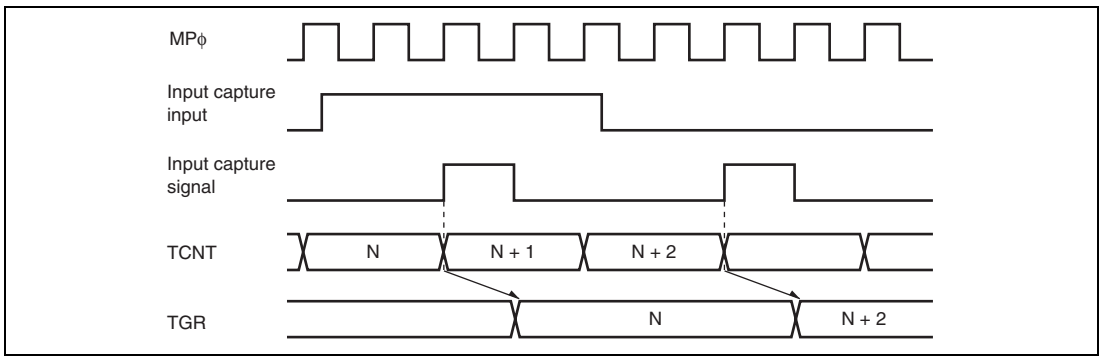

Figure 10.99 Input Capture Input Signal Timing

13.5 Interrupt Source

The WDT has one interrupt source: the interval timer interrupt (ITI).

Table 13.3 shows this interrupt source. An interval timer interrupt (ITI) is generated when the interval timer overflow flag bit (IOVF) in the watchdog timer control status register (WTSCR) is set to 1.

The interrupt request is canceled by clearing the interrupt flag to 0.

Table 13.3 Interrupt Source

Name	Interrupt Source	Interrupt Enable Bit	Interrupt Flag Bit
ITI	Interval timer interrupt	—	Interval timer overflow flag (IOVF)

13.6 Usage Note

13.6.1 WTCNT Setting Value

If WTCNT is set to H'FF in interval timer mode, overflow does not occur when WTCNT changes from H'FF to H'00 after one cycle of count clock, but overflow occurs when WTCNT changes from H'FF to H'00 after 257 cycles of count clock.

If WTCNT is set to H'FF in watchdog timer mode, overflow occurs when WTCNT changes from H'FF to H'00 after one cycle of count clock.

Figure 14.5 shows an example of the operation for transmission.

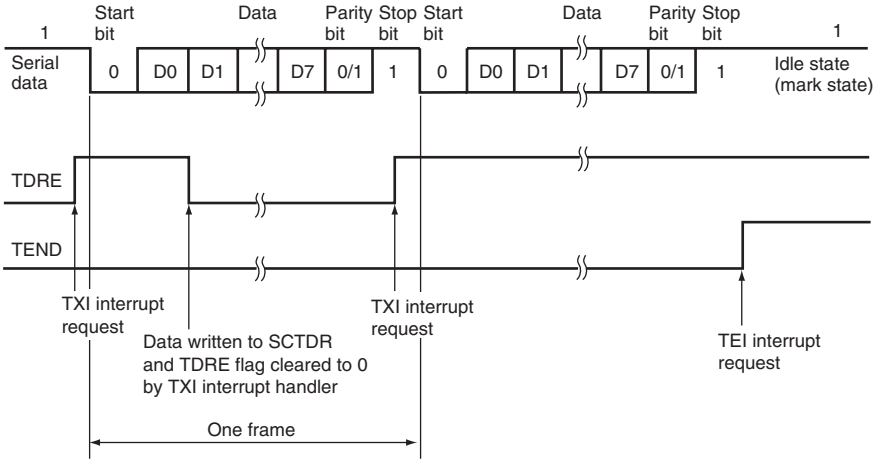

Figure 14.5 Example of Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

Figure 15.1 shows a block diagram of the A/D converter.

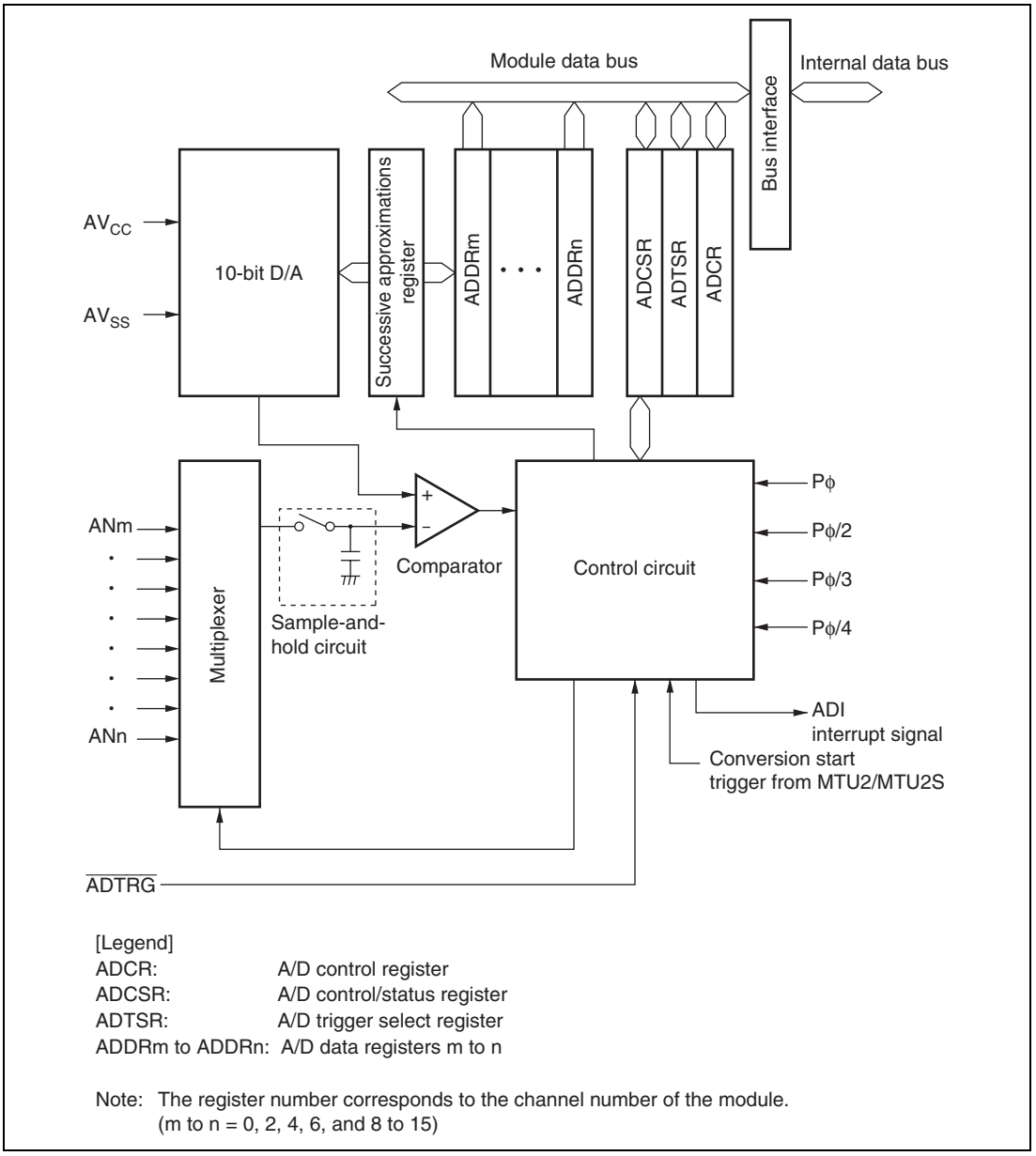

Figure 15.1 Block Diagram of A/D Converter (for One Module)

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	TRG01S[3:0]	0000	R/W	A/D Trigger 0 Group 1 Select 3 to 0 Select an external trigger, MTU2 trigger, or MTU2S trigger to start A/D conversion for group 1 when A/D module 0 is in 2-channel scan mode. 0000: External trigger pin ($\overline{\text{ADTRG}}$) input 0001: TGRA input capture/compare match for each MTU2 channel or TCNT_4 trough in complementary PWM mode (TRGAN) 0010: MTU2 CH0 compare match (TRG0N) 0011: MTU2 A/D conversion start request delaying (TRG4AN) 0100: MTU2 A/D conversion start request delaying (TRG4BN) 0101: TGRA input capture/compare match on each MTU2S channel or TCNT_4 trough in complementary PWM mode (TRGAN) 0110: Setting prohibited 0111: MTU2S A/D conversion start request delaying (TRG4AN) 1000: MTU2S A/D conversion start request delaying (TRG4BN) 1001: Setting prohibited 101x: Setting prohibited 11xx: Setting prohibited When switching the selector, first clear the ADST bit in the A/D control register (ADCR) to 0. Specify different trigger sources for the group 0 and group 1 conversion requests so that a group 0 conversion request is not generated simultaneously with a group 1 conversion request in 2-channel scan mode.

16.2.3 Compare Match Counter (CMCNT)

CMCNT is a 16-bit register used as an up-counter. When the counter input clock is selected with bits CKS1 and CKS0 in CMCSR and the STR bit in CMSTR is set to 1, CMCNT starts counting using the selected clock.

When the value in CMCNT and the value in compare match constant register (CMCOR) match, CMCNT is cleared to H'0000 and the CMF flag in CMCSR is set to 1.

The initial value of CMCNT is H'0000.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.2.4 Compare Match Constant Register (CMCOR)

CMCOR is a 16-bit register that sets the interval up to a compare match with CMCNT.

The initial value of CMCOR is H'FFFF.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PB4MD2	0	R/W	PB4 Mode
1	PB4MD1	0	R/W	Select the function of the PB4/A18/IRQ2/$\overline{\text{POE4}}$/TIC5US pin.
0	PB4MD0	0	R/W	000: PB4 I/O (port) 001: IRQ2 input (INTC) 011: TIC5US input (MTU2S) 101: A18 output (BSC)* 111: $\overline{\text{POE4}}$ input (POE) Other than above: Setting prohibited

Note: * This function is enabled only in the on-chip ROM enabled/disabled external-extension mode. Do not set 1 in single-chip mode.

- Port B Control Register L1 (PBCRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PB3 MD2	PB3 MD1	PB3 MD0	-	PB2 MD2	PB2 MD1	PB2 MD0	-	PB1 MD2	PB1 MD1	PB1 MD0	-	PB0 MD2	PB0 MD1	PB0 MD0
Initial value:	0	0*	0	0*	0	0*	0	0*	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Note: * The initial value is 1 in the on-chip ROM disabled external-extension mode.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PB3MD2	0*[1]	R/W	PB3 Mode
13	PB3MD1	0	R/W	Select the function of the PB3/A17/IRQ1/$\overline{\text{POE1}}$/TIC5V pin.
12	PB3MD0	0*[1]	R/W	000: PB3 I/O (port) 001: IRQ1 input (INTC) 010: $\overline{\text{POE1}}$ input (POE) 011: TIC5V input (MTU2) 101: A17 output (BSC)*[2] Other than above: Setting prohibited

- PBDRH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	PB18DR	PB17DR	PB16DR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	PB18DR	0	R/W	See table 18.4.
1	PB17DR	0	R/W	
0	PB16DR	0	R/W	

- PBDRL (SH7146)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	PB5DR	PB4DR	PB3DR	PB2DR	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PB5DR	0	R/W	See table 18.4.
4	PB4DR	0	R/W	
3	PB3DR	0	R/W	
2	PB2DR	0	R/W	
1, 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Table 19.7 Overlapping of RAM Area and User MAT Area

RAM Area	Block Name	RAMS	RAM2	RAM1	RAM0
H'FFFFA000 to H'FFFFAFFF	RAM area (4 kbytes)	0	x	x	x
H'00000000 to H'00000FFF	EB0 (4 kbytes)	1	0	0	0
H'00001000 to H'00001FFF	EB1 (4 kbytes)	1	0	0	1
H'00002000 to H'00002FFF	EB2 (4 kbytes)	1	0	1	0
H'00003000 to H'00003FFF	EB3 (4 kbytes)	1	0	1	1
H'00004000 to H'00004FFF	EB4 (4 kbytes)	1	1	0	0
H'00005000 to H'00005FFF	EB5 (4 kbytes)	1	1	0	1
H'00006000 to H'00006FFF	EB6 (4 kbytes)	1	1	1	0
H'00007000 to H'00007FFF	EB7 (4 kbytes)	1	1	1	1

Note: x: Don't care.

Section 20 Masked ROM

This LSI is available with 256 kbytes of on-chip masked ROM. The on-chip ROM is connected to the CPU and data transfer controller (DTC) through a 32-bit data bus (figure 20.1). The CPU and DTC can access the on-chip ROM in 8, 16, and 32-bit widths. Data in the on-chip ROM can always be accessed from the CPU in one cycle.

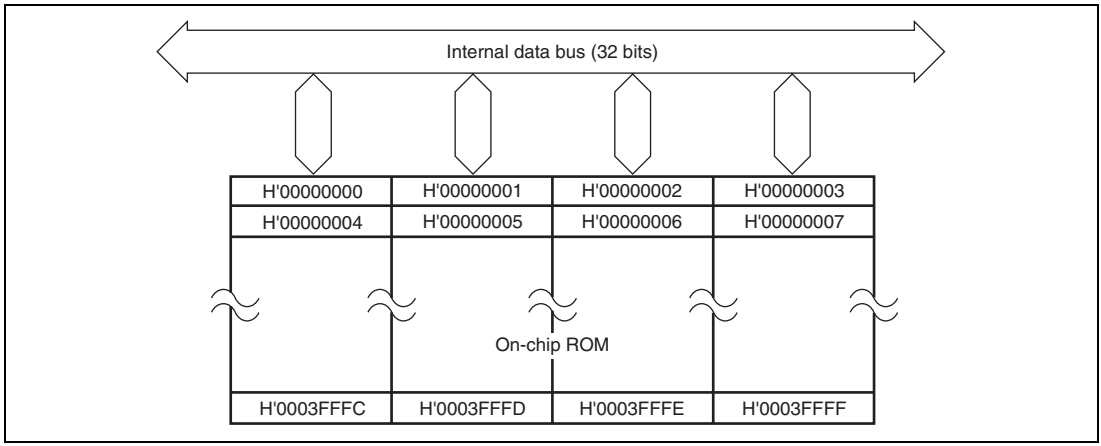

Figure 20.1 Masked ROM Block Diagram

The operating mode determines whether the on-chip ROM is valid or not. The operating mode is selected using mode-setting pins FWE, MD1, and MD0. If you are using the on-chip ROM, select mode 2 or mode 3; if you are not, select mode 0 or 1. The on-chip ROM is allocated to addresses H'00000000 to H'0003FFFF of memory area 0.

Section 22 Power-Down Modes

This LSI supports the following power-down modes: sleep mode, software standby mode, deep software standby mode, and module standby mode.

22.1 Features

- Supports sleep mode, software standby mode, module standby mode, and deep software standby mode.

22.1.1 Types of Power-Down Modes

This LSI has the following power-down modes.

- Sleep mode
- Software standby mode
- Deep software standby mode
- Module standby mode

Table 22.1 shows the methods to make a transition from the program execution state, as well as the CPU and peripheral module states in each mode and the procedures for canceling each mode.

Table 22.1 States of Power-Down Modes

		State					
Mode	**Transition Method**	**CPG**	**CPU**	**CPU Register**	**On-Chip Memory**	**On-Chip Peripheral Modules**	**Canceling Procedure**
Sleep	Execute SLEEP instruction with STBY bit in STBCR1 cleared to 0.	Runs	Halts	Held	Runs	Run	• Reset
Software standby	Execute SLEEP instruction with STBY bit in STBCR1 and STBYMD bit in STBCR6 set to 1.	Halts	Halts	Held	Halts (contents retained)	Halt	• Interrupt by NMI or IRQ • Power-on reset by the $\overline{\text{RES}}$ pin
Deep software standby	Execute SLEEP instruction with STBY bit in STBCR1 set to 1 and STBYMD bit in STBCR6 cleared to 0.	Halts	Halts	Undefined	Halts (contents undefined)	Halt	• Power-on reset by the $\overline{\text{RES}}$ pin
Module standby	Set MSTP bits in STBCR2 to STBCR5 to 1.	Runs	Runs	Held	Specified module halts (contents retained)	Specified module halts	• Clear MSTP bit to 0 • Power-on reset (for modules whose MSTP bit has an initial value of 0)

Note: For details on the states of on-chip peripheral module registers in each mode, refer to section 23.3, Register States in Each Operating Mode. For details on the pin states in each mode, refer to appendix A, Pin States.

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