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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71464ad80fpv

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions may occur due to the false recognition of the pin state as an input signal. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

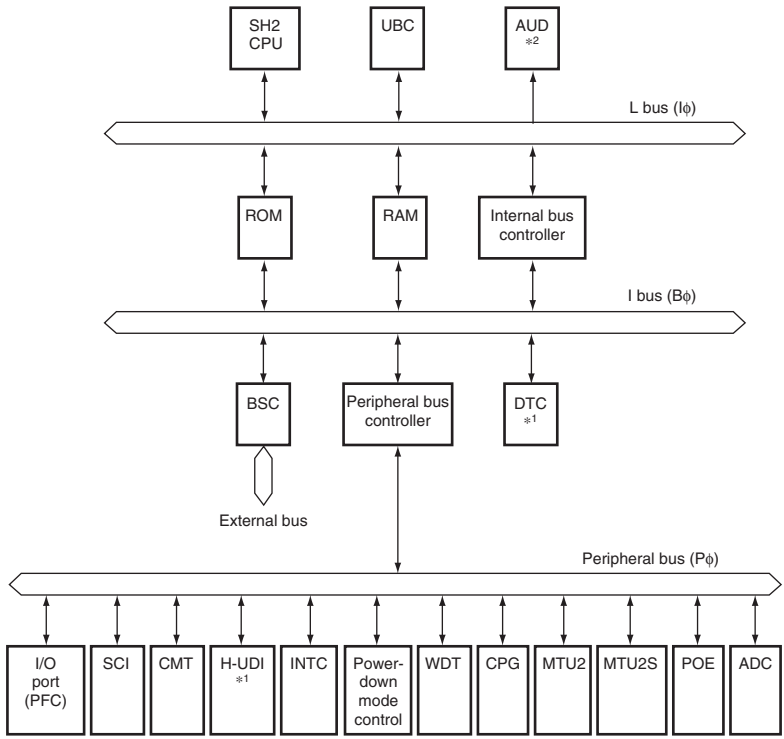
5. Differences between Products

   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

1.2 Block Diagram

The block diagram of this LSI is shown in figure 1.1.



[Legend]

ROM: On-chip ROM
RAM: On-chip RAM
UBC: User break controller
AUD: Advanced user debugger
H-UDI: User debugging interface
INTC: Interrupt controller
CPG: Clock pulse generator
WDT: Watchdog timer
CPU: Central processing unit
BSC: Bus state controller
DTC: Data transfer controller
PFC: Pin function controller
MTU2: Multi-function timer pulse unit 2
MTU2S: Multi-function timer pulse unit 2 (subset)
POE: Port output enable
SCI: Serial communication interface
CMT: Compare match timer
ADC: A/D converter

Notes: 1. Only in F-ZTAT version.
2. Only in F-ZTAT version supporting full functions of E10A.

Figure 1.1 Block Diagram

6.3.1 Interrupt Control Register 0 (ICR0)

ICR0 is a 16-bit register that sets the input signal detection mode of the external interrupt input pin NMI and indicates the input signal level on the NMI pin.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NMIL	-	-	-	-	-	-	NMIE	-	-	-	-	-	-	-	-
Initial value:	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Note: * The initial value is 1 when the level on the NMI pin is high, and 0 when the level on the pin is low.

Bit	Bit Name	Initial Value	R/W	Description
15	NMIL	*	R	NMI Input Level Indicates the state of the signal input to the NMI pin. This bit can be read to determine the NMI pin level. This bit cannot be modified. 0: State of the NMI input is low 1: State of the NMI input is high
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	NMIE	0	R/W	NMI Edge Select 0: Interrupt request is detected on the falling edge of the NMI input 1: Interrupt request is detected on the rising edge of the NMI input
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

6.6 Interrupt Operation

6.6.1 Interrupt Sequence

The sequence of interrupt operations is explained below. Figure 6.3 is a flowchart of the operations.

1. The interrupt request sources send interrupt request signals to the interrupt controller.
2. The interrupt controller selects the highest priority interrupt from interrupt requests sent, according to the priority levels set in interrupt priority registers A, D to F, and H to L (IPRA, IPRD to IPRF, and IPRH to IPRL). Interrupts that have lower-priority than that of the selected interrupt are ignored*. If interrupts that have the same priority level or interrupts within a same module occur simultaneously, the interrupt with the highest priority is selected according to the default priority shown in table 6.3.
3. The interrupt controller compares the priority level of the selected interrupt request with the interrupt mask bits (I3 to I0) in the status register (SR) of the CPU. If the priority level of the selected request is equal to or less than the level set in bits I3 to I0, the request is ignored. If the priority level of the selected request is higher than the level in bits I3 to I0, the interrupt controller accepts the request and sends an interrupt request signal to the CPU.
4. When the interrupt controller accepts an interrupt, a low level is output from the IRQOUT pin.
5. The CPU detects the interrupt request sent from the interrupt controller in the decode stage of an instruction to be executed. Instead of executing the decoded instruction, the CPU starts interrupt exception handling.
6. SR and PC are saved onto the stack.
7. The priority level of the accepted interrupt is copied to bits (I3 to I0) in SR.
8. When the accepted interrupt is sensed by level or is from an on-chip peripheral module, a high level is output from the IRQOUT pin. When the accepted interrupt is sensed by edge, a high level is output from the IRQOUT pin at the moment when the CPU starts interrupt exception processing instead of instruction execution as noted in 5. above. However, if the interrupt controller accepts an interrupt with a higher priority than the interrupt just to be accepted, the IRQOUT pin holds low level.
9. The CPU reads the start address of the exception handling routine from the exception vector table for the accepted interrupt, branches to that address, and starts executing the program. This branch is not a delayed branch.

Table 10.25 TIORL_3 (Channel 3)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_3 Function**	**TIOC3C Pin Function**
0	0	0	0	Output compare register*2	Output retained*1
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_3 is set to 1 and TGRC_3 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Bit	Bit Name	Initial Value	R/W	Description
2	TGIEC	0	R/W	TGR Interrupt Enable C Enables or disables interrupt requests (TGIC) by the TGFC bit when the TGFC bit in TSR is set to 1 in channels 0, 3, and 4. In channels 1 and 2, bit 2 is reserved. It is always read as 0 and the write value should always be 0. 0: Interrupt requests (TGIC) by TGFC bit disabled 1: Interrupt requests (TGIC) by TGFC bit enabled
1	TGIEB	0	R/W	TGR Interrupt Enable B Enables or disables interrupt requests (TGIB) by the TGFB bit when the TGFB bit in TSR is set to 1. 0: Interrupt requests (TGIB) by TGFB bit disabled 1: Interrupt requests (TGIB) by TGFB bit enabled
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) by the TGFA bit when the TGFA bit in TSR is set to 1. 0: Interrupt requests (TGIA) by TGFA bit disabled 1: Interrupt requests (TGIA) by TGFA bit enabled

(3.3) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter indicates the return value of the program processing result.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	MD	EE	FK	-	WD	WA	SF
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	Undefined	R/W	Unused Return 0.
6	MD	Undefined	R/W	Programming Mode Related Setting Error Detect Returns the check result of whether the signal input to the FWE pin is high and whether the error protection state is not entered. When a low-level signal is input to the FWE pin or the error protection state is entered, 1 is written to this bit. The input level to the FWE pin and the error protection state can be confirmed with the FWE bit (bit 7) and the FLER bit (bit 4) in FCCS, respectively. For conditions to enter the error protection state, see section 19.6.3, Error Protection. 0: FWE and FLER settings are normal (FWE = 1, FLER = 0) 1: FWE = 0 or FLER = 1, and programming cannot be performed

Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access States	Connected Bus Width
Timer interrupt skipping counter	TITCNT	8	H'FFFFC231	MTU2	8	MPϕ reference	16 bits
Timer buffer transfer set register	TBTER	8	H'FFFFC232		8	B:2	
Timer dead time enable register	TDER	8	H'FFFFC234		8	W:2	
Timer output level buffer register	TOLBR	8	H'FFFFC236		8	L:4	
Timer buffer operation transfer mode register_3	TBTM_3	8	H'FFFFC238		8, 16		
Timer buffer operation transfer mode register_4	TBTM_4	8	H'FFFFC239		8		
Timer A/D converter start request control register	TADCR	16	H'FFFFC240		16		
Timer A/D converter start request cycle set register A_4	TADCORA_4	16	H'FFFFC244		16, 32		
Timer A/D converter start request cycle set register B_4	TADCORB_4	16	H'FFFFC246		16		
Timer A/D converter start request cycle set buffer register A_4	TADCOBRA_4	16	H'FFFFC248		16, 32		
Timer A/D converter start request cycle set buffer register B_4	TADCOBRB_4	16	H'FFFFC24A		16		
Timer waveform control register	TWCR	8	H'FFFFC260		8		
Timer start register	TSTR	8	H'FFFFC280		8, 16		
Timer synchronous register	TSYR	8	H'FFFFC281		8		
Timer counter synchronous start register	TCSYSTR	8	H'FFFFC282		8		
Timer read/write enable register	TRWER	8	H'FFFFC284		8		
Timer control register_0	TCR_0	8	H'FFFFC300		8, 16, 32		
Timer mode register_0	TMDR_0	8	H'FFFFC301		8		
Timer I/O control register H_0	TIORH_0	8	H'FFFFC302		8, 16		
Timer I/O control register L_0	TIORL_0	8	H'FFFFC303		8		
Timer interrupt enable register_0	TIER_0	8	H'FFFFC304		8, 16, 32		
Timer status register_0	TSR_0	8	H'FFFFC305		8		
Timer counter_0	TCNT_0	16	H'FFFFC306		16		
Timer general register A_0	TGRA_0	16	H'FFFFC308		16, 32		
Timer general register B_0	TGRB_0	16	H'FFFFC30A		16		

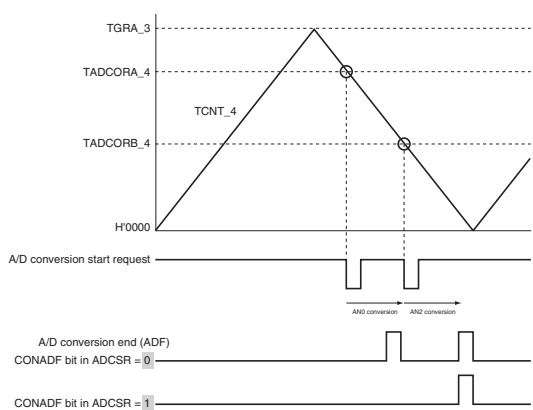
Register Name	Abbreviation	No. of Bits	Address	Module	Access Size	No. of Access States	Connected Bus Width
Timer general register B_4S	TGRB_4S	16	H'FFFFC61E	MTU2S	16	MIϕ reference	16 bits
Timer sub-counter S	TCNTSS	16	H'FFFFC620		16, 32	B:2	
Timer cycle buffer register S	TCBRS	16	H'FFFFC622		16	W:2	
Timer general register C_3S	TGRC_3S	16	H'FFFFC624		16, 32	L:4	
Timer general register D_3S	TGRD_3S	16	H'FFFFC626		16		
Timer general register C_4S	TGRC_4S	16	H'FFFFC628		16, 32		
Timer general register D_4S	TGRD_4S	16	H'FFFFC62A		16		
Timer status register_3S	TSR_3S	8	H'FFFFC62C		8, 16		
Timer status register_4S	TSR_4S	8	H'FFFFC62D		8		
Timer interrupt skipping set register S	TITCRS	8	H'FFFFC630		8, 16		
Timer interrupt skipping counter S	TITCNTS	8	H'FFFFC631		8		
Timer buffer transfer set register S	TBTERS	8	H'FFFFC632		8		
Timer dead time enable register S	TDERS	8	H'FFFFC634		8		
Timer output level buffer register S	TOLBRS	8	H'FFFFC636		8		
Timer buffer operation transfer mode register_3S	TBTM_3S	8	H'FFFFC638		8, 16		
Timer buffer operation transfer mode register_4S	TBTM_4S	8	H'FFFFC639		8		
Timer A/D converter start request control register S	TADCRS	16	H'FFFFC640		16		
Timer A/D converter start request cycle set register A_4S	TADCORA_4S	16	H'FFFFC644		16, 32		
Timer A/D converter start request cycle set register B_4S	TADCORB_4S	16	H'FFFFC646		16		
Timer A/D converter start request cycle set buffer register A_4S	TADCOBRA_4S	16	H'FFFFC648		16, 32		
Timer A/D converter start request cycle set buffer register B_4S	TADCOBRB_4S	16	H'FFFFC64A		16		
Timer synchronous clear register S	TSYCRS	8	H'FFFFC650		8		
Timer waveform control register S	TWCRS	8	H'FFFFC660		8		
Timer start register S	TSTRS	8	H'FFFFC680		8, 16		
Timer synchronous register S	TSYRS	8	H'FFFFC681		8		
Timer read/write enable register S	TRWERS	8	H'FFFFC684		8		

Pin Function		Pin State						
		Reset State		Power-Down State				
Type	Pin Name	Power-On	Manual	Deep Software Standby	Software Standby	Sleep	Oscillation Stop Detected	POE Function Used
MTU2	TIOC4A to TIOC4D	Z	I/O	Z	Z	I/O	Z	Z
	TIC5U, TIC5V	Z	I	Z	Z	I	I	I
MTU2S	TIOC3BS, TIOC3DS	Z	I/O	Z	Z	I/O	Z	Z
	TIOC4AS to TIOC4DS	Z	I/O	Z	Z	I/O	Z	Z
	TIC5US, TIC5VS	Z	I	Z	Z	I	I	I
POE	POE0 to POE2, POE4 to POE6, POE8 (PA9)	Z	I	Z	Z	I	I	I
	POE3, POE7, POE8 (PB18)	I*3	I*3	Z	Z	I*3	I*3	I*3
SCI	SCK0 to SCK2	Z	I/O	Z	Z	I/O	I/O	I/O
	RXD0 to RXD2	Z	I	Z	Z	I	I	I
	TXD0 to TXD2	Z	O	Z	O*1	O	O	O
UBC	UBCTRG	Z	O	Z	O*1	O	O	O
A/D Converter	AN0, AN2, AN4, AN6, AN8 to AN15	Z	I	Z	Z	I	I	I
	ADTRG	Z	I	Z	Z	I	I	I
I/O Port	PA0 to PA15	Z	I/O	Z	K*1	I/O	I/O	I/O
	PB2 to PB5, PB16 to PB18	Z	I/O	Z	K*1	I/O	I/O	I/O
	PE0 to PE3	Z	I/O	Z	K*1	I/O	I/O	Z
	PE4 to PE8, PE10	Z	I/O	Z	K*1	I/O	I/O	I/O
	PE9, PE11 to PE15	Z	I/O	Z	Z	I/O	Z	Z
	PE16 to PE21	Z	I/O	Z	Z	I/O	Z	Z
	PF0, PF2, PF4, PF6, PF8 to PF15	Z	I	Z	Z	I	I	I

Item	Page	Revision (See Manual for Details)
15.3.4 A/D Trigger Select Registers_0 and _1 (ADTSR_0 and ADTSR_1) • ADTSR_0	613	Bit table amended

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	TRG1S[3:0]	0000	R/W	A/D Trigger 1 Select 3 to 0 Select an external trigger, MTU2 trigger, or MTU2S trigger to start A/D conversion for A/D module 1. In 2-channel scan mode, these bits select an external trigger, MTU2 trigger, or MTU2S trigger to start A/D conversion for group 0. 0000: External trigger pin ($\overline{\text{ADTRG}}$) input 0001: TGRA input capture/compare match for each MTU2 channel or TCNT_4 trough in complementary PWM mode (TRGAN) 0010: MTU2 CH0 compare match (TRG0N) 0011: MTU2 A/D conversion start request delaying (TRG4AN) 0100: MTU2 A/D conversion start request delaying (TRG4BN) 0101: TGRA input capture/compare match on each MTU2S channel or TCNT_4 trough in complementary PWM mode (TRGAN) 0110: Setting prohibited 0111: MTU2S A/D conversion start request delaying (TRG4AN) 1000: MTU2S A/D conversion start request delaying (TRG4BN) 1001: Setting prohibited 101x: Setting prohibited 11xx: Setting prohibited When switching the selector, first clear the ADST bit in the A/D control register (ADCR) to 0. Specify different trigger sources for the group 0 and group 1 conversion requests so that a group 0 conversion request is not generated simultaneously with a group 1 conversion request in 2-channel scan mode.

15.4.7 2-Channel Scanning Figure 15.4 Example of 2-Channel Scanning	621	Figure amended



16.4 Interrupts 16.4.1 CMT Interrupt Sources and DTC Activation Table 16.2 Interrupt Source	635	Description and Table added …. The data transfer controller (DTC) can be activated by an interrupt request. In this case, the priority between channels is fixed. See section 8, Data Transfer Controller (DTC), for details. Table 16.2 lists the CMT interrupt sources.