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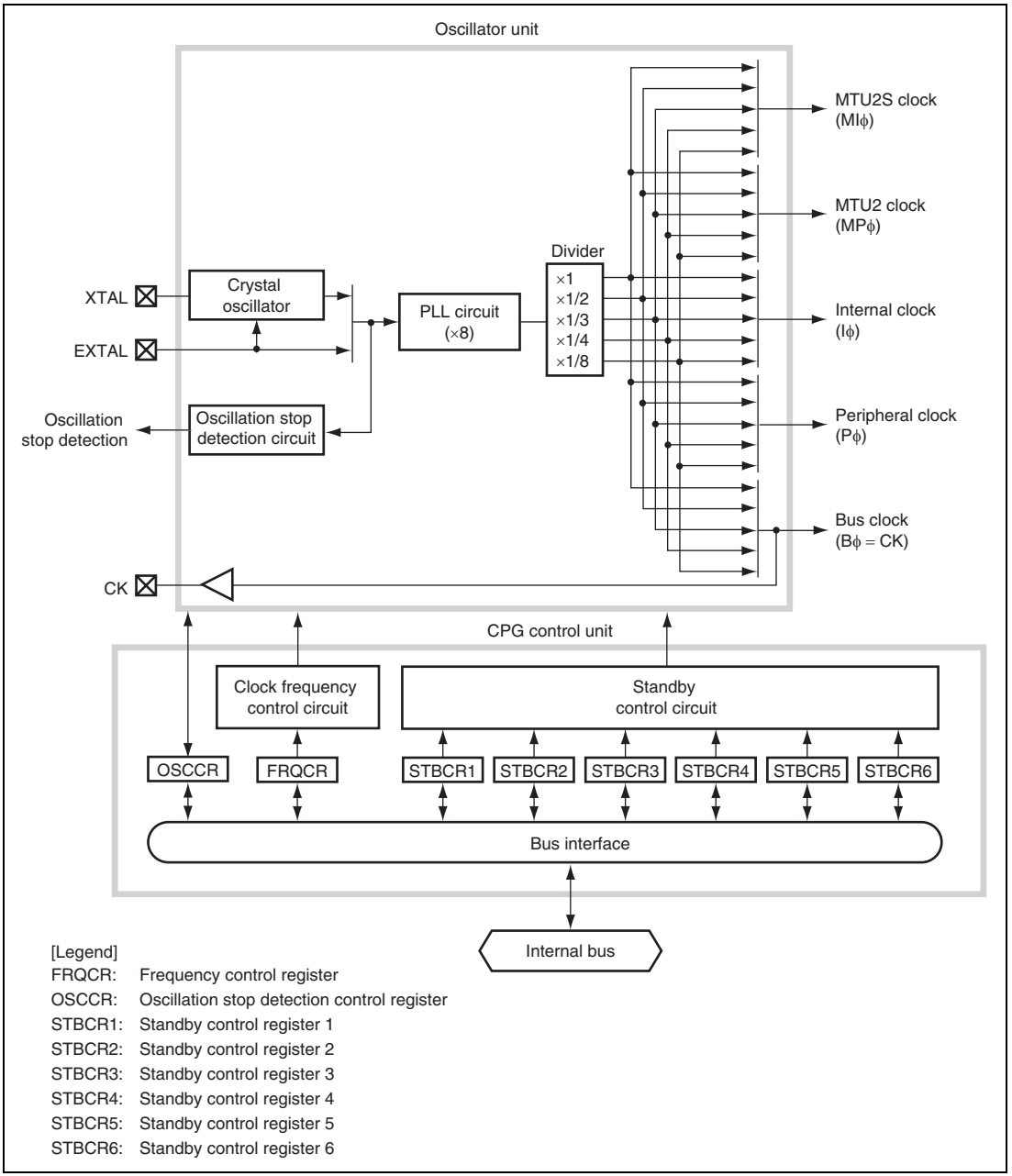
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71464an80fpv

Figure 4.1 shows a block diagram of the clock pulse generator.



[Legend]
FRQCR: Frequency control register
OSCCR: Oscillation stop detection control register
STBCR1: Standby control register 1
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4
STBCR5: Standby control register 5
STBCR6: Standby control register 6

Figure 4.1 Block Diagram of Clock Pulse Generator

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	UTRGW[1:0]	00	R/W	$\overline{\text{UBCTRG}}$ Output Pulse Width Select Select the $\overline{\text{UBCTRG}}$ output pulse width when the break condition matches. 00: Setting prohibited. 01: $\overline{\text{UBCTRG}}$ output pulse width is 3 to 4 t_{Bcyc} 10: $\overline{\text{UBCTRG}}$ output pulse width is 7 to 8 t_{Bcyc} 11: $\overline{\text{UBCTRG}}$ output pulse width is 15 to 16 t_{Bcyc} Note: t_{Bcyc} indicates the period of one cycle of the external bus clock (Bϕ = CK).
19	UBIDB	0	R/W	User Break Disable B Enables or disables the user break interrupt request when the channel B break conditions are satisfied. 0: User break interrupt request is enabled when break conditions are satisfied 1: User break interrupt request is disabled when break conditions are satisfied
18	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
17	UBIDA	0	R/W	User Break Disable A Enables or disables the user break interrupt request when the channel A break conditions are satisfied. 0: User break interrupt request is enabled when break conditions are satisfied 1: User break interrupt request is disabled when break conditions are satisfied
16	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

8.9.6 Access to DTC Registers through DTC

Do not access the DTC registers by using DTC operation.

8.9.7 Notes on IRQ Interrupt as DTC Activation Source

- The IRQ interrupt specified as a DTC activation source must not be used to cancel software standby mode.
- The IRQ edge input in software standby mode must not be specified as a DTC activation source.
- When a low level on the IRQ pin is to be detected, if the end of DTC transfer is used to request an interrupt to the CPU (transfer counter = 0 or DISEL = 1), the IRQ signal must be kept low until the CPU accepts the interrupt.

8.9.8 Notes on SCI as DTC Activation Sources

- When the TXI interrupt from the SCI is specified as a DTC activation source, the TEND flag in the SCI must not be used as the transfer end flag.

8.9.9 Clearing Interrupt Source Flag

The interrupt source flag set when the DTC transfer is completed should be cleared in the interrupt handler in the same way as for general interrupt source flags. For details, refer to section 6.9, Usage Note.

8.9.10 Conflict between NMI Interrupt and DTC Activation

When a conflict occurs between the generation of the NMI interrupt and the DTC activation, the NMI interrupt has priority. Thus the ERR bit is set to 1 and the DTC is not activated.

It takes 1 × Bcyc + 3 × Pcyc for determining DTC stop by NMI, 2 × Bcyc for determining DTC activation by IRQ, and 1 × Pcyc for determining DTC activation by peripheral modules.

8.9.11 Operation When a DTC Activation Request Is Cancelled While in Progress

Once the DTC has accepted an activation request, the DTC does not accept the next activation request until the sequence of DTC processing that ends with writeback has been completed.

Table 9.2 Address Map (Single-Chip Mode)

Address	Area	Memory Type	Capacity	Bus Width
H'00000000 to H'0003FFFF	On-chip ROM		256 kbytes	32 bits
H'00040000 to H'FFFF8FFF	Reserved			
H'FFFF9000 to H'FFFFAFFF	On-chip RAM		8 kbytes	32 bits
H'FFFFB000 to H'FFFFBFFF	Reserved			
H'FFFFC000 to H'FFFFFFFF	On-chip peripheral modules		16 kbytes	8 or 16 bits

Note: Do not access the reserved area. If the reserved area is accessed, the correct operation cannot be guaranteed. Only the on-chip ROM, on-chip RAM, and on-chip peripheral modules can be accessed; the other areas cannot be accessed.

Outline of Complementary PWM Mode Operation:

In complementary PWM mode, 6-phase PWM output is possible. Figure 10.39 illustrates counter operation in complementary PWM mode, and figure 10.40 shows an example of complementary PWM mode operation.

1. Counter Operation

   In complementary PWM mode, three counters—TCNT_3, TCNT_4, and TCNTS—perform up/down-count operations.

   TCNT_3 is automatically initialized to the value set in TDDR when complementary PWM mode is selected and the CST bit in TSTR is 0.

   When the CST bit is set to 1, TCNT_3 counts up to the value set in TGRA_3, then switches to down-counting when it matches TGRA_3. When the TCNT3 value matches TDDR, the counter switches to up-counting, and the operation is repeated in this way.

   TCNT_4 is initialized to H'0000.

   When the CST bit is set to 1, TCNT4 counts up in synchronization with TCNT_3, and switches to down-counting when it matches TCDR. On reaching H'0000, TCNT4 switches to up-counting, and the operation is repeated in this way.

   TCNTS is a read-only counter. It need not be initialized.

   When TCNT_3 matches TCDR during TCNT_3 and TCNT_4 up/down-counting, down-counting is started, and when TCNTS matches TCDR, the operation switches to up-counting. When TCNTS matches TGRA_3, it is cleared to H'0000.

   When TCNT_4 matches TDDR during TCNT_3 and TCNT_4 down-counting, up-counting is started, and when TCNTS matches TDDR, the operation switches to down-counting. When TCNTS reaches H'0000, it is set with the value in TGRA_3.

   TCNTS is compared with the compare register and temporary register in which the PWM duty is set during the count operation only.

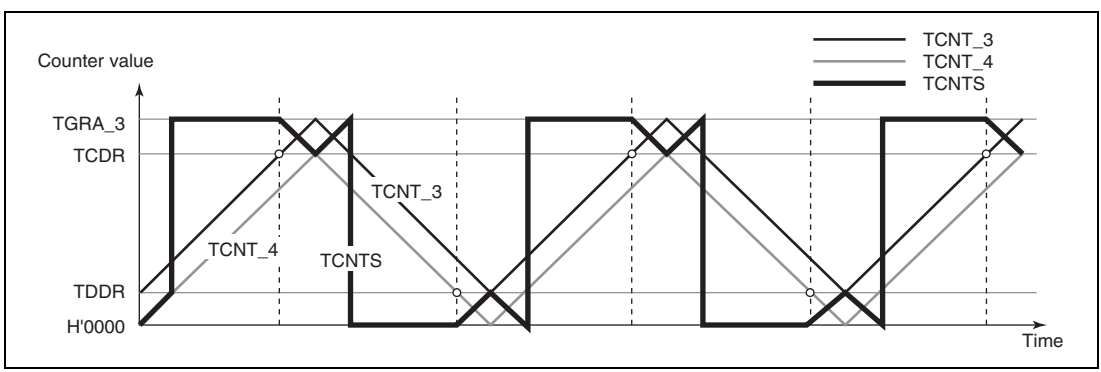


Figure 10.39 Complementary PWM Mode Counter Operation

3. Initialization

   In complementary PWM mode, there are six registers that must be initialized. In addition, there is a register that specifies whether to generate dead time (it should be used only when dead time generation should be disabled).

   Before setting complementary PWM mode with bits MD3 to MD0 in the timer mode register (TMDR), the following initial register values must be set.

   TGRC_3 operates as the buffer register for TGRA_3, and should be set with 1/2 the PWM carrier cycle + dead time Td. The timer cycle buffer register (TCBR) operates as the buffer register for the timer cycle data register (TCDR), and should be set with 1/2 the PWM carrier cycle. Set dead time Td in the timer dead time data register (TDDR).

   When dead time is not needed, the TDER bit in the timer dead time enable register (TDER) should be cleared to 0, TGRC_3 and TGRA_3 should be set to 1/2 the PWM carrier cycle + 1, and TDDR should be set to 1.

   Set the respective initial PWM duty values in buffer registers TGRD_3, TGRC_4, and TGRD_4.

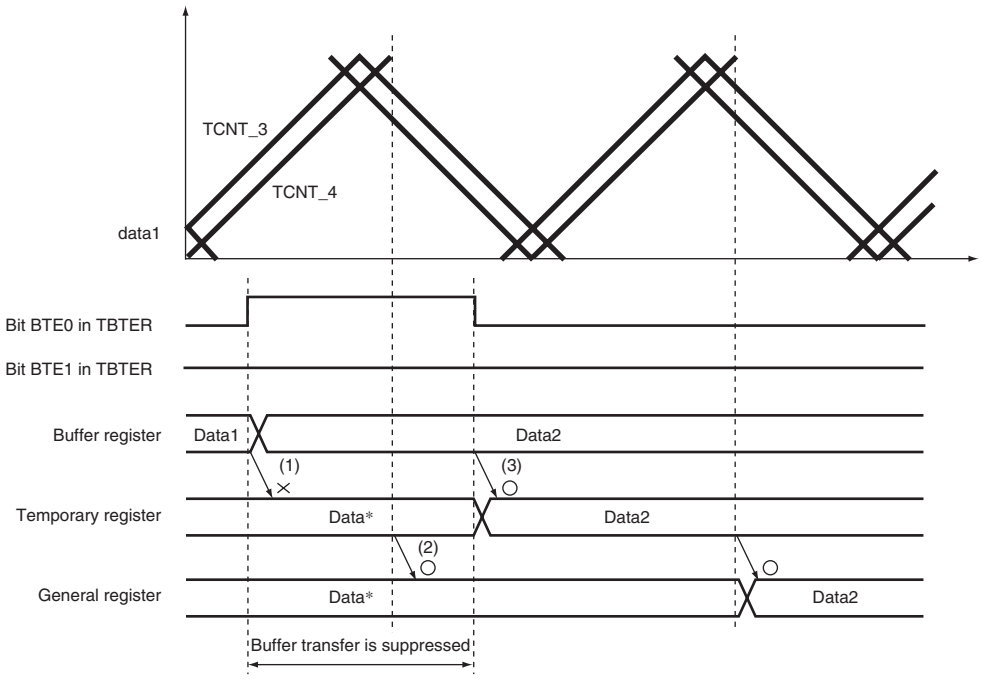
   The values set in the five buffer registers excluding TDDR are transferred simultaneously to the corresponding compare registers when complementary PWM mode is set.

   Set TCNT_4 to H'0000 before setting complementary PWM mode.

Table 10.56 Registers and Counters Requiring Initialization

Register/Counter	Set Value
TGRC_3	1/2 PWM carrier cycle + dead time Td (1/2 PWM carrier cycle + 1 when dead time generation is disabled by TDER)
TDDR	Dead time Td (1 when dead time generation is disabled by TDER)
TCBR	1/2 PWM carrier cycle
TGRD_3, TGRC_4, TGRD_4	Initial PWM duty value for each phase
TCNT_4	H'0000

Note: The TGRC_3 set value must be the sum of 1/2 the PWM carrier cycle set in TCBR and dead time Td set in TDDR. When dead time generation is disabled by TDER, TGRC_3 must be set to 1/2 the PWM carrier cycle + 1.



[Legend]

(1) No data is transferred from the buffer register to the temporary register in the buffer transfer-disabled period (bits BTE1 and BTE0 in TBTER are set to 0 and 1, respectively).
(2) Data is transferred from the temporary register to the general register even in the buffer transfer-disabled period.
(3) After buffer transfer is enabled, data is transferred from the buffer register to the temporary register.

Note: * When buffer transfer at the crest is selected.

Figure 10.76 Example of Operation when Buffer Transfer Is Suppressed (BTE1 = 0 and BTE0 = 1)

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Timer subcounter S	TCNTSS	R	H'0000	H'FFFFC620	16, 32
Timer cycle buffer register S	TCBRS	R/W	H'FFFF	H'FFFFC622	16
Timer general register C_3S	TGRC_3S	R/W	H'FFFF	H'FFFFC624	16, 32
Timer general register D_3S	TGRD_3S	R/W	H'FFFF	H'FFFFC626	16
Timer general register C_4S	TGRC_4S	R/W	H'FFFF	H'FFFFC628	16, 32
Timer general register D_4S	TGRD_4S	R/W	H'FFFF	H'FFFFC62A	16
Timer status register_3S	TSR_3S	R/W	H'C0	H'FFFFC62C	8, 16
Timer status register_4S	TSR_4S	R/W	H'C0	H'FFFFC62D	8
Timer interrupt skipping set register S	TITCRS	R/W	H'00	H'FFFFC630	8, 16
Timer interrupt skipping counter S	TITCNTS	R	H'00	H'FFFFC631	8
Timer buffer transfer set register S	TBTERS	R/W	H'00	H'FFFFC632	8
Timer dead time enable register S	TDERS	R/W	H'01	H'FFFFC634	8
Timer output level buffer register S	TOLBRS	R/W	H'00	H'FFFFC636	8
Timer buffer operation transfer mode register_3S	TBTM_3S	R/W	H'00	H'FFFFC638	8, 16
Timer buffer operation transfer mode register_4S	TBTM_4S	R/W	H'00	H'FFFFC639	8
Timer A/D converter start request control register S	TADCRS	R/W	H'0000	H'FFFFC640	16
Timer A/D converter start request cycle set register A_4S	TADCORA_4S	R/W	H'FFFF	H'FFFFC644	16, 32
Timer A/D converter start request cycle set register B_4S	TADCORB_4S	R/W	H'FFFF	H'FFFFC646	16
Timer A/D converter start request cycle set buffer register A_4S	TADCOBRA_4S	R/W	H'FFFF	H'FFFFC648	16, 32
Timer A/D converter start request cycle set buffer register B_4S	TADCOBRB_4S	R/W	H'FFFF	H'FFFFC64A	16

13.4 Operation

13.4.1 Revoking Software Standbys

The WDT can be used to revoke software standby mode with an NMI interrupt or external interrupt (IRQ). The procedure is described below. (The WDT does not run when resets are used for revoking, so keep the $\overline{\text{RES}}$ pin low until the clock stabilizes.)

1. Before transition to software standby mode, always clear the TME bit in WTCSR to 0. When the TME bit is 1, an erroneous reset or interval timer interrupt may be generated when the count overflows.
2. Set the type of count clock used in the CKS2 to CKS0 bits in WTCSR and the initial values for the counter in the WTCNT counter. These values should ensure that the time till count overflow is longer than the clock oscillation settling time.
3. Transition to software standby mode by executing a SLEEP instruction to stop the clock.
4. The WDT starts counting by detecting a change in the level input to the NMI or IRQ pin.
5. When the WDT count overflows, the CPG starts supplying the clock and the LSI resumes operation. The WOVF flag in WTCSR is not set when this happens.

13.4.2 Using Watchdog Timer Mode

While operating in watchdog timer mode, the WDT generates an internal reset of the type specified by the RSTS bit in WTCSR and asserts a signal through the $\overline{\text{WDTOVF}}$ pin every time the counter overflows.

1. Set the WT/IT bit in WTCSR to 1, set the reset type in the RSTS bit, set the type of count clock in the CKS2 to CKS0 bits, and set the initial value of the counter in the WTCNT counter.
2. Set the TME bit in WTCSR to 1 to start the count in watchdog timer mode.
3. While operating in watchdog timer mode, rewrite the counter periodically to prevent the counter from overflowing.
4. When the counter overflows, the WDT sets the WOVF flag in WTCSR to 1, asserts a signal through the $\overline{\text{WDTOVF}}$ pin for one cycle of the count clock specified by the CKS2 to CKS0 bits, and generates a reset of the type specified by the RSTS bit. The counter then resumes counting.

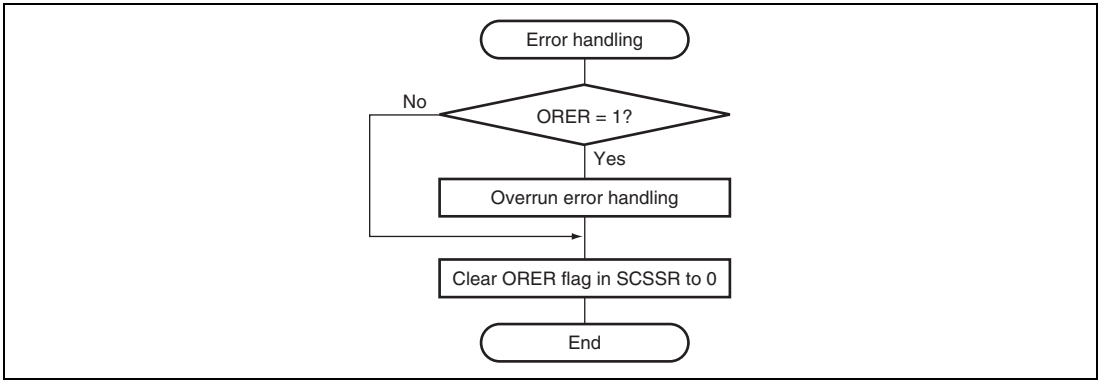


Figure 14.12 Sample Flowchart for Receiving Serial Data (2)

In receiving, the SCI operates as follows:

1. The SCI synchronizes with serial clock input or output and initializes internally.
2. Receive data is shifted into SCRSR in order from the LSB to the MSB. After receiving the data, the SCI checks whether the RDRF flag is 0 and the receive data can be transferred from SCRSR to SCRDR. If this check is passed, the SCI sets the RDRF flag to 1 and stores the received data in SCRDR. If a receive error is detected, the SCI operates as shown in table 14.16. In this state, subsequent reception cannot be continued. In addition, the RDRF flag will not be set to 1 after reception; be sure to clear the RDRF flag to 0.
3. After setting RDRF to 1, if the receive-data-full interrupt enable bit (RIE) is set to 1 in SCSCR, the SCI requests a receive-data-full interrupt (RXI). If the ORER bit is set to 1 and the RIE bit in SCSCR is also set to 1, the SCI requests a receive error interrupt (ERI).

17.1.9 IRQOUT Function Control Register (IFCR)

IFCR is a 16-bit readable/writable register that is used to control the IRQOUT pin output when it is selected as the multiplexed pin function by port E control register L4 (PECRL4). When PECRL4 selects another function, the IFCR setting does not affect the pin function.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	IRQ MD1	IRQ MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	IRQMD1	0	R/W	Port E $\overline{\text{IRQOUT}}$ Pin Function Select
0	IRQMD0	0	R/W	Select the $\overline{\text{IRQOUT}}$ pin function when bits 14 to 12 (PE15MD2 to PE15MD0) in PECRL4 are set to B'011. 00: Interrupt request accept signal output 01: Setting prohibited 10: Interrupt request accept signal output 11: Always high-level output

Bit	Bit Name	Initial Value	R/W	Description
15	PA15DR	0	R/W	See table 18.2.
14	PA14DR	0	R/W	
13	PA13DR	0	R/W	
12	PA12DR	0	R/W	
11	PA11DR	0	R/W	
10	PA10DR	0	R/W	
9	PA9DR	0	R/W	
8	PA8DR	0	R/W	
7	PA7DR	0	R/W	
6	PA6DR	0	R/W	
5	PA5DR	0	R/W	
4	PA4DR	0	R/W	
3	PA3DR	0	R/W	
2	PA2DR	0	R/W	
1	PA1DR	0	R/W	
0	PA0DR	0	R/W	

Table 18.2 Port A Data Register L (PADRL) Read/Write Operations

- PADRL Bits 15 to 0

PAIOR	Pin Function	Read	Write
0	General input	Pin state	Can write to PADRL, but it has no effect on pin state
	Other than general input	Pin state	Can write to PADRL, but it has no effect on pin state
1	General output	PADRL value	Value written is output from pin
	Other than general output	PADRL value	Can write to PADRL, but it has no effect on pin state

18.2 Port B

Port B in the SH7146 is an input/output port with the seven pins shown in figure 18.3.

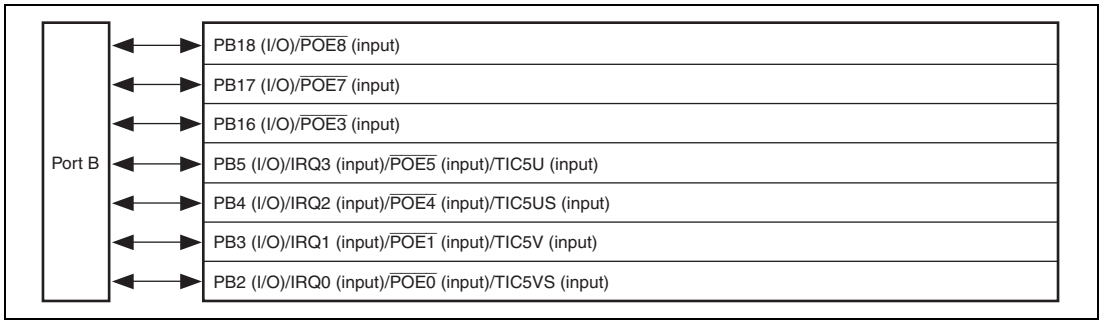


Figure 18.3 Port B (SH7146)

Port B in the SH7149 is an input/output port with the nine pins shown in figure 18.4.

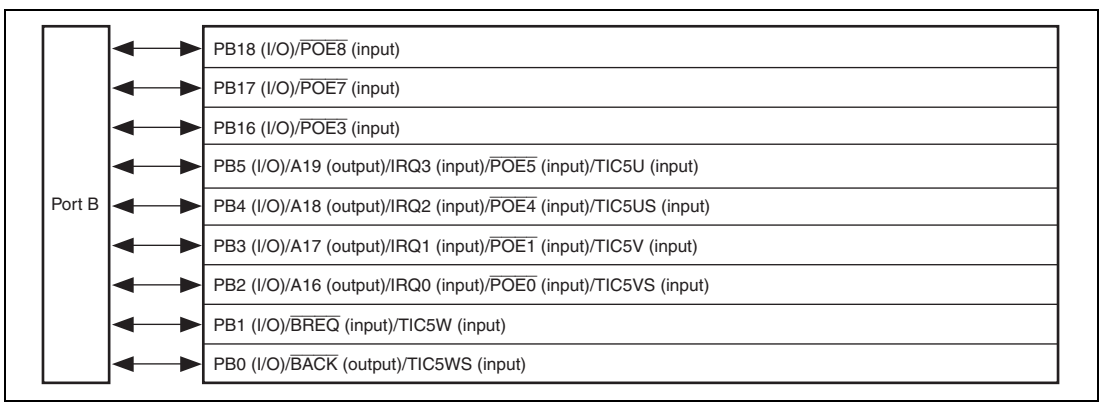


Figure 18.4 Port B (SH7149)

(4.2) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter returns the value of the erasing processing result.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	MD	EE	FK	EB	-	-	SF
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	Undefined	R/W	Unused Return 0.
6	MD	Undefined	R/W	Erasure Mode Related Setting Error Detect Returns the check result of whether the signal input to the FWE pin is high and whether the error protection state is not entered. When a low-level signal is input to the FWE pin or the error protection state is entered, 1 is written to this bit. The input level to the FWE pin and the error protection state can be confirmed with the FWE bit (bit 7) and the FLER bit (bit 4) in FCCS, respectively. For conditions to enter the error protection state, see section 19.6.3, Error Protection. 0: FWE and FLER settings are normal (FWE = 1, FLER = 0) 1: FWE = 0 or FLER = 1, and erasure cannot be performed

(1) Selection of user boot MAT programming

In response to the command for selecting programming of the user boot MAT, the boot program transfers the corresponding flash-writing program, i.e. the program for writing to the user boot MAT.

Command	H'42

— Command H'42 (1 byte): Selects programming of the user boot MAT.

Response	H'06

— Response H'06 (1 byte): Response to selection of user boot MAT programming
This ACK code is returned after transfer of the program that performs writing to the user boot MAT.

Error response	H'C2	ERROR

— Error response H'C2 (1 byte): Error response to selection of user boot MAT programming
— ERROR (1 byte): Error code
H'54: Error in selection processing (processing was not completed because of a transfer error)

(2) Selection of user MAT programming

In response to the command for selecting programming of the user MAT, the boot program transfers the corresponding flash-writing program, i.e. the program for writing to the user MAT.

Command	H'43

— Command H'43 (1 byte): Selects programming of the user MAT.

Response	H'06

— Response H'06 (1 byte): Response to selection of user MAT programming
This ACK code is returned after transfer of the program that performs writing to the user MAT.

- Inquiry on boot program state

In response to the command for inquiry on the state of the boot program, the boot program returns an indicator of its current state and error information. This inquiry can be made in the inquiry-and-selection state or the programming/erasure state.

Command	H'4F

— Command H'4F (1 byte): Inquiry on boot program state

Response	H'5F	Size	STATUS	ERROR	SUM

— Response H'5F (1 byte): Response to the inquiry regarding boot-program state

— Size (1 byte): The number of characters in STATUS and ERROR (fixed at 2)

— STATUS (1 byte): State of the standard boot program
See table 19.15, Status Codes.

— ERROR (1 byte): Error state (indicates whether the program is in normal operation or an error has occurred)
ERROR = 0: Normal
ERROR ≠ 0: Error
See table 19.16, Error Codes.

— SUM (1 byte): Checksum

Table 19.15 Status Codes

Code	Description
H'11	Waiting for device selection
H'12	Waiting for clock-mode selection
H'13	Waiting for bit-rate selection
H'1F	Waiting for transition to programming/erasure status (bit-rate selection complete)
H'31	Erasing the user MAT or user boot MAT
H'3F	Waiting for programming/erasure selection (erasure complete)
H'4F	Waiting to receive data for programming (programming complete)
H'5F	Waiting for erasure block specification (erasure complete)

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

22.3.2 Standby Control Register 2 (STBCR2)

STBCR2 is an 8-bit readable/writable register that controls the operation of modules in power-down mode.

Bit:	7	6	5	4	3	2	1	0
	MSTP7	MSTP6	-	MSTP4*	-	-	-	-
Initial value:	0	0	1	1	1	0	0	0
R/W:	R/W	R/W	R	R/W	R	R	R	R

Note: * The function is available only in the F-ZTAT version. In the masked ROM version, this bit is used as a reserved bit.

Bit	Bit Name	Initial Value	R/W	Description
7	MSTP7	0	R/W	Module Stop Bit 7 When this bit is set to 1, the supply of the clock to the RAM is halted. 0: RAM operates 1: Clock supply to RAM halted
6	MSTP6	0	R/W	Module Stop Bit 6 When this bit is set to 1, the supply of the clock to the ROM is halted. 0: ROM operates 1: Clock supply to ROM halted
5	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

24.3.7 Watchdog Timer (WDT) Timing

Table 24.11 Watchdog Timer (WDT) Timing

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V,
T_a = –20°C to +85°C (consumer applications),
T_a = –40°C to +85°C (industrial applications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	50	ns	Figure 24.20

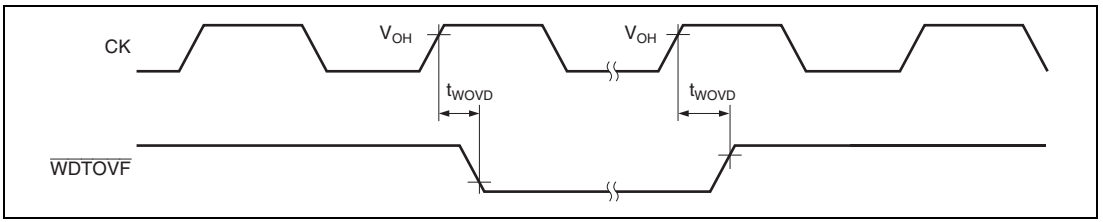


Figure 24.20 WDT Timing

D. Product Code Lineup

Table D.1 Product Code Lineup

Product Name	Product Type: Classification	ROM Capacity	RAM Capacity	Application	Operating temperature	Product Code	Package (Package Code)
SH7146	F-ZTAT version	256 kbytes	8 kbytes	Consumer application	−20 to +85°C	R5F71464AN80FPV	LQFP1414-80 (FP-80WV)
				Industrial application	−40 to +85°C	R5F71464AD80FPV	
	Masked ROM version	256 kbytes	8 kbytes	Consumer application	−20 to +85°C	R5M71464BNXXXFPV *2	
				Industrial application	−40 to +85°C	R5M71464BDXXXFPV *2	
	F-ZTAT version supporting full functions of E10A*1	256 kbytes	8 kbytes	For system development only*1	0 to +50°C	R5E71464RN80FPV	
SH7149	F-ZTAT version	256 kbytes	8 kbytes	Consumer application	−20 to +85°C	R5F71494AN80FPV	LQFP1414-100 (FP-100UV)
				Industrial application	−40 to +85°C	R5F71494AD80FPV	
	Masked ROM version	256 kbytes	8 kbytes	Consumer application	−20 to +85°C	R5M71494BNXXXFPV *2	LQFP1414-100 (FP-100UV)
				Industrial application	−40 to +85°C	R5M71494BDXXXFPV *2	
	F-ZTAT version supporting full functions of E10A*1	256 kbytes	8 kbytes	For system development only*1	0 to +50°C	R5E71494RN80FPV	LQFP1414-100 (FP-100UV)

Notes: 1. These products are only used for system development by the customer, and E10A internal bus trace function and AUD function are available. However, normal F-ZTAT version or masked ROM version must be used in mass production.

In normal F-ZTAT version, the E10A internal bus trace function and AUD function are not available.

Reliability is not guaranteed for F-ZTAT version supporting full functions of E10A.

2. XXX is the ROM code.

Item	Page	Revision (See Manual for Details)
24.5 Flash Memory Characteristics Table 24.17 Flash Memory Characteristics	934	Table amended

Item	Symbol		Min.	Typ.	Max.	Unit
Programming time*1*2*4	t_P		—	1	20	ms/128 bytes
Erase time*1*2*4	t_E		—	40	260	ms/4-Kbyte block
			—	300	1500	ms/32-Kbyte block
			—	600	3000	ms/64-Kbyte block
Programming time (total)*1*2*4	Σt_P		—	2.3	12	s/256 Kbytes
Erase time (total)*1*2*4	Σt_E		—	2.3	12	s/256 Kbytes
Programming and erase time (total)*1*2*4	Σt_{PE}		—	4.6	24	s/256 Kbytes
Reprogramming count	N_{WEC}		500*3	—	—	Times

Appendix B. Processing of Unused Pins	943	Newly added
D. Product Code Lineup Table D.1 Product Code Lineup	946	Table amended

Product Type							
Product Name	Classification	ROM Capacity	RAM Capacity	Application	Operating temperature	Product Code	Package (Package Code)
SH7146	F-ZTAT version	256 kbytes	8 kbytes	Consumer application	–20 to +85°C	R5F71464AN80FPV	LQFP1414-80 (FP-80WV)
				Industrial application	–40 to +85°C	R5F71464AD80FPV	
	Masked ROM version	256 kbytes	8 kbytes	Consumer application	–20 to +85°C	R5M71464BNXXXFPV *2	
				Industrial application	–40 to +85°C	R5M71464BDXXXFPV *2	
	F-ZTAT version supporting full functions of E10A*1	256 kbytes	8 kbytes	For system development only*1	0 to +50°C	R5E71464RN80FPV	
SH7149	F-ZTAT version	256 kbytes	8 kbytes	Consumer application	–20 to +85°C	R5F71494AN80FPV	LQFP1414-100 (FP-100UV)
				Industrial application	–40 to +85°C	R5F71494AD80FPV	
	Masked ROM version	256 kbytes	8 kbytes	onsumer application	–20 to +85°C	R5M71494BNXXXFPV *2	LQFP1414-100 (FP-100UV)
				Industrial application	–40 to +85°C	R5M71494BDXXXFPV *2	
	F-ZTAT version supporting full functions of E10A*1	256 kbytes	8 kbytes	For system development only*1	0 to +50°C	R5E71494RN80FPV	LQFP1414-100 (FP-100UV)

E. Package Dimensions Figure E.1 FP-80WV Figure E.2 FP-100UV	947, 948	Figures replaced
Figure E.3 FP-100AV	—	Figure deleted