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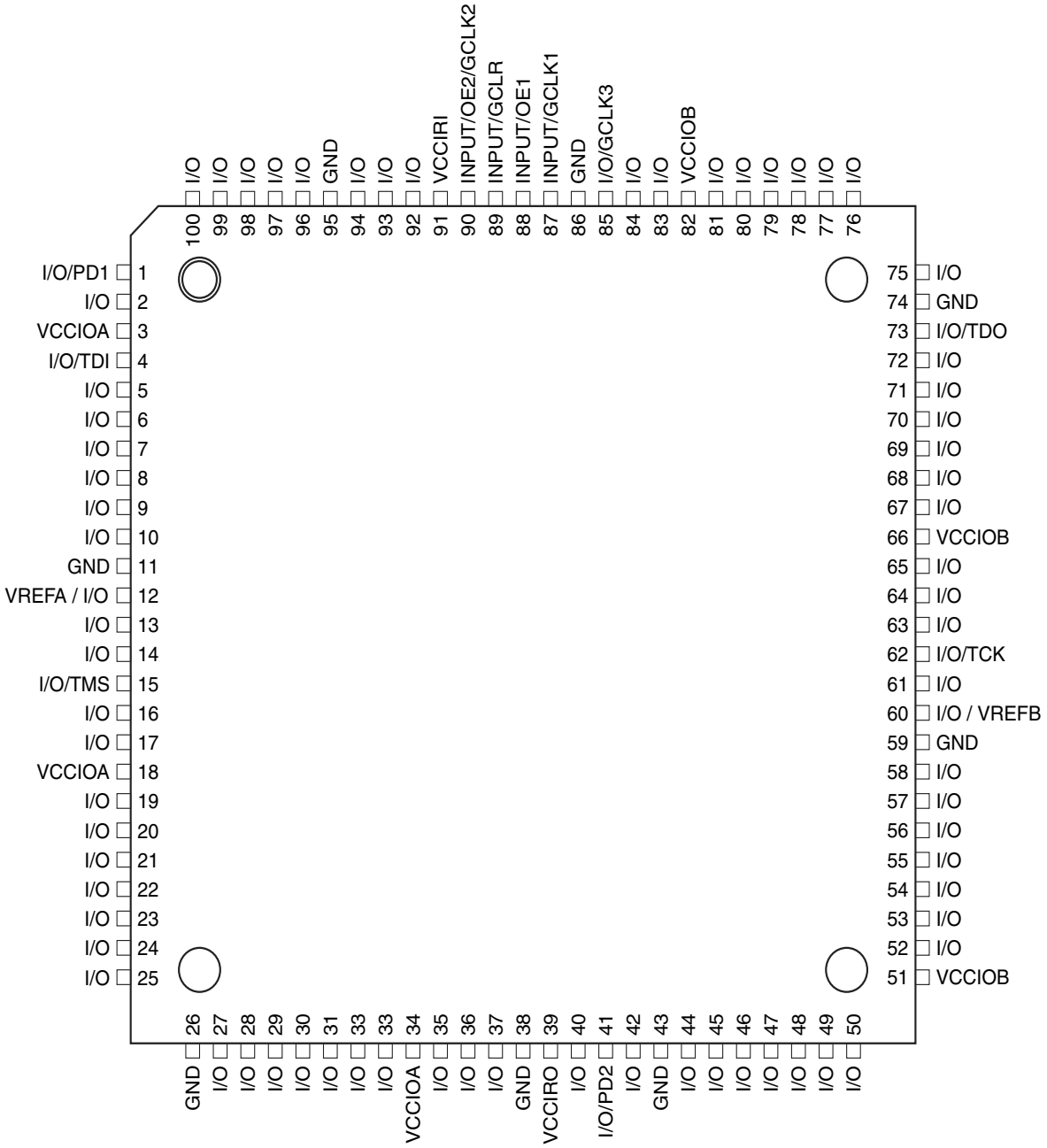
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	80
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1508re-5ax100

Figure 1-1. 100-lead TQFP Top View



Note: VCCIRO (P39 for 100 TQFP) needs to be left floating and used for coupling (use 2.2 µF/or 4.7 µF X7R chip CAP and 470 pF NPO chip CAP.

1.1 Product Terms and Select Mux

Each ATF1508RE macrocell has five product terms. Each product term receives as its inputs all signals from the switch matrix and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX configuration is determined by the design compiler, which selects the optimum macrocell configuration.

1.2 OR/XOR/CASCADE Logic

The ATF1508RE's logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with minimal additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high or low level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms.

1.3 Flip-flop

The ATF1508RE's flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software). In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be any one of the Global CLK signals (GCK[0 : 2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

1.4 Extra Feedback

The ATF1508RE macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

1.5 I/O Control

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or bi-directional pin. The output enable for each macrocell can be selected from the true or complement of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input or bi-directional pin.

1.6 Global Bus/Switch Matrix

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 128 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

1.7 Foldback Bus

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to all 16 macrocells within the logic block. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each logic block allow generation of high fan-in sum terms or other complex logic functions with little additional delay.

2. Input and I/O Pins

2.1 Programmable Pin-keeper Option for Inputs and I/Os

The ATF1508RE offers the option of individually programming each of its input or I/O pin so that pin-keeper circuit can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents undriven input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Figure 2-1 shows the pin-keeper circuit for an Input Pin and Figure 2-2 shows the same for an I/O pin. The pin-keeper circuit is a weak feedback latch and has an effective resistance that is approximately 50 kΩ

Figure 2-1. Input with Programmable Pin-keeper

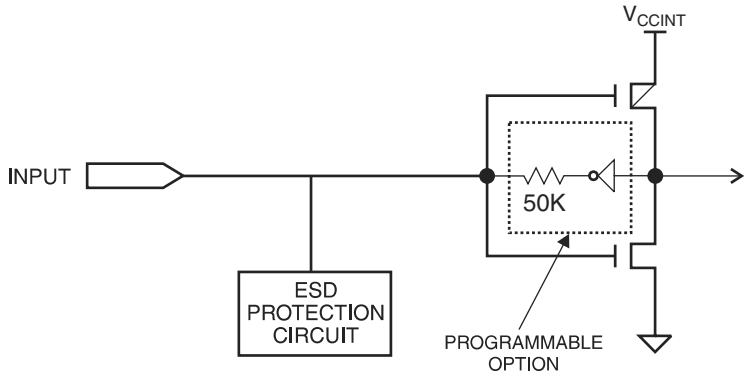
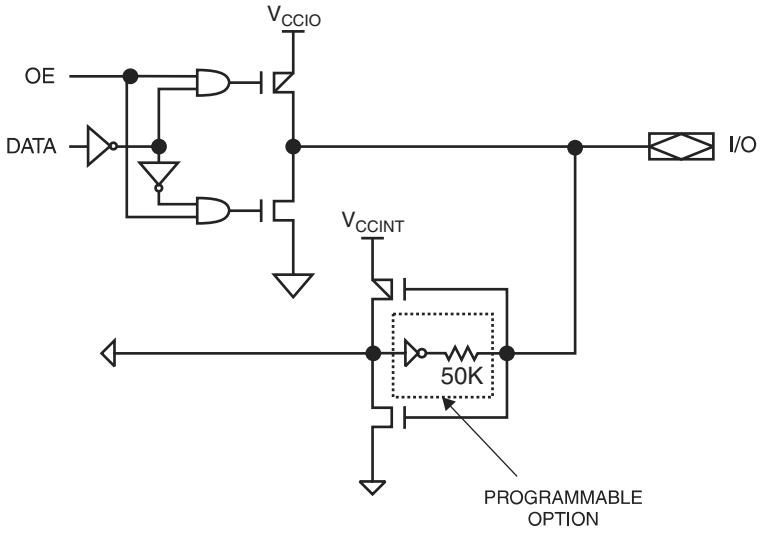


Figure 2-2. I/O with Programmable Pin-keeper



2.2 Schmitt Trigger

The Input Buffer of each input and I/O pin has an optional schmitt trigger setting. The schmitt trigger option can be used to buffer inputs with slow rise times.

2.3 Output Drive Capability

Each output has a high/low drive option. The low drive option (slow slew rate) can be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed or drive strength. Outputs default to high drive strength by Atmel software and can be set to low drive strength through the slew rate option.

2.4 I/O Bank

The I/O pins of the ATF1508RE are grouped into two banks, Bank A and Bank B. Bank A comprises of I/O pins for macrocells 1 to 64 (Logic Block A, B, C, and D), and it is powered by V_{CCIOA}. Bank B comprises of I/O pins for macrocells 65 to 128 (Logic Block E, F, G, and H), and it is powered by V_{CCIOB}.

2.5 I/O Standard

The ATF1508RE supports a wide range of I/O standards which include LVTTL, LVCMOS33, LVCMOS25, LVCMOS18 and LVCMOS15. The I/O pins of the ATF1508RE can also be individually configured to support SSTL-2 (Class I) and SSTL-3 (Class I) advanced I/O standards.

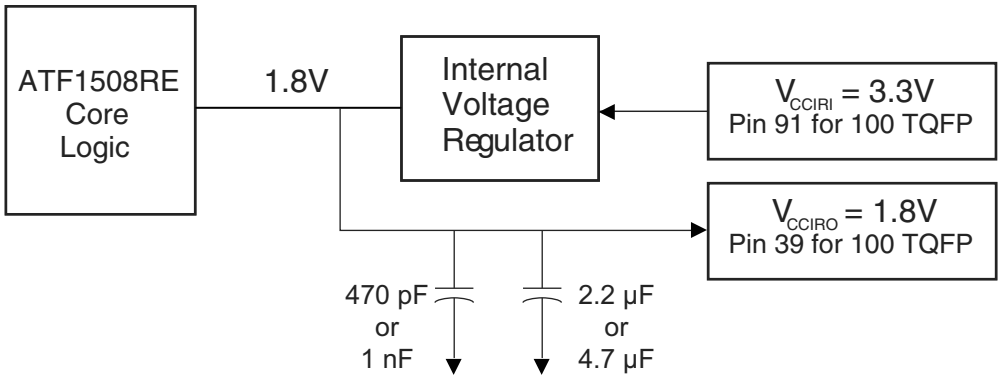
This and the two I/O banks, together, allow the ATF1508RE to be used for voltage level translation.

2.6 On-Chip Voltage Regulator

The ATF1508RE CPLD device has a built-in Internal Voltage Regulator that converts an external 3.3V supply to internal 1.8V core supply. The 1.8V output of the internal voltage regulator is also connected to the VCCIRO pin (Pin 39 for 100-pin TQFP) so that external bypass capacitors can be used to minimize noise. The recommended bypass capacitor values for the VCCIRO pin are 2.2 µF or 4.7 µF X7R, and 470 pF or 1 nF NPO type. These capacitors will help filter out noise at the output of the internal voltage regulator, which is important for the ATF1508RE to operate properly (see Figure 2-3).

The ATF1508RE CPLD also supports MultiVolt I/O interface feature, which allows seamless interface to other devices at 1.5V, 1.8V, 2.5V, or 3.3V logic levels. The ATF1508RE device has two I/O banks, each bank can be supplied with an independent VCCIO (VCCIOA or VCCIOB).

Figure 2-3. On-Chip Voltage Regulator



3. Power Management

Unlike conventional CPLDs with sense amplifiers, the ATF1508RE is designed using low-power full CMOS design techniques. This enables the ATF1508RE to achieve extremely low power consumption over the full operating frequency spectrum.

The ATF1508RE also has an optional power-down mode. In this mode, current drops to below 100 µA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins.

4. Security Feature

A fuse is provided to prevent unauthorized copying of the ATF1508RE fuse patterns. Once enabled, fuse reading or verification is inhibited. However, the 16-bit User Electronic Signature remains accessible. To reset this feature, the entire memory array in the device must be erased.

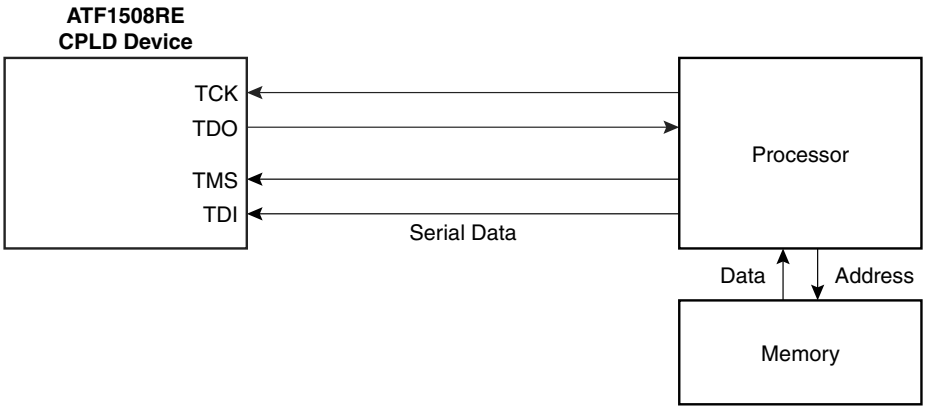
5.2 On-the-Fly Reconfiguration – OTF

In this mode, the CPLD design pattern stored in the internal configuration memory can be modified while the previously-programmed design pattern is operating with minimal disturbance to the programming operation of the new design. The new configuration will take affect after the OTF programming process is completed and the OTF mode is exited.

The configuration data for any design is stored in the internal configuration memory. Once the configuration data is transferred to the internal static registers of the CPLD, the CPLD operates with the design pattern and the configuration memory is free to be re-loaded with a new set of configuration data. The design pattern due to the new configuration content is activated through an initialization cycle that occurs on exiting the OTF mode or after the next power up sequence.

Figure 5-2 shows the electrical interface for configuration of the ATF1508RE device in the OTF mode. The processor is the controlling device that communicates with the CPLD and uses configuration data stored in the external memory to configure the CPLD.

Figure 5-2. Configuration of ATF1508RE Device Using a Processor and Memory



5.3 Direct Reconfiguration Access – DRA

This reconfiguration mode allows the user to directly modify the internal static registers of the CPLD without affecting the configuration data stored in the embedded memory. It is more useful in cases where immediate and temporary context change in the function of the hardware is desired.

The embedded configuration memory in the ATF1508RE does not change when a new set of configuration data is passed to the ATF1508RE using the DRA mode. Instead, the internal static registers of the CPLD are directly written with the data entering the device via the JTAG port. In other words, it's a temporary change in the function performed by the CPLD since a power sequence results in the device being configured again by the data stored in the embedded memory.

5.4 ISP Programming Protection

The ATF1508RE has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The I/O pins default to high-Z state during such a condition.

All ATF1508RE devices are initially shipped in the erased state, thereby making them ready to use for ISP.

6. JTAG-BST/ISP Overview

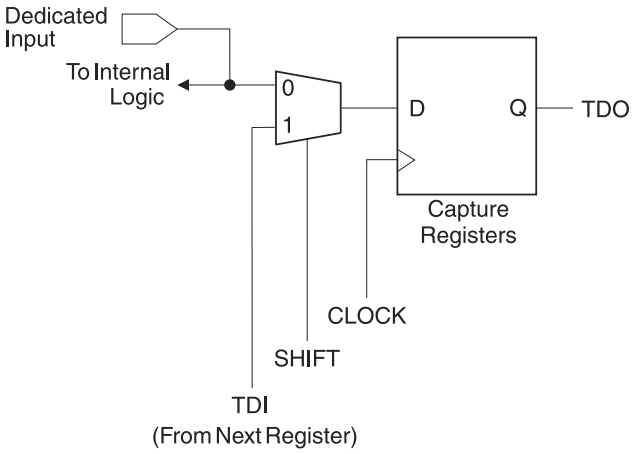
The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1508RE. The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing methods. Each input pin and I/O pin has its own boundary-scan cell (BSC) to support boundary-scan testing. The TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1508RE's BSC can be fully described using a BSDL file as described in IEEE 1149.1 standard. This allows ATF1508RE testing to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1508RE also has the option of using the four JTAG-standard I/O pins for ISP. The ATF1508RE is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE 1532 standard using 1.8V/2.5V/3.3V LVCMOS level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

6.1 JTAG Boundary-scan Cell (BSC) Testing

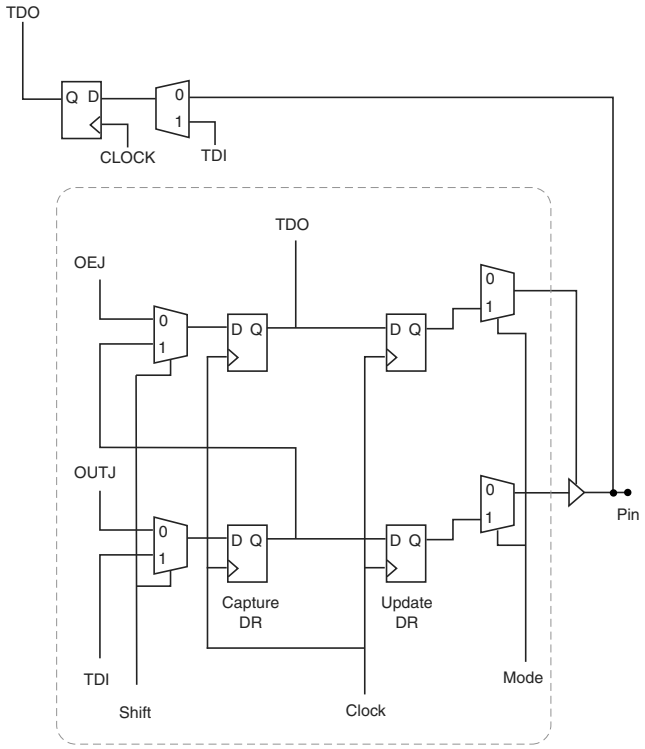
The ATF1508RE contains 80 I/O pins and four dedicated input pins. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE 1532 standard. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells is shown below.

Figure 6-1. BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)



Note: The ATF1508RE has a pull-up option on TMS and TDI pins. This feature is selected as a design option.

Figure 6-2. BSC Configuration for Macrocell



7. Design Software Support

ATF1508RE designs are supported by several third-party tools. Automated fitters allow logic synthesis using a variety of high-level description languages such as VHDL® and Verilog®. Third party synthesis and simulation tools from Mentor Graphics® are integrated into Atmel's software tools.

8. Electrical Specifications

Table 8-1. Absolute Maximum Ratings*

Operating Temperature	–40° C to +85° C
Storage Temperature	–65° C to +150° C
Supply Voltage (V_{CCINT})	–0.5V to +2.5V
Supply Voltage for Output Drivers (V_{CCIO})	–0.5V to +4.5V
Junction Temperature	–55° C to +155° C

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8-4. DC Characteristics

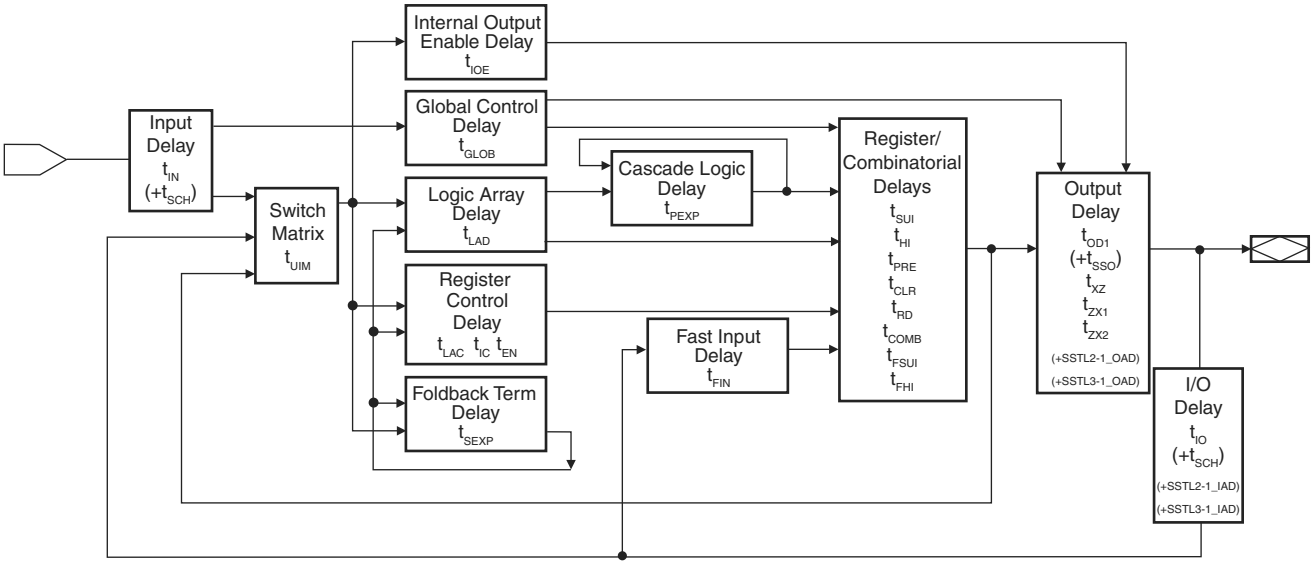
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCIRI}	Supply Voltage for internal logic and input buffers		3.0	3.3	3.6	V
V_{CCIO}	Supply Voltage for output drivers at 3.3V		3.0	3.3	3.6	V
V_{CCIO}	Supply Voltage for output drivers at 2.5V		2.3	2.5	2.7	V
V_{CCIO}	Supply Voltage for output drivers at 1.8V		1.7	1.8	1.9	V
V_{CCIO}	Supply Voltage for Output Drivers at 1.5V		1.4	1.5	1.6	V
I_{SB_IO}	Standby Current, VCCIO	V_{CCIO} = 3.3V, V_{CCIRI} = 3.3V		1		µA
I_{SB_INT}	Standby Current, V_{CC} Core(1)	V_{CCIRI} = 3.3V, V_{CCIO} = 3.3V		130		µA
$I_{CC\_INT(HD)}$	Operating Current(1) for V_{CCIRI} (supply voltage)	V_{CCIRI} = 3.3V, V_{CCIO} = 3.3V, f = 1 MHz		450		µA
$I_{CC\_IO(HD)}$	Operating Current(1) for V_{CCIO} (supply voltage for output drivers), per LAB	V_{CCIRI} = 3.3V, V_{CCIO} = 3.3V, f = 1 MHz		375		µA
$I_{CC\_INT(LD)}$	Operating Current(1) for V_{CCIRI} (low drive)	V_{CCIRI} = 3.3V, V_{CCIO} = 3.3V, f = 1 MHz		450		µA
$I_{CC\_IO(LD)}$	Operating Current(1) for V_{CCIO} (supply voltage for output drivers), per LAB	V_{CCIRI} = 3.3V, V_{CCIO} = 3.3V, f = 1 MHz		150		µA
I_{IL}, I_{IH}	Input Leakage	V_{CCIRI} = 3.3V, V_{IN} = 0V or 1.9V			±1	µA
I_{OZH}, I_{OH}	Output or IO Leakage	V_{CCIRI} = 3.3V, V_{CCIRO} = 3.6V, V_{IN} = 0V or V_{CCIRO}			±1	µA
LVCMOS 3.3V & LVTTL (HD: High Drive, LD: Low Drive)						
V_{IL}	Input Low-voltage		-0.3		0.8	V
V_{IH}	Input High-voltage		2		3.9	V
V_{OL}	Output Low-voltage	HD: I_{OL} = 8 mA, V_{CCIO} = 3V			0.4	V
		LD: I_{OL} = 1 mA, V_{CCIO} = 3V			0.4	V
V_{OH}	Output High-voltage	HD: I_{OH} = -8 mA, V_{CCIO} = 3V	V_{CCIO} - 0.4V			V
		LD: I_{OH} = -1 mA, V_{CCIO} = 3V	V_{CCIO} - 0.4V			V
LVCMOS 2.5V						
V_{IL}	Input Low-voltage		-0.3		0.7	V
V_{IH}	Input High-voltage		1.7		3.9	V
V_{OL}	Output Low-voltage	HD: I_{OL} = 8 mA, V_{CCIO} = 2.3V			0.4	V
		LD: I_{OL} = 1 mA, V_{CCIO} = 2.3V			0.4	V
V_{OH}	Output High-voltage	HD: I_{OH} = -8 mA, V_{CCIO} = 2.3V	V_{CCIO} - 0.4V			V
		LD: I_{OH} = -1 mA, V_{CCIO} = 2.3V	V_{CCIO} - 0.4V			V

Table 8-7. SSTL3-1 DC Voltage Specifications

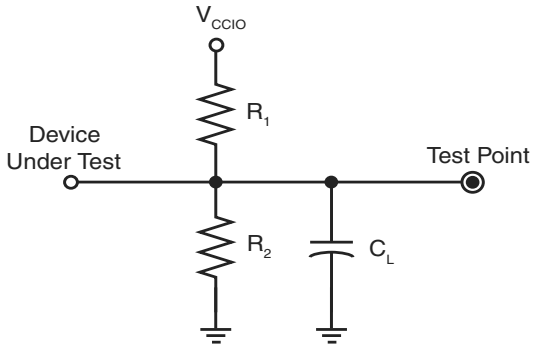
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCIO}	Input Source Voltage		3.0	3.3	3.6	V
V_{REF}(1)	Input Reference Voltage		1.3	1.5	1.7	V
V_{TT}(2)	Termination Voltage		V_{REF} - 0.05	1.5	V_{REF} + 0.05	V
V_{IH}	Input High Voltage		V_{REF} + 0.4		V_{CCIO} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		V_{REF} - 0.6	V
V_{OH}	Output High Voltage	I_{OH} = -8 mA, V_{CCIO} = 3V	V_{CCIO} - 1.1			V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V			0.7	V
$V_{IH(DC)}$	Input High Voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Input Low Voltage		-0.3		V_{REF} - 0.18	V

Notes: 1. Peak-to-peak noise on V_{REF} may not exceed ±2% V_{REF}, V_{REF} should track the variations in V_{CCIO}.
2. V_{TT} of transmitting device must track V_{REF} of receiving devices.

9. Timing Model



10. Output AC Test Loads



	R1	R2	CL
LVTTL	350 Ohm	350 Ohm	35 pF
LVCMOS33	300 Ohm	300 Ohm	35 pF
LVCMOS25	200 Ohm	200 Ohm	35 pF
LVCMOS18	150 Ohm	150 Ohm	35 pF

Note: C_L includes test fixtures and probe capacitance.

11. AC Characteristics

Table 11-1. AC Characteristics [1]

Symbol	Parameter		-5 Min	-5 Max	-7 Min	-7 Max	Units
t_{PD1_INP}	Delay for Single Input to Non-registered Output			5.0		6	ns
t_{PD1}	Input or Feedback to Non-registered Output			7		7.5	ns
t_{PD2}	Input or Feedback to Non-registered Feedback			4.2		4.7	ns
t_{SU}	Global Clock Setup Time		2.2		2.8		ns
t_{H}	Global Clock Hold Time		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input		1		2		ns
t_{FH}	Global Clock Hold Time of Fast Input		0.5		0.75		ns
t_{COP}	Global Clock to Output Delay			6		6.9	ns
t_{CH}	Global Clock High Time		1.25		2		ns
t_{CL}	Global Clock Low Time		1.25		2		ns
t_{ASU}	Array Clock Setup Time		1.7		2.2		ns
t_{AH}	Array Clock Hold Time		0.50		0.60		ns
t_{ACOP}	Array Clock to Output Delay			6.5		7.5	ns
t_{ACH}	Array Clock High Time		1.75		2.5		ns
t_{ACL}	Array Clock Low Time		1.75		2.5		ns
t_{CNT}	Minimum Global Clock Period			3		4.75	ns
f_{CNT}	Maximum Internal Global Clock Frequency		333		210		MHz
t_{ACNT}	Minimum Array Clock Period			4		5.5	ns
f_{ACNT}	Maximum Internal Array Clock Frequency		250		181		MHz
$f_{MAX\_EXT\_SYNC}$	Maximum External Frequency	V_{CCIO} = 3.3V		122		103	MHz
$f_{MAX\_EXT\_ASYNC}$	Maximum External Frequency	V_{CCIO} = 3.3V		122		103	MHz
t_{IN}	Input Pad and Buffer Delay		0.7			0.9	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.7			0.9	ns
t_{FIN}	Fast Input Delay			1		1	ns
t_{SEXP}	Foldback Term Delay			2		3	ns
t_{PEXP}	Cascade Logic Delay			0.5		1.0	ns
t_{LAD}	Logic Array Delay			1.8		1.8	ns
t_{LAC}	Logic Control Delay			1.5		2	ns
t_{IOE}	Internal Output Enable Delay			2		2	ns
t_{OD1}	Output Buffer Delay (HD) (High Drive; C_L = 35 pF)	V_{CCIO} = 1.5V V_{CCIO} = 1.8V V_{CCIO} = 2.5V V_{CCIO} = 3.3V		4.5 4.0 3.5 2.8		4.5 4.0 3.5 2.8	ns

Table 13-2. ATF1508RE I/O Pinouts

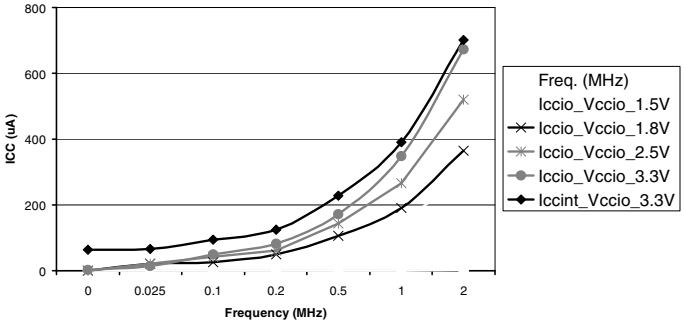
MC	Logic Block	100-lead TQFP	132-ball CBGA	MC	Logic Block	100-lead TQFP	132-ball CBGA
1	A	2	G1	33	C	25	B1
2	A	-	-	34	C	-	-
3	A/ **PD1**	1	F1	35	C	24	B2
4	A	-	-	36	C	-	-
5	A	100	F2	37	C	23	A1
6	A	99	F3	38	C	22	B4
7	A	-	-	39	C	-	-
8	A	98	E1	40	C	21	A4
9	A	97	E2	41	C	20	C5
10	A	-	-	42	C	-	-
11	A	96	E3	43	C	19	B5
12	A	-	-	44	C	-	-
13	A	94	D1	45	C	17	A5
14	A	93	D2	46	C	16	C6
15	A	-	-	47	C	-	-
16	A	92	C1	48	C/ **TMS**	15	N10
17	B	14	C2	49	D	37	P2
18	B	-	-	50	D	-	-
19	B	13	G3	51	D	36	M3
20	B	-	-	52	D	-	-
21	B/**VREFA**	12	H1	53	D	35	N3
22	B	10	H2	54	D	33	P3
23	B	-	-	55	D	-	-
24	B	9	H3	56	D	32	M4
25	B	8	J1	57	D	31	M5
26	B	-	-	58	D	-	-
27	B	7	J2	59	D	30	N5
28	B	-	-	60	D	-	-
29	B	6	K1	61	D	29	P5
30	B	5	K3	62	D	28	M6
31	B	-	-	63	D	-	-
32	B/ **TDI**	4	M9	64	D	27	N6

Table 13-2. ATF1508RE I/O Pinouts (Continued)

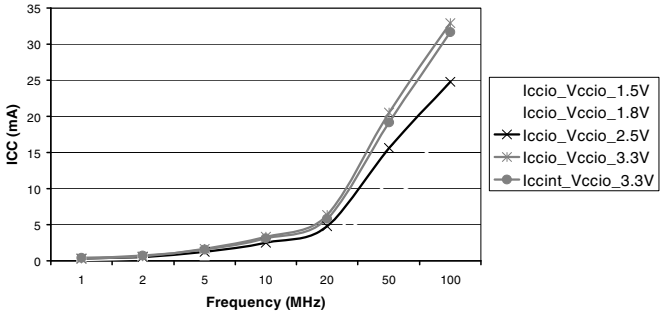
MC	Logic Block	100-lead TQFP	132-ball CBGA	MC	Logic Block	100-lead TQFP	132-ball CBGA
65	E	40	G13	97	G	63	C12
66	E	-	-	98	G	-	-
67	E/ **PD2**	41	G12	99	G	64	B12
68	E	-	-	100	G	-	-
69	E	42	F14	101	G	65	A12
70	E	44	F13	102	G	67	C11
71	E	-	-	103	G	-	-
72	E	45	F12	104	G	68	B11
73	E	46	E13	105	G	69	A11
74	E	-	-	106	G	-	-
75	E	47	E12	107	G	70	C10
76	E	-	-	108	G	-	-
77	E	48	D14	109	G	71	A10
78	E	49	D13	110	G	72	C9
79	E	-	-	111	G	-	-
80	E	50	D12	112	G/ **TDO**	73	B9
81	F	52	H12	113	H	75	N14
82	F	-	-	114	H	-	-
83	F	53	H13	115	H	76	N13
84	F	-	-	116	H	-	-
85	F	54	J13	117	H	77	P14
86	F	55	J12	118	H	78	P12
87	F	-	-	119	H	-	-
88	F	56	K14	120	H	79	M11
89	F	57	K13	121	H	80	N11
90	F	-	-	122	H	-	-
91	F	58	L14	123	H	81	P11
92	F	-	-	124	H	-	-
93	F/**VREFB**	60	L13	125	H	83	P10
94	F	61	L12	126	H	84	P9
95	F	-	-	127	H	-	-
96	F/ **TCK**	62	M10	128	H/ **GCLK3**	85	M8

14. Typical DC and AC Characteristic Graphs

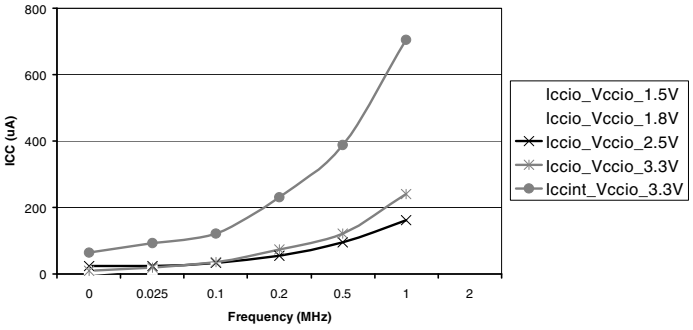
ICC INT & ICC I/O (HD) @
VCCIRI = 3.3V Over Frequency, Room Temp



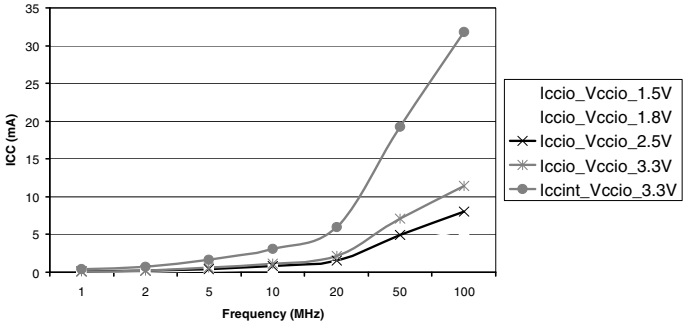
ICC INT & ICC I/O (HD) @
VCCIRI = 3.3V Over Frequency, Room Temp



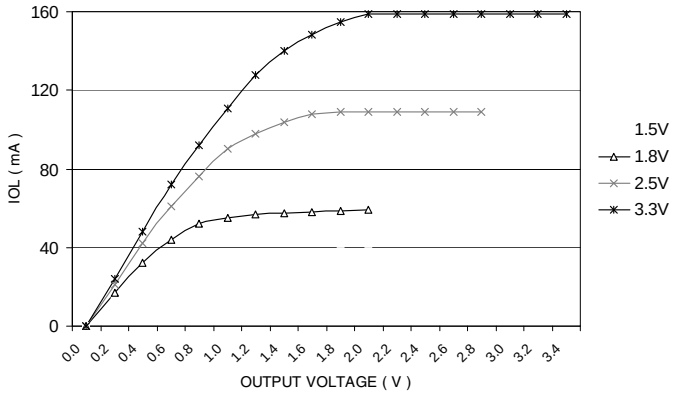
ICC INT & ICC I/O (LD) @
VCCIRI = 3.3V Over Frequency, Room Temp



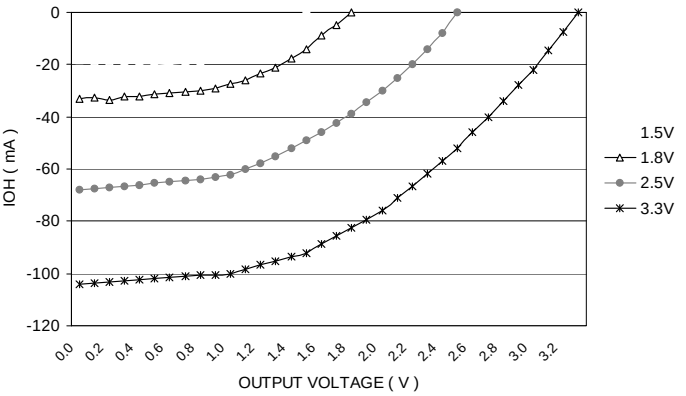
ICC INT & ICC I/O (LD) @
VCCIRI = 3.3V Over Frequency, Room Temp



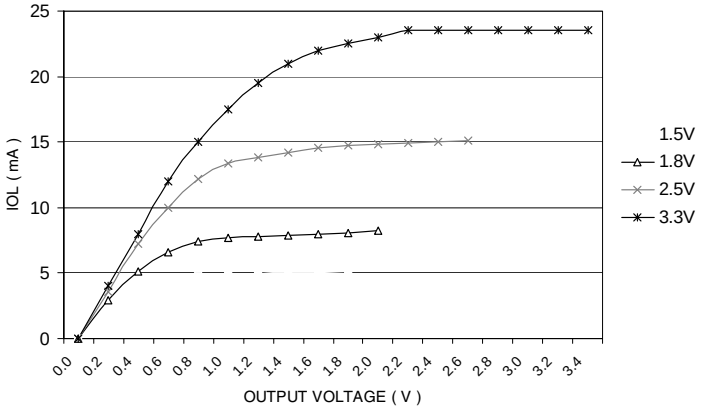
OUTPUT SINK CURRENT(IOL) VS. OUTPUT VOLTAGE
(VCCIRI = 3.3V, VCCIO = 1.5-3.3V, TA = 25C), High Drive



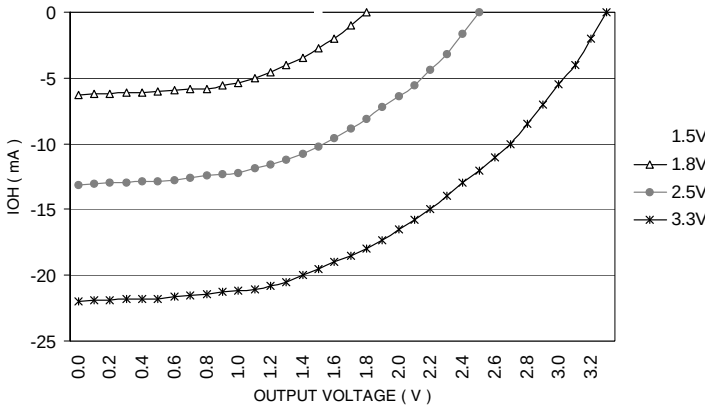
OUTPUT SOURCE CURRENT(IOH) VS. OUTPUT VOLTAGE
(VCCIRI = 1.8V, VCCIO = 1.5-3.3V, TA = 25C), High Drive



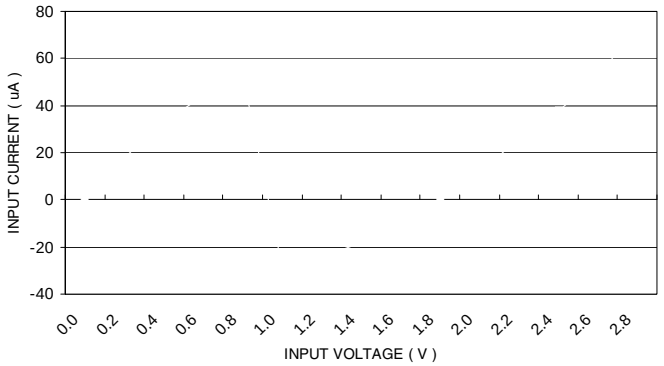
OUTPUT SINK CURRENT(IOL) VS. OUTPUT VOLTAGE
(VCCIRI = 1.8V, VCCIO = 1.5-3.3V, TA = 25C), Low Drive



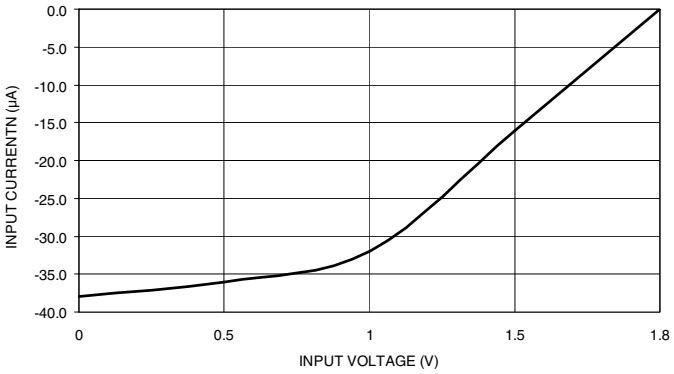
OUTPUT SOURCE CURRENT(IOH) VS. OUTPUT VOLTAGE
(VCCIRI = 1.8V, VCCIO =1.5-3.3V, TA = 25C), Low Drive



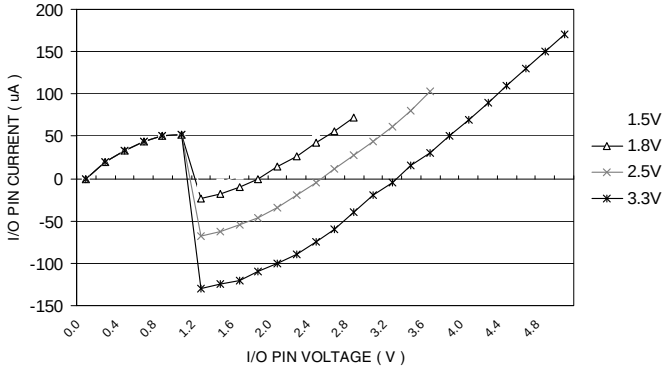
INPUT CURRENT VS. INPUT VOLTAGE
INPUT PIN (VCCIRI = 3.3V, TA = 25C)
(PIN-KEEPER ON)



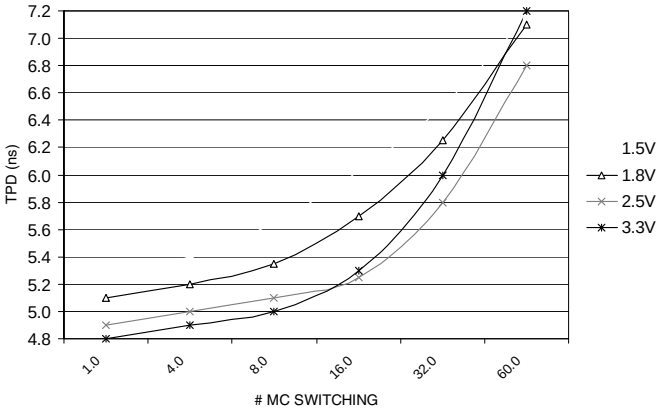
INPUT & I/O CURRENT VS. INPUT VOLTAGE
VCCIRI = 3.3V, VCCIO = 1.8V (TA = 25°C)
(Pull-Up On)



I/O PIN CURRENT VS. I/O PIN VOLTAGE
I/O PIN (VCCIRI = 3.3V, VCCIO = 1.5V-3.3V, TA = 25C)
(PIN KEEPER ON)



TPD VS. # MC SWITCHING
(VCCIRI = 3.3V, VCCIO = 1.5-3.3V, TA = 25C)



15. Ordering Information

15.1 Lead-free Package Options (RoHS Compliant)

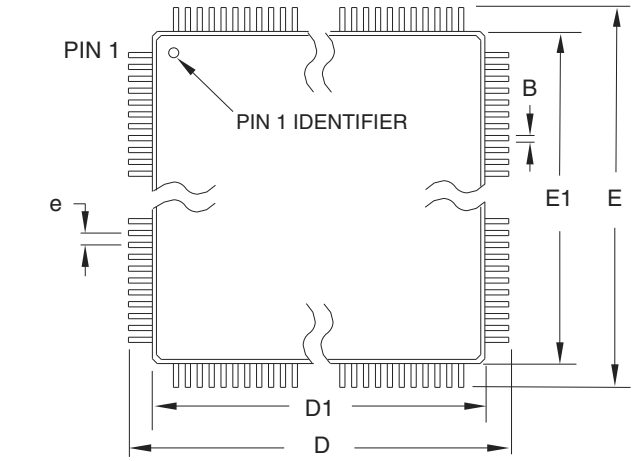
t_{PD} (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
5	6	ATF1508RE-5AX100	100A	Commercial (0° C to +70° C)
7	6.5	ATF1508RE-7AU100	100A	Industrial (-40° C to +85° C)
5	6	ATF1508RE-5CX132	132C1	Commercial (0° C to +70° C)
7	6.5	ATF1508RE-7CU132	132C1	Industrial (-40° C to +85° C)

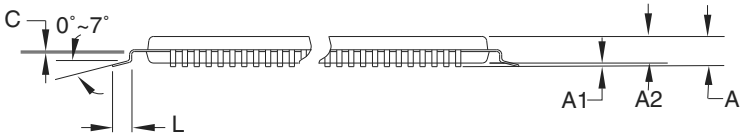
Note: For shaded devices, contact marketing for availability.

Package Type	
100A	100-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
132C1	132-ball, Plastic Chip-Size Ball Grid Array Package (CBGA)

16. Packaging Information

16.1 100A – TQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	C

17. Revision History

Revision Level – Release Date	History
A – October 2008	Initial release

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
pld@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature