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###VcY°B dgZ°
; ZVij gZh

- Adl "edl Zg'deZgM'đc`YZh^c
 Á &#"K'hj eean'kdaV\Z'hZZ' WwZ'†
 Á 8deeZg'ciZgXdccZXi'gZyj XZh'edl ZgXdchj b ei'dc
 Á B j á'K dá'°B`\$D'hj eedg'[dg&#"K!" # "K!VcY'(#"K'ciZgVXZh
 Á : H7h'd[[Zgc`egd\gMb b WwZ'edl Zg'hVc`c`b dYZ
 ■ ; aZmWwZ'adX`b VcV\Zb Zci`X'gYj '†gn'††' j e'íd'[dj ge] VhZ"adX ZY`
 addeh'EAAH
 Á 7j 'š"°c`adl "h' Zl `XadX`i'gZZ
 Á J e'íd'Z^]i`adVWaXadX`h^cVh
 Á 8adX AdX`†B`[ZVij gZ'gZyj X'c`XadX`YZa/n`VcY`h' Zl
 Á 8adX 7ddh'†B`[ZVij gZ'egdk`Y`c`XadX`b j á'eaXMI'đc`VcY`
 Y`k`h'đc
 Á 8adX Hj`†j'†B`[ZVij gZ'egdk`Y`c`egd\gMb b WwZ'adX`e] VhZ`VcY`
 YZa/n'h]`†j`c`
 ■ Edl Zgjj a`\$D`[ZVij gZh
 Á 8db eaVci'††' eZg'e] ZgVaXdb edcZci`ciZgXdccZXi`heZXVa`
 c`iZg'h'°c`gdj e`†E8>H>††' **PCI Local Bus Specification,
 Revision 2.2** [dg('#"K'đeZgM'đc`V'((`dg++B = oVcY'(`dg+) W'h
 Á Hj eedg'[dg] ^] "heZZY ZniZgcVab Zb dgZH'°cXj Y`c`°99G`
 mcX] gdcj hYncVb`X'G6B`†H9G6B†VcY`07I`hiVi`X'G6B`
 †H'G6B†
 Á &+`°cej i`VcY`&+`dj iej i`AK9H'X] VccZah
 Á 9`gZi`XdccZXi`đc`[gdb`°\$D`e`ch'íd'adXVa`ciZgXdccZXi`egdk`Y`c`
 [Vh'i`8D`VcY`i`Hj`i`b`Zh[dgXdb eaZm'ad`X
 Á B j á'K dá'°\$D`h' eedg'[dg&#"K!" # "K!VcY'(#"K'ciZgVXZh
 Á Egd\gMb b WwZ`Xa/b e'íd'K`88>D
 Á c`Y`k`Yj Vaig`h'ViZ`dj iej i`ZcWwZ`Xdcigda[dgZVX]`e`c
 Á Egd\gMb b WwZ`dj iej i`h'Zl`"gViZ`Xdcigda'đ'gZyj XZ'h`†X]`c`
 cd'hZ
 Á Hj eedg'[dgVYkVcXZY`\$D`h'VcYVgY'h'°cXj Y`c`adl`"kdaV\Z`
 Y`[[ZgZci`Vah^cVa`c`†AK9H!†AKE: 8A!E8>M'6<E!8I!†
 HH A"(VcY`HH A""!°<I Až!VcY`= HI A`8a/hh>
 Á Hj eedg'h'] di`hdX`Zi`c`deZgM'đc
 Á Ej aej e`dc`°\$D`e`ch`WZ[dgZ`VcY`Yj g`c`Xdc[^j gM'đc

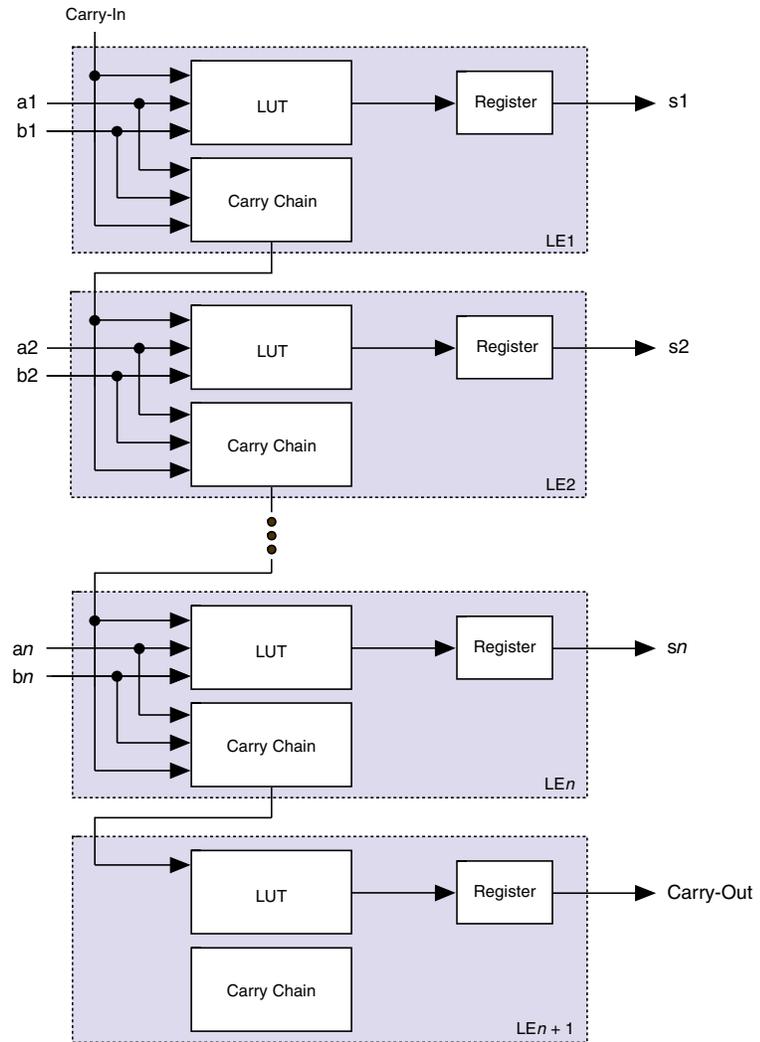
I WwZ'° #6E: M'°@8'Hj eean'KdaV\Zh	
	KdaV\Z
; ZVij gZ	
Internal supply voltage (V _{CCINT})	1.8 V
MultiVolt I/O interface voltage levels (V _{CCIO})	1.8 V, 2.5 V, 3.3 V, 5.0 V (1)

Note:
 †† 6E: M'°@8`Yzk`XZh`Xvc`WZ`*`#%K`†dažg'vci`W'h]`h`c`Vc`ZniZgc`Važh'h'đg#

- 6YkVcXZY`ciZgXdccZXi`hig`Xij`gZ
 - Á 8deeZg`ciZgXdccZXi`[dg]`^]`eZgfdgb`VcXZ
 - Á ;dj`g`aZkZa]`ZgVgX]`XVa;`Vhi`gVX`i`ciZgXdccZXi`hig`Xij`gZ`
egdk`Y`c`\"[Vhi`e`gZY`X`WVZ`ciZgXdccZXi`YZa/nh
 - Á 9ZY`XViZY`XVgn`X]`V`c`i]`Vi`b`eazb`ZcihVg1]`b`Zi`Xtj`cXi`dchhj`Xj`
Vh[Vhi`WY`Zgh`Xdj`ciZgh`VcY`Xdb`eVgM`dgh`Vj]`idb`Vi`XVan]`hZY`Vh`
hd[i]`VgZ`iddah`VcY`b`Z`Vlj`cXi`dch
 - Á 9ZY`XViZY`XVhXVYZ`X]`V`c`i]`Vi`b`eazb`Zcih]`^]`"heZZY!"
]`^]`"[Vc`c`ad`Xtj`cXi`dch`Vj]`idb`Vi`XVan]`hZY`Vh`hd[i]`VgZ`iddah`
VcY`b`Z`Vlj`cXi`dch
 - Á >ciZgZV`kZY`adXVa`ciZgXdccZXi`Vaadl`h`dcZ`A: `id`Yg`kZ`"`. `di]`Zg`
A: `hi]`gdj`\"i]`Z`[Vhi`adXVa`ciZgXdccZXi`
- 6YkVcXZY`hd[i]`VgZ`hj`eedg
 - Á Hd[i]`VgZ`YZh`^c`hj`eedg`VcY`Vj`idb`Vi`X`ea/XZ`VcY`"gdj`iZ`
egdk`Y`ZY`Vh`i]`Z`6`aZgV`F`j`Vgj`H`B`>Y`ZkZadeb`Zci`hnh`Zb`[dg`
L`c`Ydi`h`W`hZY`E8h`Hj`c`HE`6`G8h`Vi`dch`VcY`= `E`.`%%`%
HZg`Zh`,`%\$`-`%&l`dg`hi`Vi`dch
 - Á 6`aZgV`B`Z`V8`dgZ`i`j]`cXi`dch`VcY`6`aZgV`B`Z`Vlj]`cXi`dc`E`VgjcZgh`
Egd`gVb`E6`B`EE`H`b`Z`Vlj]`cXi`dch`dei`b`bZY`[dg`6`E: `M`%@`8`
VgX]`fZXj`gZ`V`kV`aWZ
 - Á C`Vi`kZA`c`^`B`ciZ`gM`dc`l`f]`edej`d`ghnci]`Zh`h`h`b`j`dM`dc!`
VcY`i`b`c`\"VcVanh`h`iddah
 - Á F`j`Vgj`h`>`H`^c`Vd`Ve`i`Zb`WZY`ZY`ad`X`VcVanoZgh`b`ea`[Zh`
c`hnh`Zb`YZh`^c`ZkVj`Vi`dc`Vh`\"k`c`\"VXX`Zh`id`ciZgc`VacdY`Zh`
Yj`g`c`\"YZk`XZ`deZgM`dc
 - Á Hj`eedg`h`edej`d`g`gZk`h`dc`"Xdcigda`hd[i]`VgZ`eVX`V`Zh`c`Xj`Y`c`\"
EK`8H`G8H`VcY`H88H`"

I WZ`(#6E: M`%@8`F; E`fi7<6`EVX`VZ`Dei`dch`fi`>D`8dj`ci`*****Notes (1), (2)					
9Zk`XZ	&)"E`c`i`F; E	'`%`"E`c`EF; E	(')`%E`c`EF; E	(*`+`"E`c`7<6	+*`"E`c`7<6
EP20K100C	92	151	183	246	
EP20K200C		136	168	271	376
EP20K400C					488
EP20K600C					488
EP20K1000C					488
EP20K1500C					488

; ^j g' + #6E: M % @8'8Vgn'8] V'c



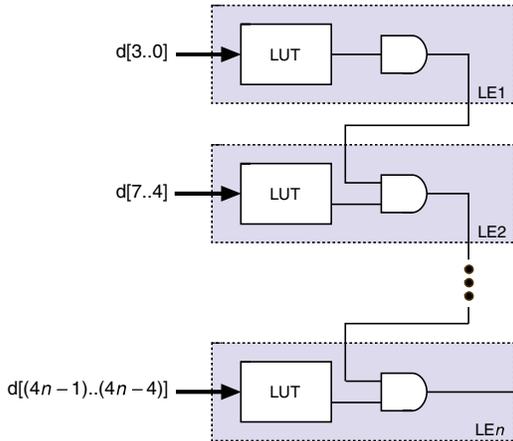
Cascade Chain

L 1] i] Z'XhWYZ'X] V'c!i] Z'6E: M' %@8 VgX] 1ZXj g'Xvc"b eazb Zci" [j cX'dch1 1] V'kZgn1 YZ'[Vc"c#6Y_VXZci'AJ I h'Xvc"Xdb ej iZ'edg'dch' d[V'lj cX'dc"eVgVaaZa] Z'XhWYZ'X] V'c h'ZgVaa'XdccZXi'i] Z' 'ciZgb ZY'ViZ'kVj Zh#] Z'XhWYZ'X] V'c Xvc'j h'Z'ad\ X'VaAND'dgad\ X'VaOR tk V'9Z'B dgVcA'c'kZgh'dci id'XdccZXi'i] Z'dj iej ih'd[VY_VXZci'A: h#: VX' WYY'1'dcVaA: 'egdk'YZh'dj gb dgZ'cej ih'di] Z'Z[[ZXi'kZ1 Yi] d[V' [j cX'dc!1 1] V'h] dg'XhWYZ'YZa'n#8VhWYZ'X] V'c'ad\ X'Xvc'W'XgZ'VIZY' Vj idb Vi X'Van'Wh'i] Z'F j Vgj h'>>8db e'azgYj g'e\ YZh'c'egdXZhh'e!\'dg' b Vcj Van'Wh'i] Z'YZh'cZgYj g'e\ YZh'c'Zcign#

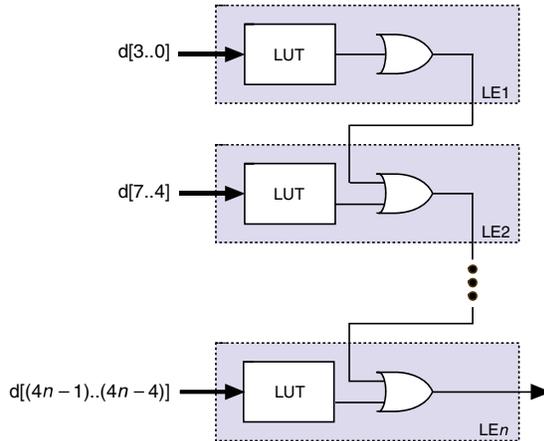
8VhWYZ'X] V'ch'adc\Zgi] Vc'izc'A: h'VgZ'b eazb ZciZY'Vj idb Vi X'Van'Wh' a'c' c'\A6 7h'id\Zi] Zg#, dgZc] VcXZY' [1i'c!\V'adc\ X'hWYZ'X] V'c h' 'eh' VaZgc'ViZ'A6 7h'c V'B Z\VA6 7'hig Xij gZ'#6 X'hWYZ'X] V'c'adc\Zgi] Vc'dcZ' A6 7h' 'ehZ1] Zg[gdb Vc ZkZc'cj b WZgZY'A6 7'id'i] Z'cZmi'ZkZc'cj b WZgZY' A6 7!dg[gdb Vc'dYY'cj b WZgZY'A6 7'id'i] Z'cZmi'dYY'cj b WZgZY'A6 7#, dg ZnVb eaz'i] Z'a'hi'A: d[i] Z'[gh'A6 7'c'i] Zj eeZg'aZ'i B Z\VA6 7'hig Xij gZ' X'Vgg'Zh'id'i] Z'[gh'A: d[i] Z'i] gh'A6 7'c'i] Z'B Z\VA6 7'hig Xij gZ', h] dl h] dl i] Z'XhWYZ'lj cX'dc'Xvc'XdccZXi'W_VXZci'A: hid'dgp [j cX'dch1 1] V'1 YZ'[Vc"c#

; ^j gZ', #6E: M' %@8'8VhWYZ'8] V'c

6C9'8VhWYZ'8] V'c



DG'8VhWYZ'8] V'c



Normal Mode

I] Z'cdgb Vab dYZ'hj 1WZ[dg\ZcZgVad\XVeeAXi'dch'Xdb WcVidgVa
 [j cX'dch'dgl YZYXdy'e\j cX'dch'i] Vi'Xvc'iv Z'WkVciVZ'd[V'
 XhXVYZ'X] V'c#>c'cdgb Vab dYZ!'[dj g'YVIV'cej ih'[gdb i] Z'A6 7'adXVa'
 ^ciZgXdccZX'VcY'i] Z'XVgn"e'VgZ'cej ih'idV'[dj g'cej i'AJ I #] Z'
 F j Vgj h>>8db e'ZgVj idb Vi'XVan'hZaZhi] Z'XVgn"e'dgi] Z'DATA3'hAcVa'
 Vh'dcZ'd[i] Z'cej ih'id'i] Z'AJ I #] Z'AJ I 'dj iej i'Xvc'WZ'Xdb WcZY1 4] i] Z'
 XhXVYZ"e'hAcVaid'[dgb V'XhXVYZ'X] V'c'i] gdi \] i] Z'XhXVYZ'dj i'hAcVaf
 A: h'c'cdgb Vab dYZ'hj eedg'eVX ZY'gZ'hZgh#

Arithmetic Mode

I] Z'Vgt] b Zi'Xb dYZ'h'YZVa[dg'b eazb Zci'e\WYZgh'VXj b j aIdgh'VcY'
 Xdb eVgMidg#6c'A: ^c'Vgt] b Zi'Xb dYZ] hZhi! d('cej i'AJ I #DcZ'AJ I '
 Xdb ej iZhVi] gZ"cej i'[j cX'dcQ] Z'di] Zg\ZcZgMiZh'XVgn'dj iej i#6h'
 h] dl c'c'; ^j gZ'-!i] Z'[ghi'AJ I j hZhi] Z'XVgn"e'hAcVaVcY'i! d'YVIV'
 ^cej ih'[gdb i] Z'A6 7'adXVa'ciZgXdccZX'id\ZcZgMiZ'V'Xdb WcVidgVadg'
 gZ'hZgZY dj iej i#, dgZnVb eaz!1] Zc'b eazb Zci'e\Vc'WYZg[i] 'hdj iej i'
 'hi] Z'hj b 'd[i] gZ'hAcVah/DATA1!DATA2!VcY'XVgn"e#] Z'hZXdY'AJ I '
 j hZhi] ZhVb Zi] gZ'hAcVahid\ZcZgMiZ'XVgn'dj i'hAcVai] ZgZVh'XgZVi'e\
 V'XVgn'X] V'c#] Z'Vgt] b Zi'Xb dYZ'Vad'hj eedgh'h'b j aVcZdj h'Z'd[i] Z'
 XhXVYZ'X] V'c#A: h'c'Vgt] b Zi'Xb dYZ'Xvc'YgkZ'dj i'gZ'hZgZY'VcY'
 j cgZ'hZgZY'kZgh'dch'd[i] Z'AJ I 'dj iej i#

I] ZF j Vgj h>>hd[i] VgZ'b eazb Zci'heVgVb ZiZg'oZY'j cX'dch'i] Vi j hZi] Z'
 Vgt] b Zi'Xb dYZ'Vj idb Vi'XVan'1] ZgZ'Veegdeg'ViZQ] Z'YZhAcZgYdZhicdi'
 cZZY'id'heZX[n] dl i] Z'XVgn'X] V'c'1 ^aVZ'j hZY#

Counter Mode

I] Z'Xdj ciZgb dYZ'd[[Zgh'XadX 'ZcWZ!'Xdj ciZgZcWZ!'hncX] gldcj h'
 j e\$Ydl c'Xdcigd'hncX] gldcj h'XaZVg'VcY'hncX] gldcj h'adVY'dei'dch#] Z'
 Xdj ciZgZcWZ'VcY'hncX] gldcj h'j e\$Ydl c'Xdcigd'hAcVhVgZ'\ZcZgMiZY'
 [gdb i] Z'YVIV'cej ih'd[i] Z'A6 7'adXVa'ciZgXdccZXi#] Z'hncX] gldcj h'XaZVg'
 VcY'hncX] gldcj h'adVY'dei'dch'VgZ'A6 7"! YZ'hAcVahi] Vi'V[[ZX'Vai'
 gZ'hZgh'c'i] Z'A6 7#8dchZfj Zcian!'[Vcn'd[i] Z'A: h'c'Vc'A6 7] hZ'i] Z'
 Xdj ciZgb dYZ'i] ZgA: h'c'i] Vi'A6 7'b j hi'WZ'j hZY'Vh'eVg'd[i] Z'hVb Z'
 Xdj ciZgdgVZ'j hZY'[dgV'Xdb WcVidgVa] cX'dc#] ZF j Vgj h>>hd[i] VgZ'
 Vj idb Vi'XVan'eaVXh'Vcn'gZ'hZgh'i] Vi'VgZ'cdi'j hZY'Wh'i] Z'Xdj ciZg'cid'
 di] ZgA6 7h#

I] ZXdj ciZgb dYZj hZhiI d("cej iAJ I h/dcZ\ZcZgMZhI] ZXdj ciZgYVIM!
 VcY'i] Z'di] Zg\ZcZgMZh'i] Z'[Vhi XVggN W#6 " "id"&b j a eazmgfegdk YZh
 hncX] gldcj h'adVY c\!VcY Vcdi] ZgAND\ViZ'egdk YZh'hncX] gldcj h'
 XaZVg'e\#>[i] Z'XVhXVYZ'j cXi 'dc'hj hZY VhVc'A: 'c'Xdj ciZgb dYZ'i] Z'
 hncX] gldcj h'XaZVgdg'adVY'dkZggYZhVcn'h\cVaXVggZY'dc'i] Z'XVhXVYZ'
 X] V'c#I] Z'hncX] gldcj h'XaZVgdg'adVY'dkZggYZh'i] Z'hncX] gldcj h'adVY#A: h'c'
 Vg†] b Zi Xb dYZXVc YgkZ'dj i gZ\ 'hiZgZY VcYj c gZ\ 'hiZgZY kZgh'dchd[i] Z'
 AJ I 'dj iej i#

Clear & Preset Logic Control

Ad\ X'[dgi] Z'gZ\ 'hiZgZY XaZVgVcY'egZhi h\cVh'h'XdcigdaZY Vh'A6 7"l 'YZ'
 h\cVh#I] Z'A: 'Y'gZi an'hj eedg'hVc VhncX] gldcj h'XaZVg[j cXi 'dc#I] Z'
 F j Vgj h>>8db e'azgXVc'j hZV'not" \ViZ'ej h] "WX iZX] c'fj Z'idZb j aMIZ'
 Vc VhncX] gldcj h'egZhi'dg'idZb j aMIZ'h'b j aVcZdj h'egZhi VcY XaZVgdg'
 VhncX] gldcj h'adVY#=# dl ZkZg'i] 'hiZX] c'fj Zj hZhi] gZ'VY†'dcVaA: h'
 eZggZ\ 'hiZg#6 aZb j aM'dc'h'eZg'dgb ZY Vj idb Vi XVan1] Zc'i] ZYZhAc'h'
 Xdb e'azY#GZ\ 'hiZg'i] Vi Zb j aMIZ'h'b j aVcZdj h'egZhi VcY adVY† 'aZciZg'
 Vc'j c' cdl c'hiViZj edc'edl Zg'j e'dgi] Zc'i] Z'X] 'e"l 'YZ'gZhi'hVhZgZY#

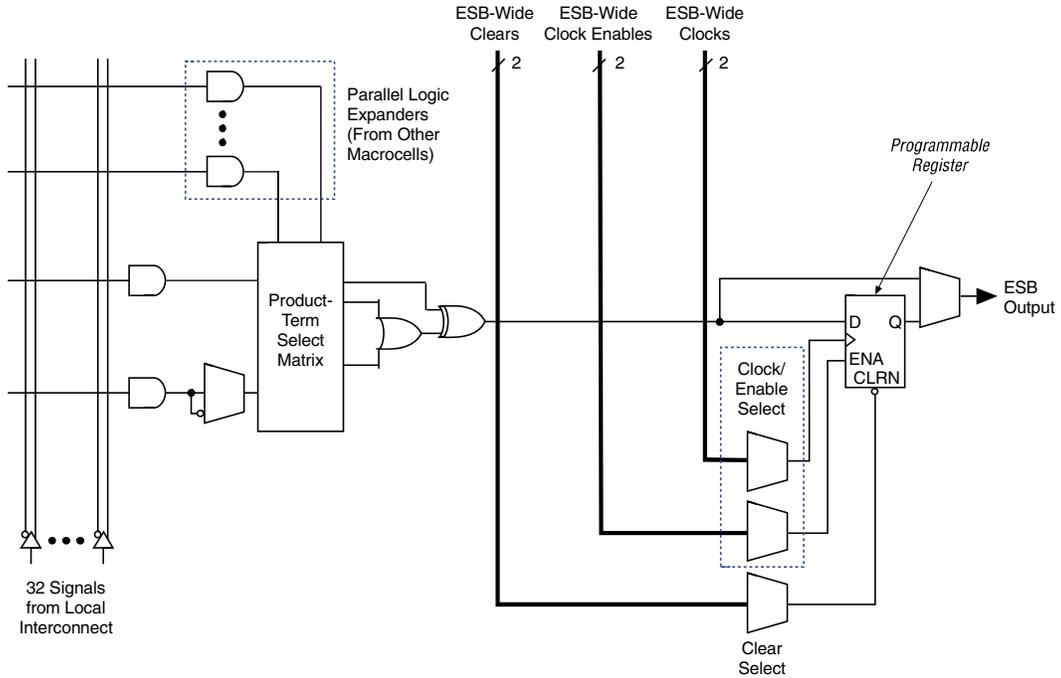
∞ VY†'dc'id'i] Z'il d'XaZVgVcY'egZhi'b dYZh'6 E: M' %@8 YZk XZh'
 egdk YZV'X] 'e"l 'YZ'gZhi'e'c' bDEV CLRn†i] Vi gZhihVagZ\ 'hiZg'i'c'i] Z'
 YZk XZ#J hZ'd[i] h'e'c'h'XdcigdaZY'i] gdl \] Vc'dei'dc'c'i] Z'F j Vgj h>>
 hd[i] VgZ'i] Vi'h'hzi VZ[dg'Xdb e'aM'dc#I] Z'X] 'e"l 'YZ'gZhi'dkZggYZhVaa'
 di] Zg'Xdciglah\cVh#GZ\ 'hiZg'h'c\ Vc VhncX] gldcj h'egZhi VgZ'egZhi'
 I] Zc'i] Z'X] 'e"l 'YZ'gZhi'hVhZgZYQ] hZ[[ZXi gZj ah[gdb i] Z'ckZgh'dc'
 iZX] c'fj Zj hZY'id'b eazb Zci'i] Z'VhncX] gldcj h'egZhi#

; VhiI gVX °ciZgXdccZXI

∞ i] Z'6 E: M' %@8 VgX] †ZXj gZ'XdccZXI'dchVZil ZZc'A: h': H7h'VcY'>SD'
 e'chVgZ'egdk YZY Vh'i] Z'; VhiI gVX °ciZgXdccZXI#I] Z'; VhiI gVX °
 'ciZgXdccZXI'hVhZgZhd[Xdci'cj dj h] dg'odciVaVcY kZg'XVagdj i'c\'
 X] VccZhi] Vi'igVkZghZ'i] Z'YZk XZ#I] h'adVWagdj i'c\ 'hi g' Xj gZ'egdk YZh'
 egZY X'WwZ'eZg'dgb VcXZ!ZkZc'c'Xdb eazmY Zh\ch#∞ Xdcig/h'i!i] Z'
 hZ\ b ZciZY'gdj i'c\ 'c'; E < 6 h'gZfj 'gZhi'† X] 'b Vi g'XZhi'd'XdccZXI V'
 kVgVwZ'cj b VZgd[gdj i'c\ 'eVi] h'c'XgZVh'c\ i] Z'YZaVnhVZil ZZc'ad\ X'
 gZhdj gZhVcY'gZj X'c\ 'eZg'dgb VcXZ#

I] Z'; VhiI gVX °ciZgXdccZXI'Xdch'h'hid[gd] VcY'Xdj b c'ciZgXdccZXI'
 X] VccZhi] Vi'heVc'i] Z'Zci'gZ'YZk XZ#I] Z'gd] °ciZgXdccZXI'gdj iZh'h\cVh'
 i] gdj \] dj iVgd] 'd[B Z\VA6 7 hi g' Xj gZhd] Z'Xdj b c'ciZgXdccZXI'gdj iZh'
 h\cVh'i] gdj \] dj iVXdj b c'd[B Z\VA6 7 hi g' Xj gZhd]] Zc'j h'c\ i] Z'gd] °
 VcY'Xdj b c'ciZgXdccZXI!Vc'A: !>D: !>dg: H7 XVc YgkZVcn'di] ZgA: !>D: !>
 dg: H7 'c' VYZk XZ#HZZ'; ^j gZ'. #

; ^j g^&) #6E: M %@8^B VxgdXZaa



; dg^gZ\ ^hi ZgZY ^j cXl ^dc h^ZVX] ^b VxgdXZaaigZ\ ^hi Zg^XVc ^VZ ^egd\ gVb b ZY ^cY ^k ^Yj Van ^id ^b eaZb Zci ^9! ^! ^?@! ^dg^HG ^de ZgMl ^dc ^l ^1] ^egd\ gVb b WwZ ^XadX ^Xdcigda#l] Z^gZ\ ^hi Zg^XVc ^VZ ^Vh^VhZy ^[dg^Xdb Wc^Vidg^Vade ZgMl ^dc# 9j g^c\ ^Yzh^c Zcign! ^i] Z^Yzh^c Zg^heZX (^Zhi) Z^Yzh^gZY ^gZ\ ^hi Zg^ine ZQl] Z^ F j Vgj h^>>hd[iil VgZ^i] Zc ^hZaZXi hi] Z^b dhi Z[[^X^Zci ^gZ\ ^hi Zg^de ZgMl ^dc ^[dg^ ZVX] ^gZ\ ^hi ZgZY ^j cXl ^dc ^id ^dei ^b ^oZ^gZhdj gXZ] i ^abVi ^dc#l] Z^F j Vgj h^>>hd[iil VgZ^dgdi] Zg^hnci] Zh^hi dda^XVc ^Vhd ^hZaZXi ^i] Z^b dhi Z[[^X^Zci ^gZ\ ^hi Zg^ de ZgMl ^dc ^Vj idb Vi ^XVan ^l] Zc ^hnci] Zh^b^c\ ^= 9AYzh^ch#

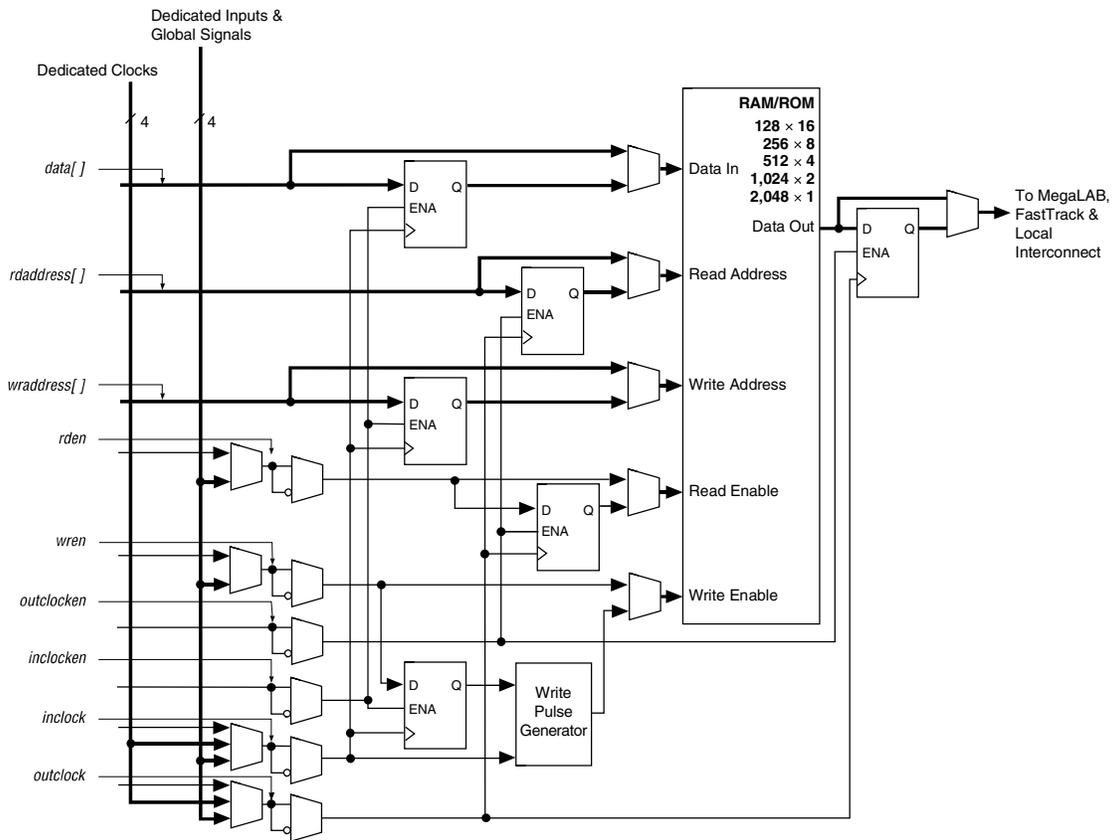
: VX] ^egd\ gVb b WwZ^gZ\ ^hi Zg^XVc ^VZ ^XadX ZY ^Vh^dcZ^d[iil d: H7^l ^YZ ^XadX h#l] Z: H7^l ^YZ ^XadX h^XVc ^VZ ^Zc ZgMl ZY [gdb ^Yzk ^XZYZY ^XlZY ^XadX ^e^ch! ^adVWah^cVh! ^dg^adXVa^ci ZgXdccZXi #: VX] ^XadX ^Vhd] Vh^Vc ^VhhdX^ViZY ^XadX ^ZcWwZ! ^ZcZgMl ZY [gdb ^i] Z^adXVa^ci ZgXdccZXi #l] Z^XadX ^VcY ^XadX ^ZcWwZ^h^cVhVgZ^gZa^iZY ^[dg^V^eVg ^Xj a/g: H7OVcn^b VxgdXZaa j h^c\ ^V^XadX ^Vhd^j hZhi] Z^VhhdX^ViZY ^XadX ^ZcWwZ#

>[^Wdi] ^i] Z^g^h^c\ ^VcY ^[Va^c\ ^ZY ^Zh^d[^V^XadX ^VgZ^j hZY ^c^Vc: H7^l ^Wdi] ^: H7^l ^YZ ^XadX ^h^cVhVgZ^j hZY#

RAM/ROM

The RAM/ROM block is a dual-port memory device that can be configured as either RAM or ROM. It is accessed via a data bus and address buses. The data bus is 16 bits wide, and the address buses are 8 bits wide. The RAM/ROM block is capable of storing up to 2,048 words of data. The RAM/ROM block is accessed via a data bus and address buses. The data bus is 16 bits wide, and the address buses are 8 bits wide. The RAM/ROM block is capable of storing up to 2,048 words of data.

Note (1)

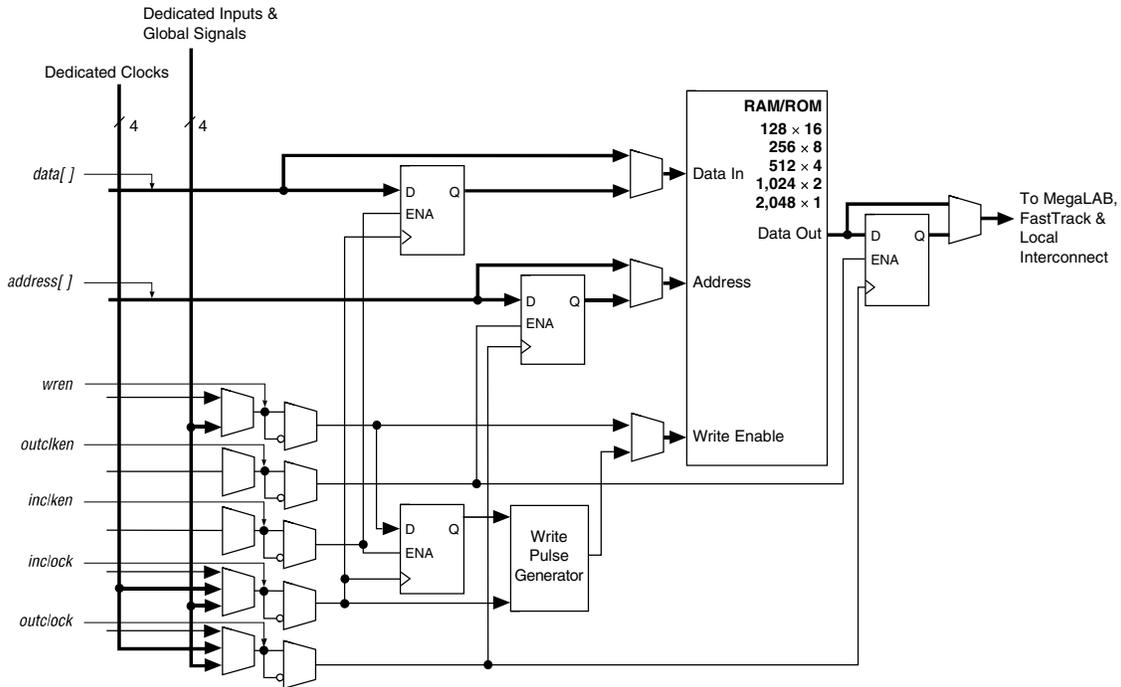


Note: The RAM/ROM block is accessed via a data bus and address buses. The data bus is 16 bits wide, and the address buses are 8 bits wide. The RAM/ROM block is capable of storing up to 2,048 words of data.

RAM/ROM

RAM/ROM: 128 x 16, 256 x 8, 512 x 4, 1,024 x 2, 2,048 x 1. Includes Data In, Address, Write Enable, and Data Out ports.

Note (1): H7... Note (1)



Note:

6 aigZ\ hi ZghXvc WZ VmcX] gdcjd han XaZVgY Vh: H7 adXVa ci ZgXdccZXi h\cVh\ adVWah\cVh\ dgi] ZX] e"l YZ'gZhi#

RAM/ROM

RAM/ROM: 128 x 16, 256 x 8, 512 x 4, 1,024 x 2, 2,048 x 1. Includes Data In, Address, Write Enable, and Data Out ports.

86 B hj hZY [dg] \ "heZZY hZVgX deZgi dch#L] Zc hZVgX c\ [dgYVIV l 1] c VG6B WdX !i] Z hZVgX hieZgdg ZY hZgVan#l] j h'cY'c\ V eVg Xj d/gYVIV dg Xvc iV Zb Vcn XnXaZ#86B hZVgX ZhVaaYYgZhZh'c eVgVaaZaVcY dj iej ih i] Z WYgZhhi dg c\ VeVg Xj d/gl dgY #L] Zc Vb ViX h' [dj cY! Vb ViX [d\ h' hzi] \] #; \j gZ" (h) dl hi] Z'86B WdX Y\ \gVb #

I W& #6E: M %@8`8adX `cej i`fi`Dj iej i`EVg/b ZiZg`EVg` d[" i`.....Note (1)							
Hhb Vda	EVg/b ZiZg	S`H`i`Vc`Y`V`g`	", `HeZZY`<g`V`Z`		"- `HeZZY`<g`V`Z`		J c`th
			B `c`	B Vm	B `c`	B Vm	
f _{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz
f _{IN}	Input clock frequency	3.3-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz

Notes to tables:

6 ad`cej i`XadX `heZX[`XMi`dch`b`j`h`i`VZ`b`Zi`#`]`Z`EAA`b`Vn`cdi`adX `dcid`Vc`c`Xdb` c`\\`XadX `f`i`]`Z`XadX `heZX[`XMi`dch` VgZ`cdi`b`Zi`!`XgZVi`c`\\`Vc`ZggdcZdj`h`XadX`1`1`]`c`i`]`ZYZk`XZ`#`
 E`f`]`Z`b`Vmb`j`b`adX`i`b`Z`h`)%`uh`idg`!`%%`cej`i`XadX`Xn`Xzh`1`]`X`Zk`ZgdXj`gh`[`gh`#`
 E`f` 7Z`[dgZ`Xdc`[`^`gM`dci`i`]`Z`EAA`X`g`j`1`h`VgZ`Y`h`W`V`c`Y`edl`ZgZ`Y`dl`c`#`9`j`g`c`\\`Xdc`[`^`gM`dci`i`]`Z`EAA`h`g`Zb`V`c` Y`h`W`V`Z`Y`#`]`Z`EAA`h`V`\\`c`id`adX`dc`XZ`i`]`ZYZk`XZ`h`c`i`]`Z`j`h`Zgb`dYZ`#`-`i`]`Z`XadX`Zc`W`V`Z`[`Z`Vij`gZ`h`j`h`ZY`!`adX`V`\\`ch` dc`XZ`i`]`Z`CLKLK`_`ENA`e`c`\\`d`Zh`]`^`]`c`j`h`Zgb`dYZ`#`
 E`f`]`]`Z`EAA`K`8D`de`ZgM`c`\\`g`V`c`Z`h`" `%%`B` =`o`≤` [k`8D` ≤`-`)`%`B` =`o`[dg`AK`9`Hb`dYZ`#`
 E`f` 8dci`VXi`6`a`ZgV`6`eea`XVi`dch`[dg`c`[dgb`Vi`d`c`dc`i`]`Zh`e`Vg/b`ZiZg`#`

H`^`c`V`d`V`e`
 :`b`V`Z`Y`Z`Y`
 Ad`\\`X`^`c`V`ano`Z`g`

6 E: M' %@8`YZk`XZ`h`c`Xj` YZ`YZk`XZ`Zc`]`Vc`XZb`Zci`h`d`h`j`eedg`i`]`Z`
 H`^`c`V`d`V`e`Z`b`V`Z`Y`Z`Y`ad`X`V`c`V`ano`Z`g`#`7`n`c`Xj`Y`c`\\`i`]`h`X`g`j`1`gn`i`]`Z`
 6 E: M' %@8`YZk`XZ`e`g`dk`Y`Z`h`i`]`Z`W`W`a`f`n`i`d`b`dc`1`dg`Y`Z`h`c`de`ZgM`d`c`dk`Zg`
 V`e`Zg`d`Y`d`[`i`b`Z`i`]`gdj`\\`]`i`]`Z`>` :` :`H`Y`#`&&` .`#`E`7`6`<`1`X`g`j`1`gn`O`V`Y`Z`h`c`Z`g`
 X`V`c`V`c`V`ano`Z`c`i`Z`g`c`V`aad`\\`X`Vi`he`ZZY`1`1`]`dj`i`V`g`c`\\`c`\\`c`i`Z`g`c`V`ah`c`V`h`i`d`i`]`Z`
 >`\$D`e`c`h`#`]`h`[Z`Vij`gZ`h`e`Vg`X`j`a`/`gn`b`edg`V`ci`[dg`W`Y`k`V`c`X`Z`Y`e`V`X`V`Z`h`
 h`j`X`]`V`h`;`c`Z`A`c`Z`7`<`6`e`V`X`V`Z`h`V`Z`X`j`h`Z`W`Y`c`\\`V`X`d`c`c`Z`X`i`d`c`id`V`e`c`
 Y`j`g`c`\\`i`]`Z`Y`Z`V`j`\\`c`\\`e`g`d`X`Z`h`X`V`c`V`Z`Y`[`[`X`j`a`V`[i`Z`g`V`W`d`V`g`Y`h`Y`Z`h`c`Z`Y`
 V`c`Y`b`V`c`j`[V`X`j`gZ`Y`#`

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20KC devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20KC devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc). Finally, APEX 20KC devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20KC devices support the JTAG instructions shown in Table 13.

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20KC device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

I WZ & #6E: M %@8 9Zk XZ GZXdb b ZcYZY DeZgMi c\ 8dcY1 dch					
Hnb Wda	EVg/b ZiZg	8dcY1 dch	B c	B Vm	J c1
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V _I	Input voltage	(2), (5)	-0.5	4.1	V
V _O	Output voltage		0	V _{CCIO}	V
T _J	Junction temperature	For commercial use	0	85	° C
		For industrial use	-40	100	° C
t _R	Input rise time (10% to 90%)			40	ns
t _F	Input fall time (90% to 10%)			40	ns

I WZ & #6E: M %@8 9Zk XZ 98 DeZgMi c\ 8dcY1 dch Notes (6), (7)						
Hnb Wda	EVg/b ZiZg	8dcY1 dch	B c	I ne	B Vm	J c1
I _I	Input pin leakage current (8)	V _I = 4.1 to -0.5 V	-10		10	μA
I _{OZ}	Tri-stated I/O pin leakage current (8)	V _O = 4.1 to -0.5 V	-10		10	μA
I _{CC0}	V _{CC} supply current (standby) (All ESBs in power-down mode)	V _I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V _I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R _{CONF}	Value of I/O pin pull-up resistor before and during configuration	V _{CCIO} = 3.0 V (9)	20		50	kΩ
		V _{CCIO} = 2.375 V (9)	30		80	kΩ
		V _{CCIO} = 1.71 V (9)	60		150	kΩ



9 8 DeZgMi c\ HeZX1 XM dchdc 6 E: M %@8 \$D hiVcYVg/hVgZ ahiZY c1 WZh" &id(+ #

I WZ (%#HHI A" `8a/hh">HeZX[XVi dch						
Hnb Wda	EVg/b ZiZg	8dcYf dch	B c'bj b	I ne XVa	B Vmb j b	J c fh
V _{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V _{TT}	Termination voltage		V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	V
V _{REF}	Reference voltage		1.15	1.25	1.35	V
V _{IH}	High-level input voltage		V _{REF} + 0.18		V _{CCIO} + 0.3	V
V _{IL}	Low-level input voltage		-0.3		V _{REF} - 0.18	V
V _{OH}	High-level output voltage	I _{OH} = -15.2 mA (1)	V _{TT} + 0.76			V
V _{OL}	Low-level output voltage	I _{OL} = 15.2 mA (2)			V _{TT} - 0.76	V

I WZ (&#HHI A" (`8a/hh">HeZX[XVi dch						
Hnb Wda	EVg/b ZiZg	8dcYf dch	B c'bj b	I ne XVa	B Vmb j b	J c fh
V _{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V _{TT}	Termination voltage		V _{REF} - 0.05	V _{REF}	V _{REF} + 0.05	V
V _{REF}	Reference voltage		1.3	1.5	1.7	V
V _{IH}	High-level input voltage		V _{REF} + 0.2		V _{CCIO} + 0.3	V
V _{IL}	Low-level input voltage		-0.3		V _{REF} - 0.2	V
V _{OH}	High-level output voltage	I _{OH} = -8 mA (1)	V _{TT} + 0.6			V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA (2)			V _{TT} - 0.6	V

I WzH) (i] gdl \] ; - h] dl i] Z [B 6M VcY ZmiZgcVai b c \ eVg/b ZiZg [dg
 : E8' % @ & % % ! : E8' % @ ' % % ! : E' % @) % % ! : E' % @ + % % ! : E' % @ & % % ! VcY
 : E' % @ * % % B YZk XZh#

I WzH) (#: E' % @ & % % [B 6M A: i b c \ eVg/b ZiZg *****Note (1)							
Hrb Wda	", HeZZY<gVZ		"- HeZZY<gVZ(2)		". HeZZY<gVZ(2)		Jc†
	B c	B Vm	B c	B Vm	B c	B Vm	
t _{SU}	0.3						ns
t _H	0.3						ns
t _{CO}		0.3					ns
t _{LUT}		0.7					ns

I WzH) (#: E' % @ & % % [B 6M i: H7i b c \ eVg/b ZiZg *****Note (1)							
Hrb Wda	", HeZZY<gVZ		"- HeZZY<gVZ(2)		". HeZZY<gVZ(2)		Jc†
	B c	B Vm	B c	B Vm	B c	B Vm	
t _{ESBARC}		1.4					ns
t _{ESBSRC}		2.5					ns
t _{ESBAWC}		3.1					ns
t _{ESBSWC}		3.0					ns
t _{ESBWASU}	0.5						ns
t _{ESBWAH}	0.5						ns
t _{ESBWDSU}	0.6						ns
t _{ESBWDH}	0.5						ns
t _{ESBRASU}	1.4						ns
t _{ESBRAH}	0.0						ns
t _{ESBWESU}	2.3						ns
t _{ESBDATASU}	0.0						ns
t _{ESBWADDRSU}	0.2						ns
t _{ESBRADDRSU}	0.2						ns
t _{ESBDATACO1}		1.0					ns
t _{ESBDATACO2}		2.3					ns
t _{ESBDD}		2.7					ns
t _{PD}		1.6					ns
t _{PTERMSU}	1.0						ns
t _{PTERMCO}		1.0					ns

I WZ** (#: E' %@ %B: B' b j b 'Ej aZ'L ^ij] ' b' c\`EVg/b ZiZgh*****Note (1)							
Hnb Wda	", "HeZZY"<gVYZ		"- "HeZZY"<gVYZ*(2)		". "HeZZY"<gVYZ*(2)		Jc†
	B' c	B Vm	B' c	B Vm	B' c	B Vm	
t _{CH}	2.2						ns
t _{CL}	2.3						ns
t _{CLRP}	0.2						ns
t _{PREP}	0.2						ns
t _{ESBCH}	2.3						ns
t _{ESBCL}	2.3						ns
t _{ESBWP}	1.1						ns
t _{ESBRP}	0.9						ns

I WZ** (#: E' %@ %B: niZg:Val' b' c\`EVg/b ZiZgh							
Hnb Wda	", "HeZZY"<gVYZ		"- "HeZZY"<gVYZ*(2)		". "HeZZY"<gVYZ*(2)		Jc†
	B' c	B Vm	B' c	B Vm	B' c	B Vm	
t _{INSU}	2.0						ns
t _{INH}	0.0						ns
t _{OUTCO}	2.0	5.0					ns
t _{INSUPLL}	3.3						ns
t _{INHPLL}	0.0						ns
t _{OUTCOPLL}	0.5	2.1					ns

I WZ** - #: E' %@) %B' B' b j b Ej aZ'L ^ij] 1' b' c\`EVg/b ZiZgh*****Note (1)							
Hnb Wda	", HeZZY`<gVYZ		"- HeZZY`<gVYZ` (2)		". HeZZY`<gVYZ` (2)		J c†
	B' c	B Vm	B' c	B Vm	B' c	B Vm	
t _{CH}	2.0						ns
t _{CL}	2.0						ns
t _{CLRP}	0.2						ns
t _{PREP}	0.2						ns
t _{ESBCH}	2.0						ns
t _{ESBCL}	2.0						ns
t _{ESBWP}	1.0						ns
t _{ESBRP}	0.8						ns

I WZ** . #: E' %@) %B: niZg:Val' b' c\`EVg/b ZiZgh							
Hnb Wda	", HeZZY`<gVYZ		"- HeZZY`<gVYZ` (2)		". HeZZY`<gVYZ` (2)		J c†
	B' c	B Vm	B' c	B Vm	B' c	B Vm	
t _{INSU}	2.1						ns
t _{INH}	0.0						ns
t _{OUTCO}	2.0	5.0					ns
t _{INSUPLL}	3.2						ns
t _{INHPLL}	0.0						ns
t _{OUTCOPLL}	0.5	2.1					ns

I WZ +&#: E' %@) %B: niZgcVá7Y^gXi ^dcVál 'b ^c\`EVg/b ZiZgh`							
Hnb Wda	", HeZZY<gVYZ		"- HeZZY<gVYZ(2)		". HeZZY<gVYZ(2)		J c†
	B ^c	B Vm	B ^c	B Vm	B ^c	B Vm	
t _{INSUBIDIR}	2.4						ns
t _{INHBIDIR}	0.0						ns
t _{OUTCOBIDIR}	2.0	5.0					ns
t _{XZBIDIR}		7.1					ns
t _{ZXBIDIR}		7.1					ns
t _{INSUBIDIRPLL}	3.8						ns
t _{INHBIDIRPLL}	0.0						ns
t _{OUTCOBIDIRPLL}	0.5	2.1					ns
t _{XZBIDIRPLL}		4.2					ns
t _{ZXBIDIRPLL}		4.2					ns

I WZ +&#: E' %@) %B: [B 6M]A: 'I 'b ^c\`EVg/b ZiZgh` ***** Note (1)							
Hnb Wda	", HeZZY<gVYZ		"- HeZZY<gVYZ(2)		". HeZZY<gVYZ(2)		J c†
	B ^c	B Vm	B ^c	B Vm	B ^c	B Vm	
t _{SU}	0.3						ns
t _H	0.3						ns
t _{CO}		0.3					ns
t _{LUT}		0.7					ns

I WZ, (#: E' %&%%B: niZg:Vā7Y'gZi'dcVāi 'b ċ\`EVg/b ZiZg'							
Hnb Wda	", "HeZZY"<gVYZ		"- "HeZZY"<gVYZ"(2)		". "HeZZY"<gVYZ"(2)		J c†
	B ċ	B Vm	B ċ	B Vm	B ċ	B Vm	
t _{INSUBIDIR}	2.4						ns
t _{INHBIDIR}	0.0						ns
t _{OUTCOBIDIR}	2.0	5.0					ns
t _{XZBIDIR}		7.1					ns
t _{ZXBIDIR}		7.1					ns
t _{INSUBIDIRPLL}	3.8						ns
t _{INHBIDIRPLL}	0.0						ns
t _{OUTCOBIDIRPLL}	0.5	2.1					ns
t _{XZBIDIRPLL}		4.2					ns
t _{ZXBIDIRPLL}		4.2					ns

I WZ, (#: E' %&%%B: [B 6M: 'i 'b ċ\`EVg/b ZiZg'*****Note (1)							
Hnb Wda	", "HeZZY"<gVYZ		"- "HeZZY"<gVYZ"(2)		". "HeZZY"<gVYZ"(2)		J c†
	B ċ	B Vm	B ċ	B Vm	B ċ	B Vm	
t _{SU}	0.3						ns
t _H	0.3						ns
t _{CO}		0.3					ns
t _{LUT}		0.6					ns

Table 78. EP20K1500C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.6						ns
t_{INHBIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.9						ns
$t_{\text{INHBIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Notes to tables:

- (1) Timing information is preliminary. Final timing information will be released in a future version of this data sheet.
- (2) Timing information for these devices will be released in a future version of this data sheet.

Tables 79 and 80 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at <http://www.altera.com>.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20KC devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20KC device can be loaded with one of five configuration schemes (see Table 81), chosen on the basis of the target application. An EPC16, EPC2, or EPC1 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20KC device. When a configuration device is used, the system can configure automatically at system power-up.