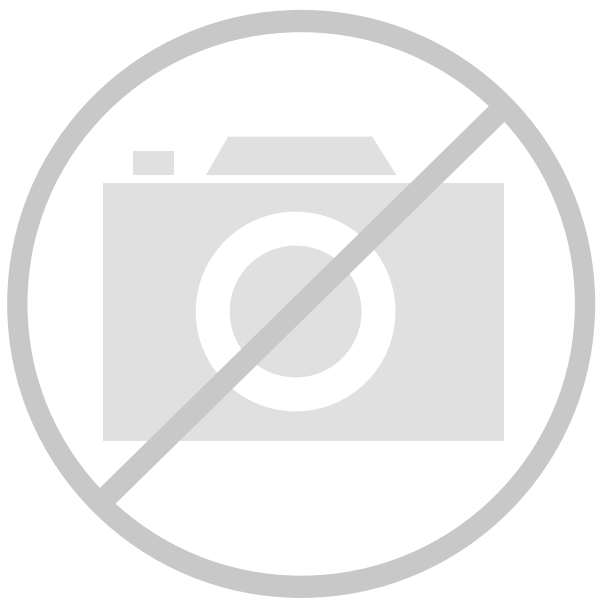




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	93
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100cf144c8es

General Description

Similar to APEX 20K and APEX 20KE devices, APEX 20KC devices offer the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20KC architecture uniquely suited for SOPC designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20KC device.

APEX 20KC devices include additional features such as enhanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. Table 7 shows the features included in APEX 20KC devices.

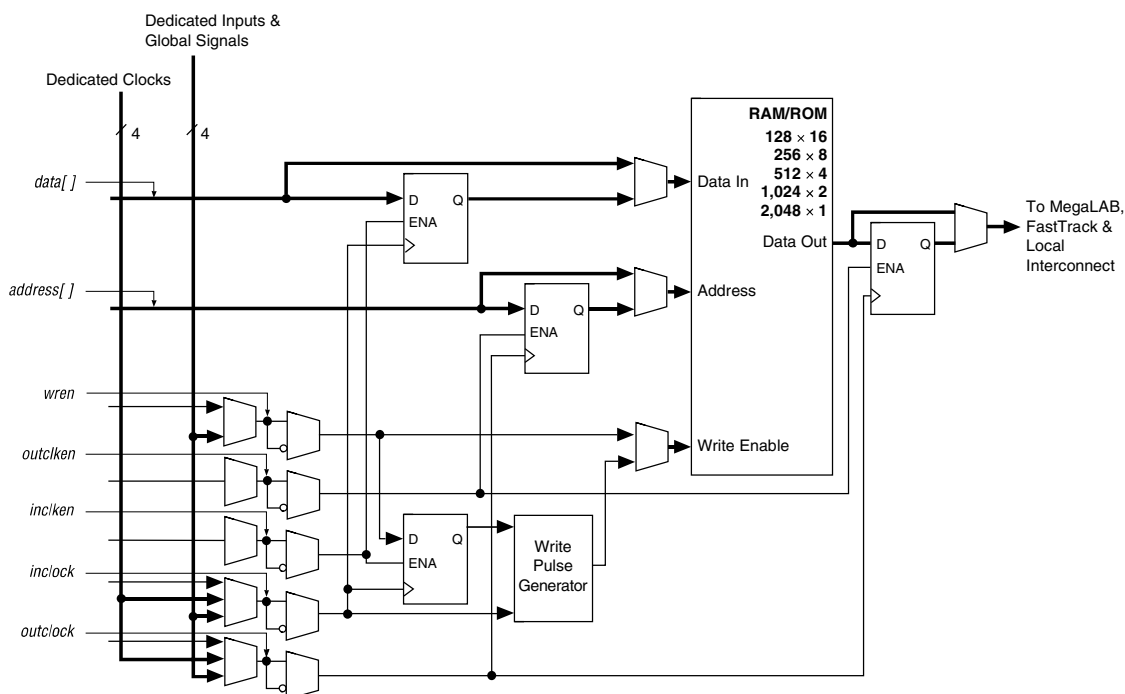
Table 7. APEX 20KC Device Features (Part 1 of 2)

Feature	APEX 20KC Devices
MultiCore system integration	Full support
Hot-socketing support	Full support
SignalTap logic analysis	Full support
32-/64-bit, 33-MHz PCI	Full compliance
32-/64-bit, 66-MHz PCI	Full compliance in -7 speed grade
MultiVolt I/O	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected bank by bank 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction $m/(n \times v)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift circuitry LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Eight

Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



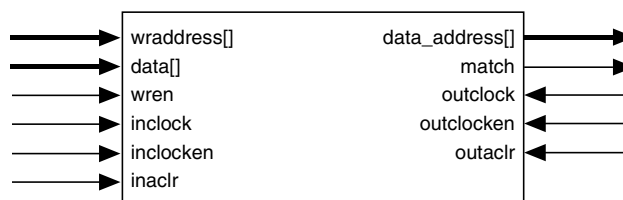
Note:

- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

Content-Addressable Memory

In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Figure 23. APEX 20KC CAM Block Diagram

CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KC on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KC device eliminates off-chip and on-chip delays, improving system performance.

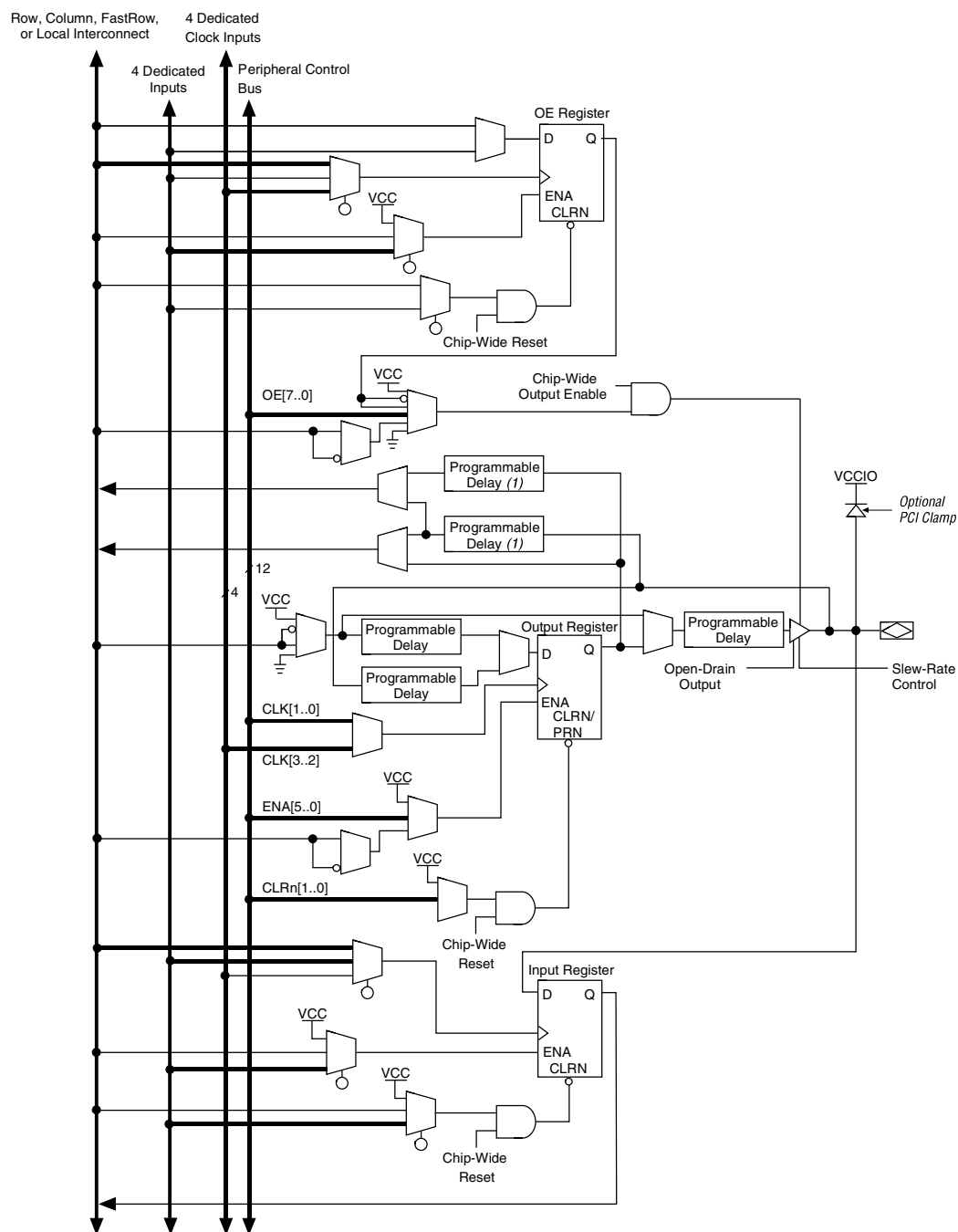
When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing “don’t care” bits into words of the memory. The “don’t care” bit can be used as a mask for CAM comparisons; any bit set to “don’t care” has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM’s output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When “don’t care” bits are used, a third clock cycle is required.

Figure 25. APEX 20KC Bidirectional I/O Registers *Notes (1), (2)***Notes:**

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

Figure 26. Row IOE Connection to the Interconnect

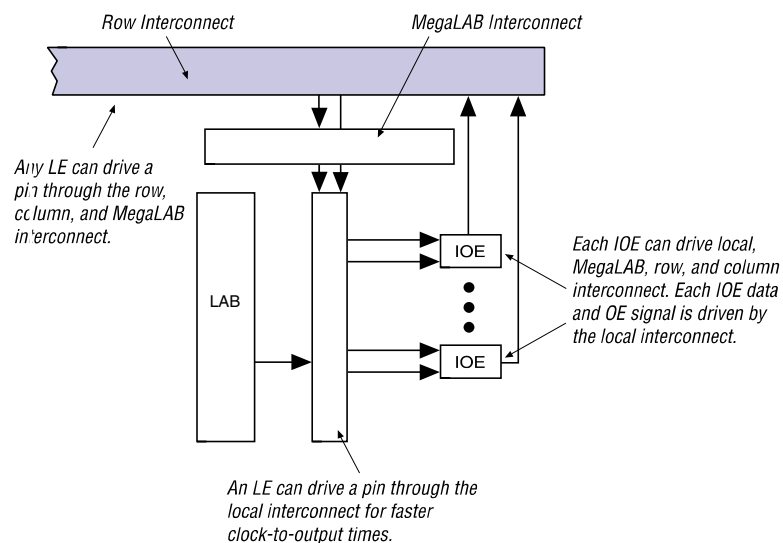


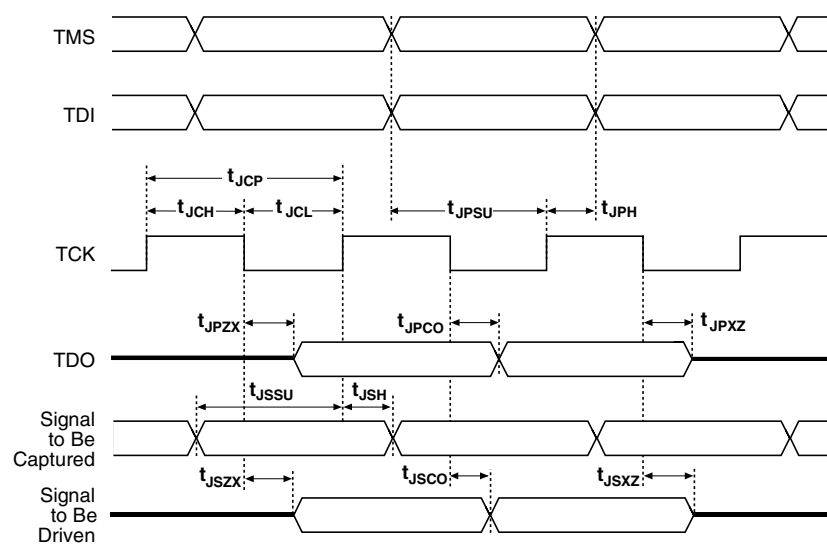
Figure 30. APEX 20KC JTAG Waveforms

Table 16 shows the JTAG timing parameters and values for APEX 20KC devices.

Table 16. APEX 20KC JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Table 20. APEX 20KC Device Capacitance *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V . During transitions, the inputs may undershoot to -0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms , and V_{CC} must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (6) Typical values are for $T_A = 25^\circ\text{C}$, $V_{CCINT} = 1.8\text{ V}$, and $V_{CCIO} = 1.8\text{ V}$, 2.5 V or 3.3 V .
- (7) These values are specified under the APEX 20KC device recommended operating conditions, shown in [Table 18 on page 53](#).
- (8) This value is specified for normal device operation. The value may vary during power-up.
- (9) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO} .
- (10) Capacitance is sample-tested only.

Tables 21 through 36 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

Table 21. LVTTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V}$ or 3.3 V	-10	10	μA
V_{OH}	High-level output voltage	$I_{OH} = -12\text{ mA}$, $V_{CCIO} = 3.0\text{ V}$ (1)	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 12\text{ mA}$, $V_{CCIO} = 3.0\text{ V}$ (2)		0.4	V

Table 22. LVC MOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V or } 3.3\text{ V}$	-10	10	μA
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0\text{ V}$ $I_{OH} = -0.1\text{ mA (1)}$	$V_{CCIO} - 0.2$		V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0\text{ V}$ $I_{OL} = 0.1\text{ mA (2)}$		0.2	V

Table 23. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.7	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V or } 3.3\text{ V}$	-10	10	μA
V_{OH}	High-level output voltage	$I_{OH} = -0.1\text{ mA (1)}$	2.1		V
		$I_{OH} = -1\text{ mA (1)}$	2.0		V
		$I_{OH} = -2\text{ mA (1)}$	1.7		V
V_{OL}	Low-level output voltage	$I_{OL} = 0.1\text{ mA (2)}$		0.2	V
		$I_{OL} = 1\text{ mA (2)}$		0.4	V
		$I_{OL} = 2\text{ mA (2)}$		0.7	V

Table 28. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		$V_{REF} + 0.1$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.1$	V
V_{OL}	Low-level output voltage	$I_{OL} = 36 \text{ mA}$ (2)			0.65	V

Table 29. SSTL-2 Class I Specifications

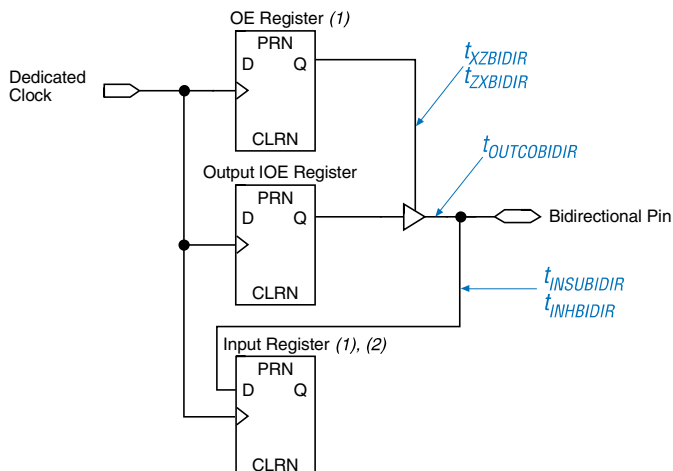
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -7.6 \text{ mA}$ (1)	$V_{TT} + 0.57$			V
V_{OL}	Low-level output voltage	$I_{OL} = 7.6 \text{ mA}$ (2)			$V_{TT} - 0.57$	V

Table 34. LVPECL Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output Supply Voltage	3.135	3.3	3.465	V
V_{IH}	Low-level input voltage	1300		1700	mV
V_{IL}	High-level input voltage	2100		2600	mV
V_{OH}	Low-level output voltage	1450		1650	mV
V_{OL}	High-level output voltage	2275		2420	mV
V_{ID}	Input voltage differential	400	600	950	mV
V_{OD}	Output voltage differential	625	800	950	mV
t_r, t_f	Rise/fall time (20 to 80%)	85		325	ps
t_{DSKEW}	Differential skew			25	ps
t_O	Output load		150		Ω
R_L	Receiver differential input resistor		100		Ω

Table 35. 3.3-V AGP I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = -500 \mu A$	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	$I_{OUT} = 1500 \mu A$			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	-10		10	μA

Figure 34. Synchronous Bidirectional Pin External Timing**Notes:**

- (1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin. Use the "Output Enable Routing = Single-Pin" option in the Quartus II software to set the output enable register.
- (2) Use the "Decrease Input Delay to Internal Cells = OFF" option in the Quartus II software to set the LAB-adjacent input register. This maintains a zero hold time for LAB-adjacent registers while giving a fast, position-independent setup time. Set "Decrease Input Delay to Internal Cells = ON" and move the input register farther away from the bidirectional pin for a faster setup time with zero hold time. The exact position where zero hold occurs with the minimum setup time varies with device density and speed grade.

Tables 37 to 39 describes the f_{MAX} timing parameters shown in Figure 33. Table 40 describes the functional timing parameters.

Table 37. APEX 20KC t_{MAX} LE Timing Parameters	
Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 45. EP20K100C t_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	1.0						ns

Table 46. EP20K100C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.3						ns
t_{CL}	2.3						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.3						ns
t_{ESBCL}	2.3						ns
t_{ESBWP}	1.1						ns
t_{ESBRP}	0.9						ns

Table 47. EP20K100C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.0						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.3						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 50. EP20K200C t_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.4					ns
t_{ESBSRC}		2.5					ns
t_{ESBAWC}		3.1					ns
t_{ESBSWC}		3.0					ns
$t_{ESBWASU}$	0.5						ns
t_{ESBWAH}	0.5						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.5						ns
$t_{ESBRASU}$	1.4						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.3						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.2						ns
$t_{ESBRADDRSU}$	0.2						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.3					ns
t_{ESBDD}		2.7					ns
t_{PD}		1.6					ns
$t_{PTERMSU}$	1.0						ns
$t_{PTERMCO}$		1.0					ns

Table 51. EP20K200C t_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	1.0						ns

Table 58. EP20K400C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.0						ns
t_{CL}	2.0						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.0						ns
t_{ESBCL}	2.0						ns
t_{ESBWP}	1.0						ns
t_{ESBRP}	0.8						ns

Table 59. EP20K400C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.2						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 62. EP20K600C t_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.4					ns
t_{ESBSRC}		2.5					ns
t_{ESBAWC}		3.1					ns
t_{ESBSWC}		3.0					ns
$t_{ESBWASU}$	0.5						ns
t_{ESBWAH}	0.5						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.5						ns
$t_{ESBRASU}$	1.4						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.3						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.2						ns
$t_{ESBRADDRSU}$	0.2						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.3					ns
t_{ESBDD}		2.7					ns
t_{PD}		1.6					ns
$t_{PTERMSU}$	1.0						ns
$t_{PTERMCO}$		1.0					ns

Table 63. EP20K600C t_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	2.2						ns

Table 64. EP20K600C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.3						ns
t_{CL}	2.3						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.3						ns
t_{ESBCL}	2.3						ns
t_{ESBWP}	1.1						ns
t_{ESBRP}	0.9						ns

Table 65. EP20K600C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.2						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.3						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 72. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.4						ns
t_{INHIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.8						ns
$t_{\text{INHIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 73. EP20K1500C f_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 74. EP20K1500C t_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 75. EP20K1500C t_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	1.4						ns
t_{F20+}	2.8						ns

Table 76. EP20K1500C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.0						ns
t_{CL}	2.0						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.0						ns
t_{ESBCL}	2.0						ns
t_{ESBWP}	1.0						ns
t_{ESBRP}	0.8						ns

Table 77. EP20K1500C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.2						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 79. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade ⁽¹⁾		-9 Speed Grade ⁽¹⁾		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.1					ns
1.8 V		0.5					ns
PCI		0.4					ns
GTL+		−0.3					ns
SSTL-3 Class I		−0.4					ns
SSTL-3 Class II		−0.4					ns
SSTL-2 Class I		−0.3					ns
SSTL-2 Class II		−0.3					ns
LVDS		−0.2					ns
CTT		−0.3					ns
AGP		0.0					ns

Table 80. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grade ⁽¹⁾		-9 Speed Grade ⁽¹⁾		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.5					ns
1.8 V		1.7					ns
PCI		−0.2					ns
GTL+		−0.4					ns
SSTL-3 Class I		−0.1					ns
SSTL-3 Class II		−0.6					ns
SSTL-2 Class I		0.0					ns
SSTL-2 Class II		−0.4					ns
LVDS		−0.8					ns
CTT		−0.2					ns
AGP		−0.4					ns

Note to tables:

(1) Timing information will be released in a future version of this data sheet.