



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

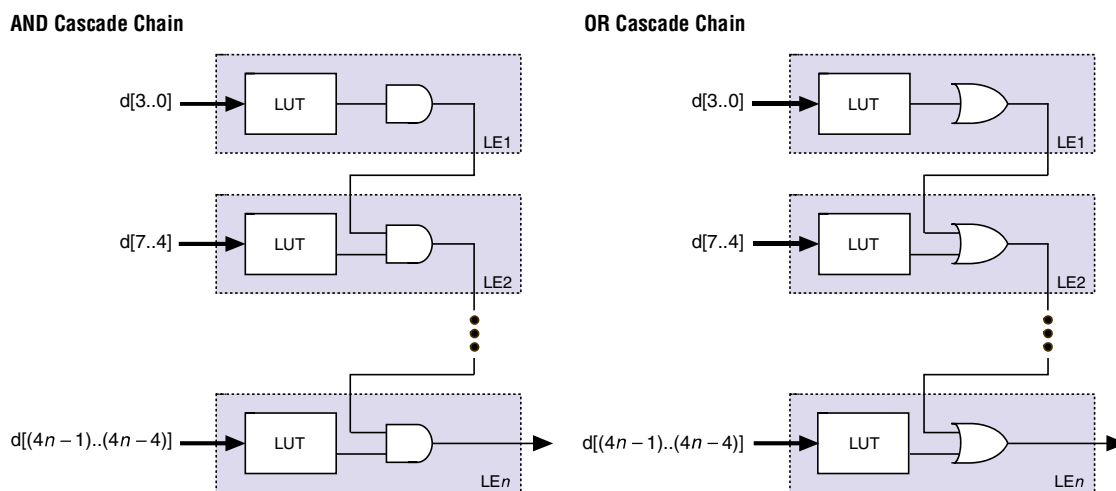
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	159
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100cq208c7

Cascade Chain

With the cascade chain, the APEX 20KC architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20KC Cascade Chain



Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 12. APEX 20KC FastRow Interconnect

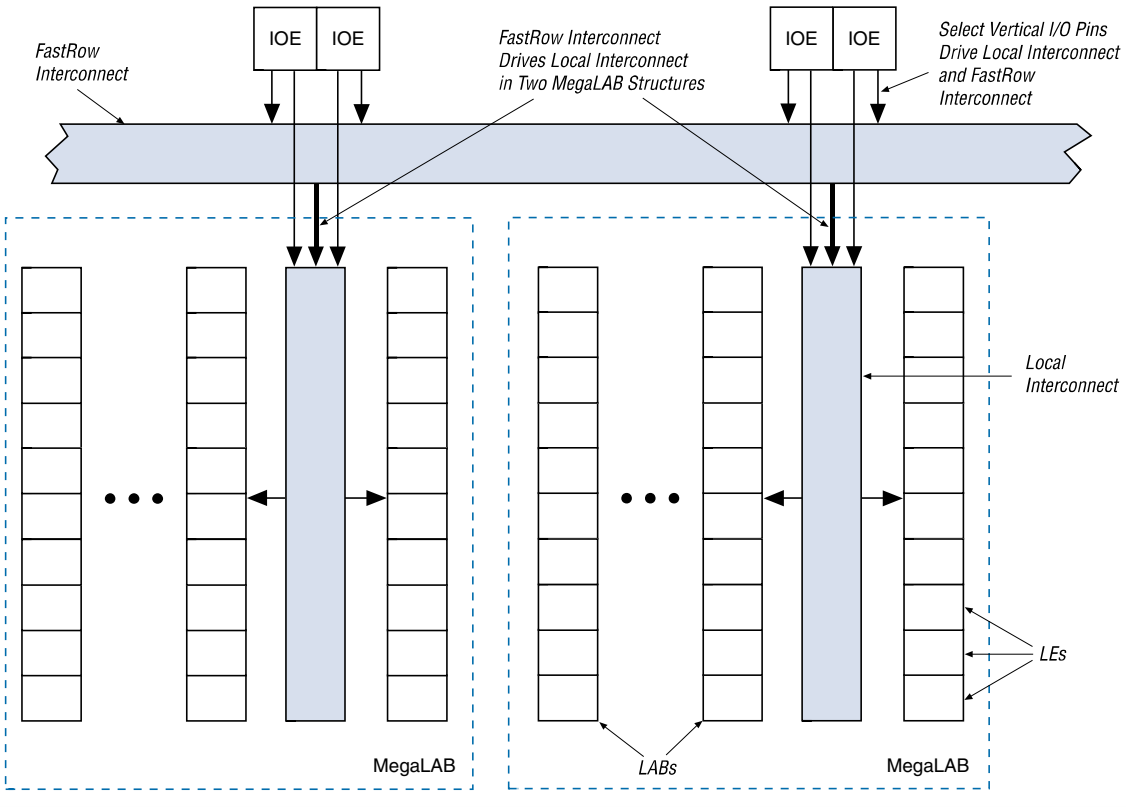


Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

Table 8. APEX 20KC Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O pin					✓	✓	✓	✓	
Column I/O pin					✓			✓	✓
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local interconnect	✓	✓	✓	✓					
MegaLAB interconnect					✓				
Row FastTrack interconnect						✓		✓	
Column FastTrack interconnect						✓	✓		
FastRow interconnect					✓				

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

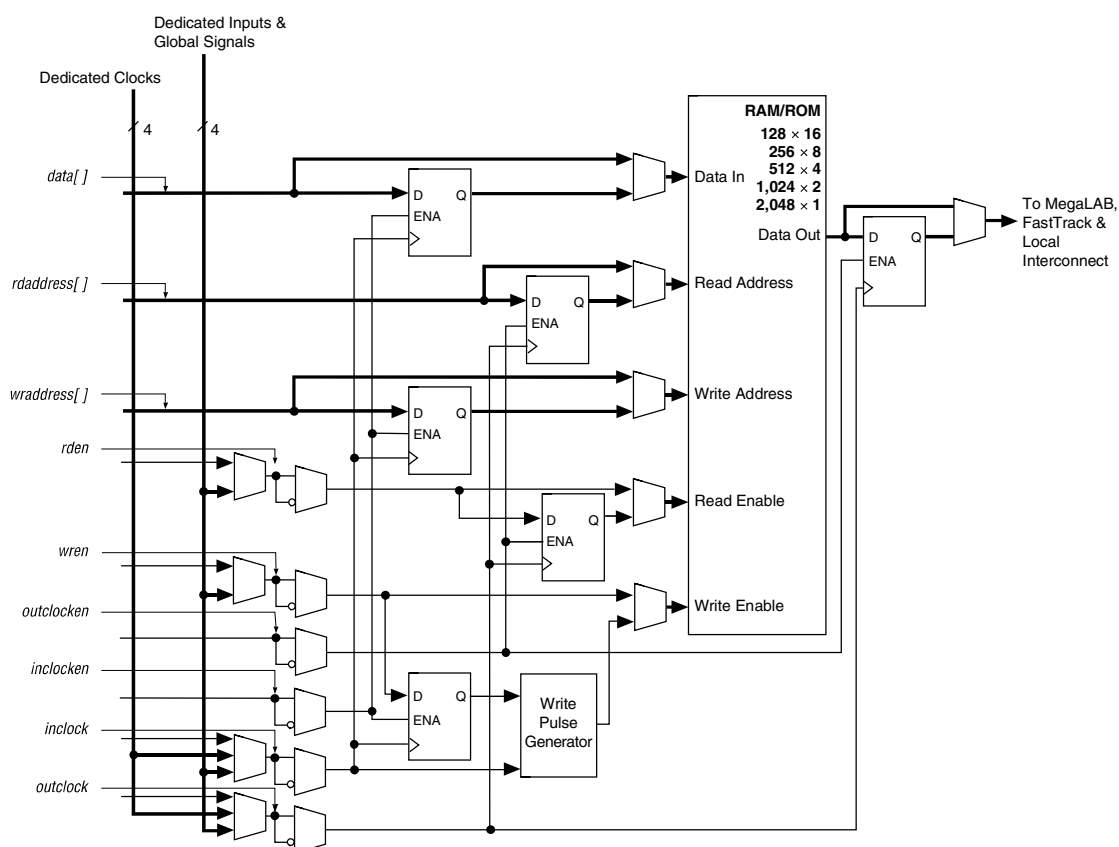
In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. [Figure 13](#) shows the ESB in product-term mode.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, $\overline{WE}$, and write address. The other clock controls all registers associated with reading: read enable ($\overline{RE}$), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies.

Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



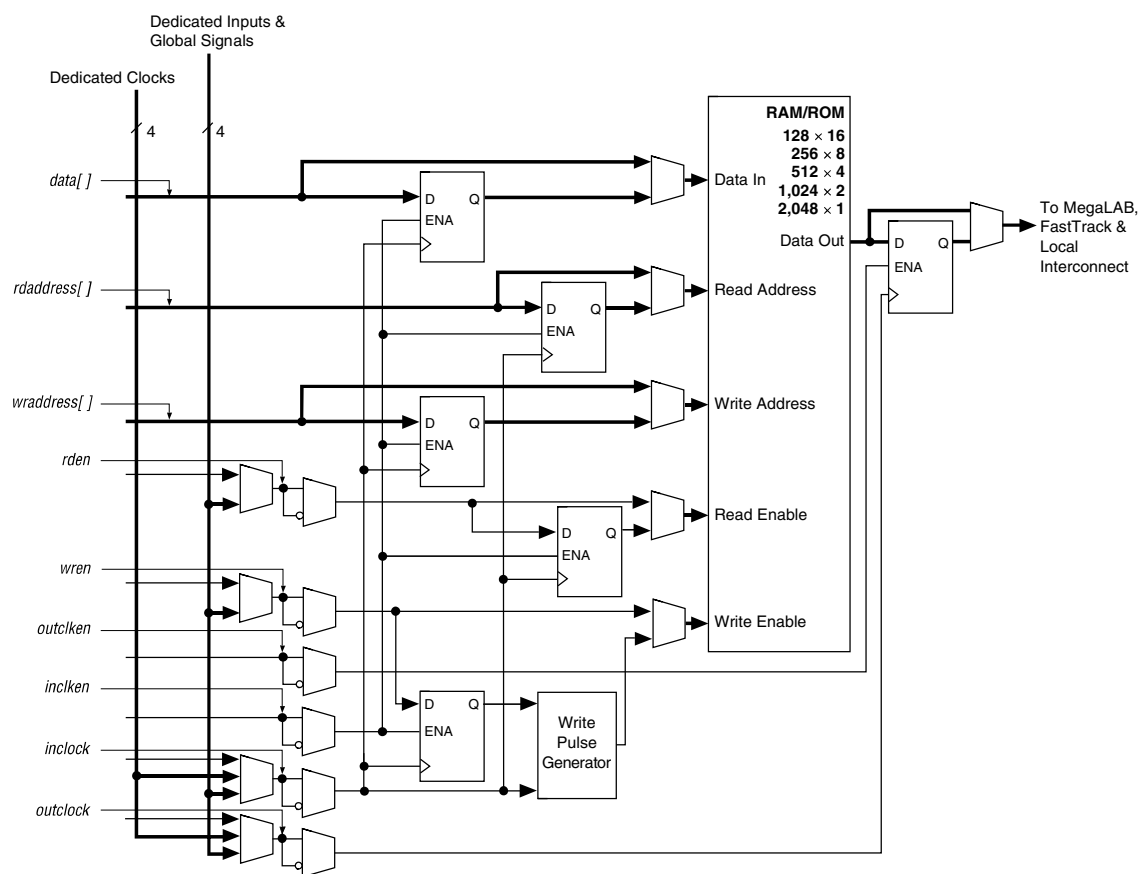
Note:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode *Note (1)*



Note:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

Tables 11 and 12 summarize the ClockLock and ClockBoost parameters for APEX 20KC devices.

Table 11. APEX 20KC ClockLock & ClockBoost Parameters <i>Note (1)</i>						
Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	%
$t_{OUTJITTER}$	RMS jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	%
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
$t_{LOCK}^{(2)},^{(3)}$	Time required for ClockLock or ClockBoost to acquire lock				40	μs

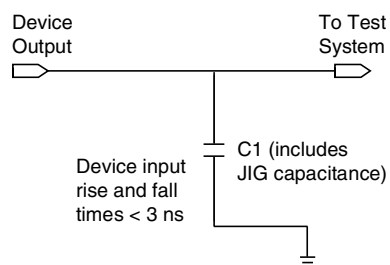
Table 12. APEX 20KC Clock Input & Output Parameters (Part 1 of 2) <i>Note (1)</i>							
Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
$f_{VCO}^{(4)}$	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	Clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	Clock1 PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external clock0 output	3.3-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz

Generic Testing

Each APEX 20KC device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20KC devices are made under conditions equivalent to those shown in Figure 31. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Figure 31. APEX 20KC AC Test Conditions



Operating Conditions

Tables 17 through 20 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KC devices.

Table 17. APEX 20KC Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground (2)	-0.5	2.5	V
V_{CCIO}			-0.5	4.6	V
V_I	DC input voltage		-0.5	4.6	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

Table 18. APEX 20KC Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V _I	Input voltage	(2), (5)	−0.5	4.1	V
V _O	Output voltage		0	V _{CCIO}	V
T _J	Junction temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
t _R	Input rise time (10% to 90%)			40	ns
t _F	Input fall time (90% to 10%)			40	ns

Table 19. APEX 20KC Device DC Operating Conditions Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _I	Input pin leakage current (8)	V _I = 4.1 to −0.5 V	−10		10	μA
I _{OZ}	Tri-stated I/O pin leakage current (8)	V _O = 4.1 to −0.5 V	−10		10	μA
I _{CC0}	V _{CC} supply current (standby) (All ESBs in power-down mode)	V _I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V _I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R _{CONF}	Value of I/O pin pull-up resistor before and during configuration	V _{CCIO} = 3.0 V (9)	20		50	kΩ
		V _{CCIO} = 2.375 V (9)	30		80	kΩ
		V _{CCIO} = 1.71 V (9)	60		150	kΩ



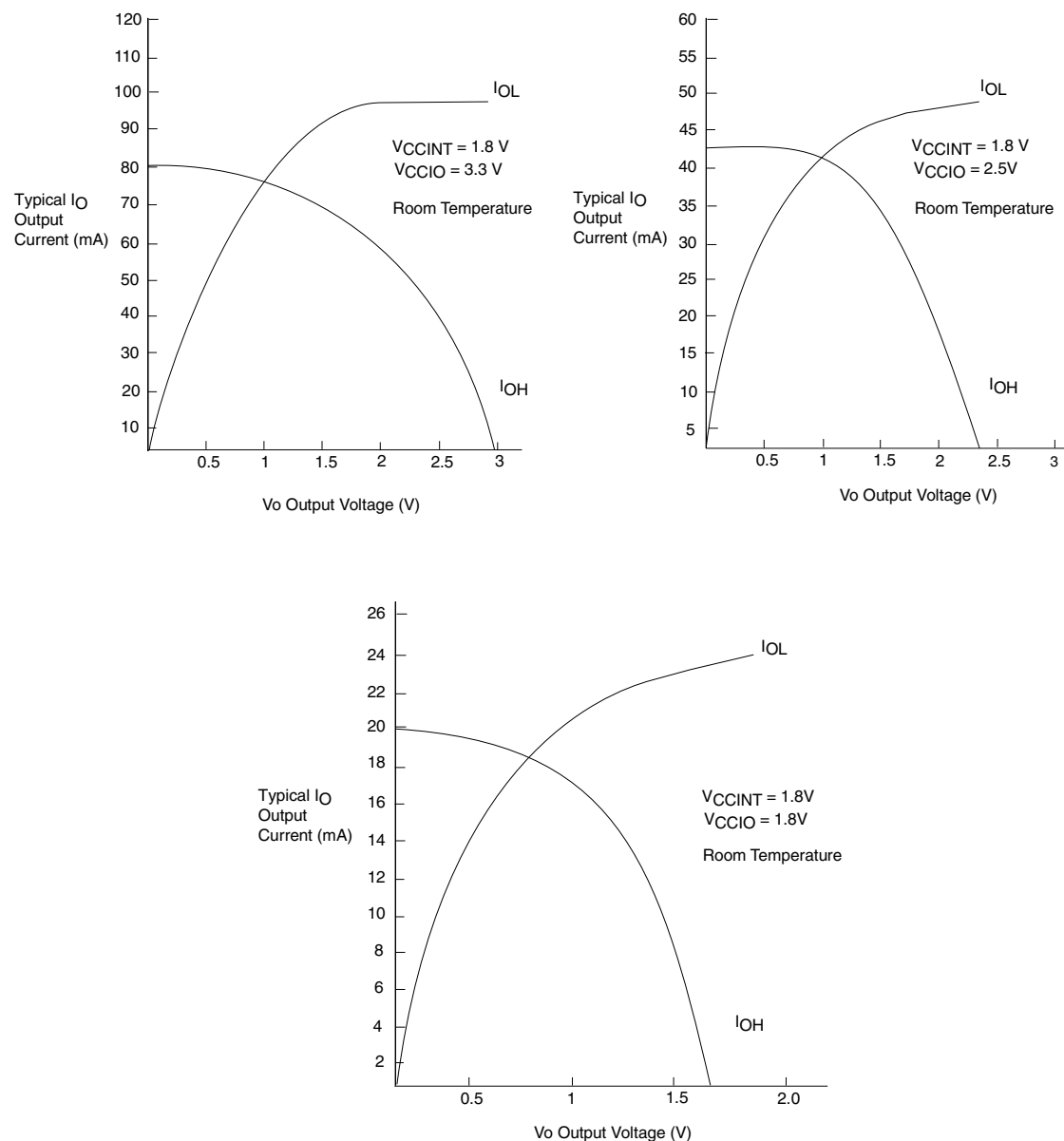
DC Operating Specifications on APEX 20KC I/O standards are listed in Tables 21 to 36.

Table 22. LVC MOS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Power supply voltage range		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V or } 3.3\text{ V}$	-10	10	μA
V_{OH}	High-level output voltage	$V_{CCIO} = 3.0\text{ V}$ $I_{OH} = -0.1\text{ mA (1)}$	$V_{CCIO} - 0.2$		V
V_{OL}	Low-level output voltage	$V_{CCIO} = 3.0\text{ V}$ $I_{OL} = 0.1\text{ mA (2)}$		0.2	V

Table 23. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.7	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V or } 3.3\text{ V}$	-10	10	μA
V_{OH}	High-level output voltage	$I_{OH} = -0.1\text{ mA (1)}$	2.1		V
		$I_{OH} = -1\text{ mA (1)}$	2.0		V
		$I_{OH} = -2\text{ mA (1)}$	1.7		V
V_{OL}	Low-level output voltage	$I_{OL} = 0.1\text{ mA (2)}$		0.2	V
		$I_{OL} = 1\text{ mA (2)}$		0.4	V
		$I_{OL} = 2\text{ mA (2)}$		0.7	V

Figure 32. Output Drive Characteristics of APEX 20KC Devices

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 33 shows the f_{MAX} timing model for APEX 20KC devices.

Figure 33. f_{MAX} Timing Model

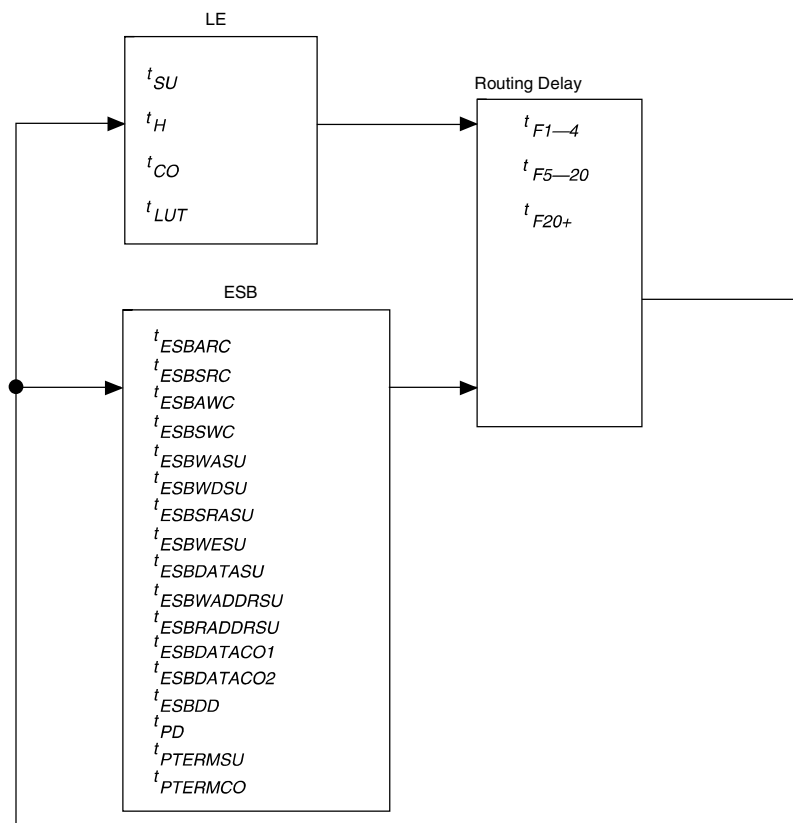


Figure 34 shows the timing model for bidirectional I/O pin timing.

Table 40. APEX 20KC Minimum Pulse Width Timing Parameters

Symbol	Parameter
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 41 and 42 describe APEX 20KC external timing parameters.

Table 41. APEX 20KC External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF

Table 42. APEX 20KC External Bidirectional Timing Parameters *Note (1)*

Symbol	Parameter	Condition
$t_{\text{INSUBIDIR}}$	Setup time for bidirectional pins with global clock at LAB-adjacent input register	
t_{INHBIDIR}	Hold time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
t_{XZBIDIR}	Synchronous output enable register to output buffer disable delay	C1 = 35 pF
t_{ZXBIDIR}	Synchronous output enable register to output buffer enable delay	C1 = 35 pF
$t_{\text{INSUBIDIRPLL}}$	Setup time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{\text{INHBIDIRPLL}}$	Hold time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{\text{OUTCOBIDIRPLL}}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE register	C1 = 35 pF
$t_{\text{XZBIDIRPLL}}$	Synchronous output enable register to output buffer disable delay with PLL	C1 = 35 pF
$t_{\text{ZXBIDIRPLL}}$	Synchronous output enable register to output buffer enable delay with PLL	C1 = 35 pF

Note to tables:

(1) These timing parameters are sample-tested only.

Table 56. EP20K400C t_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 57. EP20K400C t_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	2.2						ns

Table 66. EP20K600C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.4						ns
t_{INHBIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.9						ns
$t_{\text{INHBIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 67. EP20K1000C f_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 68. EP20K1000C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.5						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 69. EP20K1000C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	1.3						ns
t_{F20+}	2.6						ns

Table 74. EP20K1500C t_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 75. EP20K1500C t_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	1.4						ns
t_{F20+}	2.8						ns

Table 78. EP20K1500C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade ⁽²⁾		-9 Speed Grade ⁽²⁾		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	2.6						ns
t _{INHBIDIR}	0.0						ns
t _{OUTCOBIDIR}	2.0	5.0					ns
t _{XZBIDIR}		7.1					ns
t _{ZXBIDIR}		7.1					ns
t _{INSUBIDIRPLL}	3.9						ns
t _{INHBIDIRPLL}	0.0						ns
t _{OUTCOBIDIRPLL}	0.5	2.1					ns
t _{XZBIDIRPLL}		4.2					ns
t _{ZXBIDIRPLL}		4.2					ns

Notes to tables:

- (1) Timing information is preliminary. Final timing information will be released in a future version of this data sheet.
 (2) Timing information for these devices will be released in a future version of this data sheet.

Tables 79 and 80 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at <http://www.altera.com>.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20KC devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20KC device can be loaded with one of five configuration schemes (see Table 81), chosen on the basis of the target application. An EPC16, EPC2, or EPC1 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20KC device. When a configuration device is used, the system can configure automatically at system power-up.