Intel - EP20K100CQ208C8ES Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

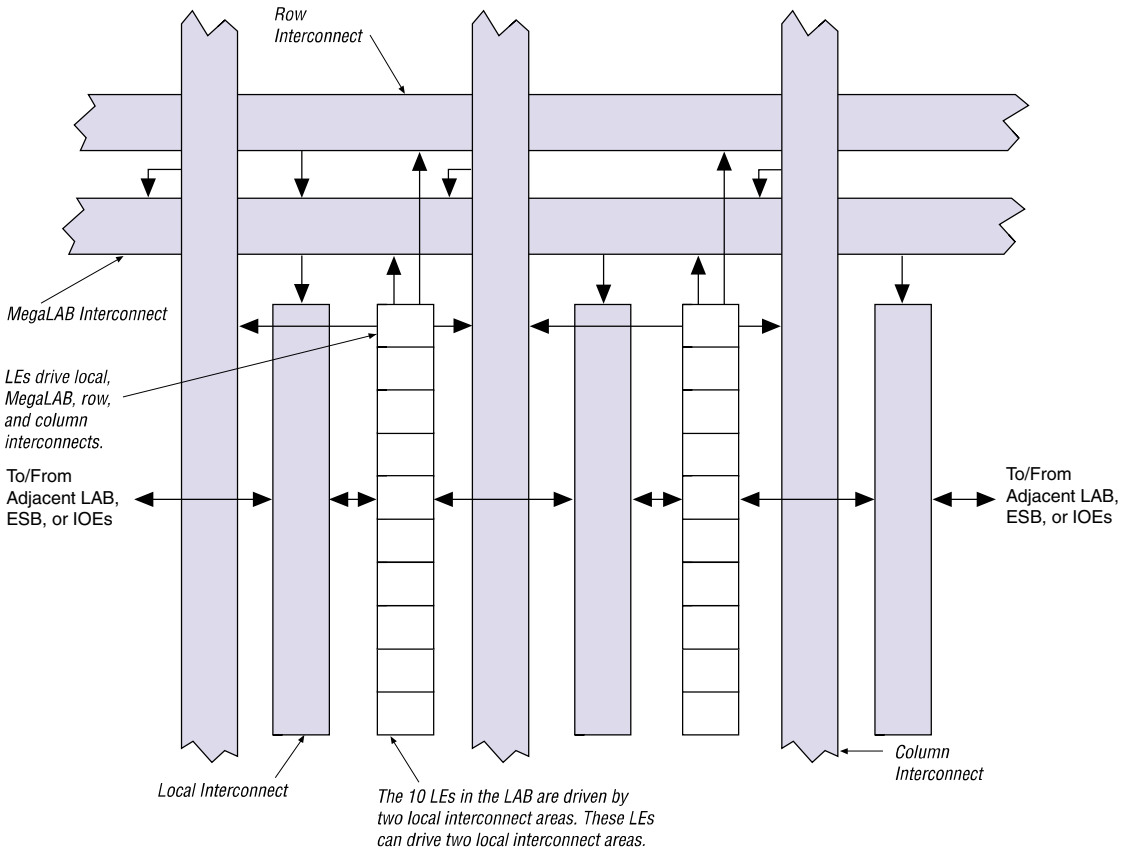
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	159
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100cq208c8es

Figure 3. LAB Structure



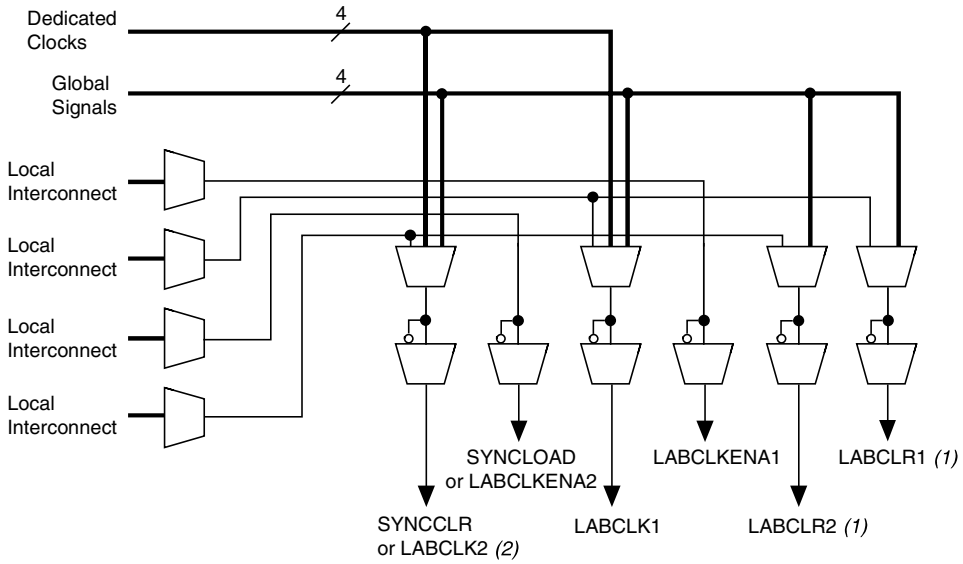
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation

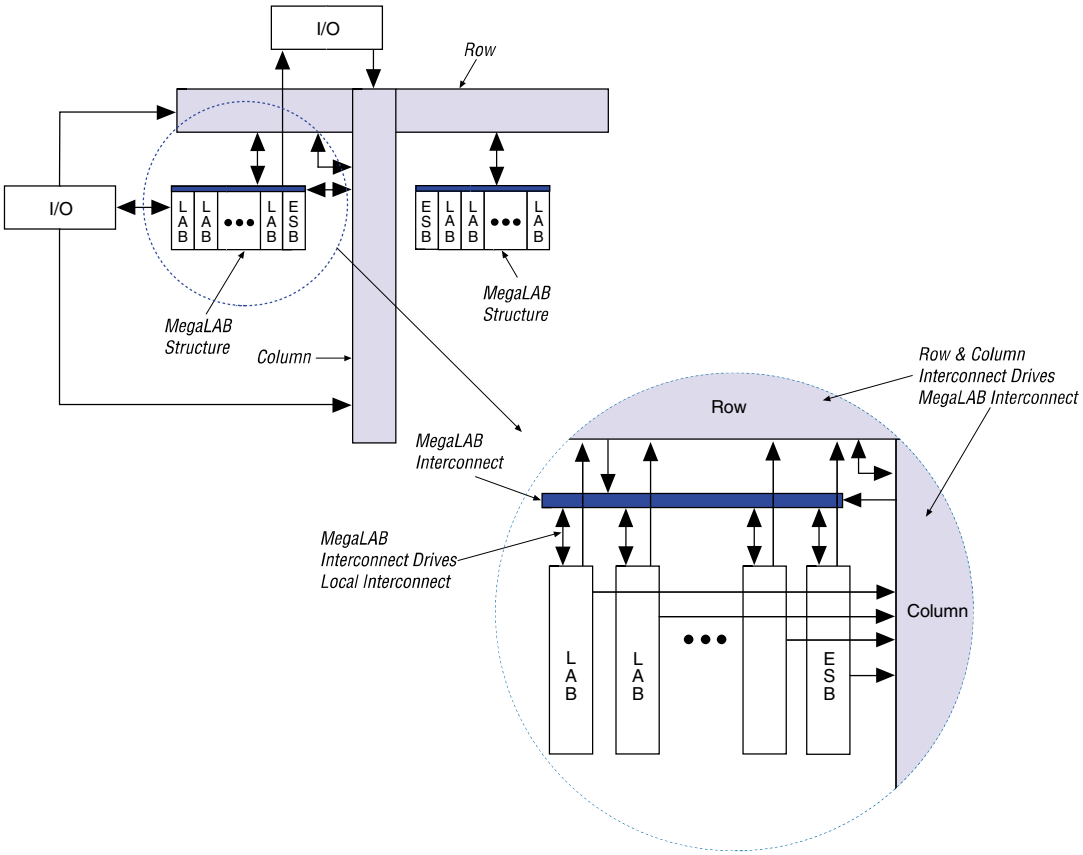


Notes:
(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE, the smallest unit of logic in the APEX 20KC architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Figure 10. FastTrack Connection to Local Interconnect



ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the FastTrack or MegaLAB interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the FastTrack and MegaLAB interconnects. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

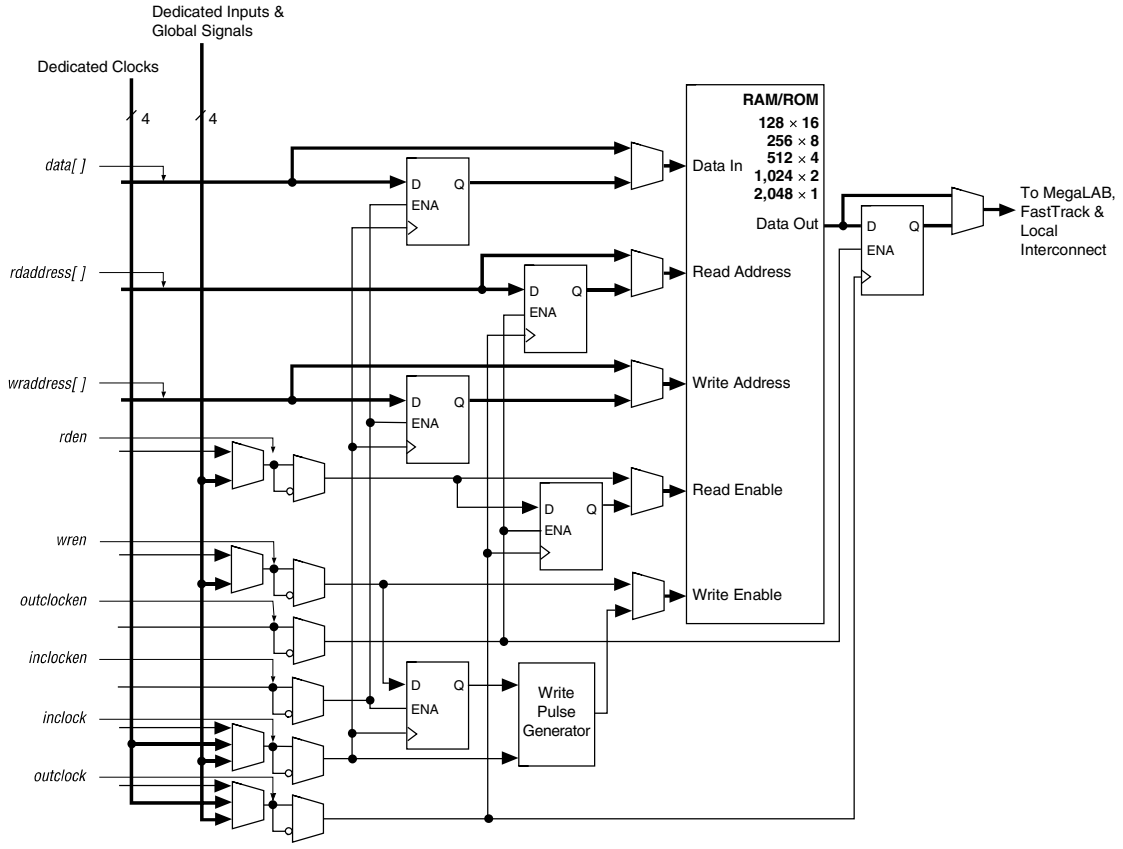
When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Note:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

Open-drain output pins on APEX 20KC devices (with a series resistor and a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

ClockLock & ClockBoost Features

APEX 20KC devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20KC devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20KC device's high-speed clock to provide significant improvements in system performance and bandwidth. APEX 20KC devices in -7 and -8 speed grades include the ClockLock feature.

The ClockLock and ClockBoost features in APEX 20KC devices are enabled through the Quartus II software. External devices are not required to use these features.

APEX 20KC ClockLock Feature

APEX 20KC devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K100C and EP20K200C devices have two PLLs; the EP20K400C and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KC PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KC device and another high-speed device, such as SDRAM.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20KC devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20KC devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20KC devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20KC devices support the JTAG instructions shown in Table 13.

Table 13. APEX 20KC JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20KC device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Table 18. APEX 20KC Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time (10% to 90%)			40	ns
t_F	Input fall time (90% to 10%)			40	ns

Table 19. APEX 20KC Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current *(8)*	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current *(8)*	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

☞ DC Operating Specifications on APEX 20KC I/O standards are listed in Tables 21 to 36.

Table 24. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.7	1.9	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage			0.35 × V_{CCIO}	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(1)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.45	V

Table 25. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 30. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(2)*			V_{TT} – 0.76	V

Table 31. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			V_{TT} – 0.6	V

Figure 33 shows the f_{MAX} timing model for APEX 20KC devices.

Figure 33. f_{MAX} Timing Model

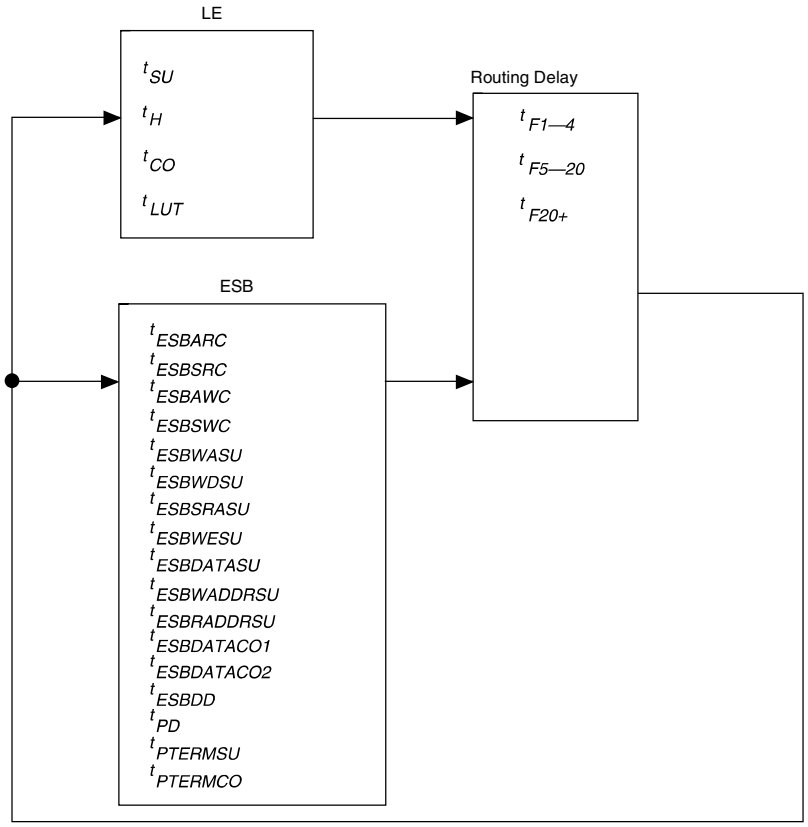


Figure 34 shows the timing model for bidirectional I/O pin timing.

Table 38. APEX 20KC f_{MAX} ESB Timing Parameters

Symbol	Parameter
t_{ESBARC}	ESB asynchronous read cycle time
t_{ESBSRC}	ESB synchronous read cycle time
t_{ESBAWC}	ESB asynchronous write cycle time
t_{ESBSWC}	ESB synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay

Table 39. APEX 20KC f_{MAX} Routing Delays

Symbol	Parameter
t_{F1-4}	Fan-out delay estimate using local interconnect
t_{F5-20}	Fan-out delay estimate using MegaLab interconnect
t_{F20+}	Fan-out delay estimate using FastTrack interconnect

Table 40. APEX 20KC Minimum Pulse Width Timing Parameters

Symbol	Parameter
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 41 and 42 describe APEX 20KC external timing parameters.

Table 41. APEX 20KC External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF

Table 42. APEX 20KC External Bidirectional Timing Parameters *Note (1)*

Symbol	Parameter	Condition
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{XZBIDIR}$	Synchronous output enable register to output buffer disable delay	C1 = 35 pF
$t_{ZXBIDIR}$	Synchronous output enable register to output buffer enable delay	C1 = 35 pF
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE register	C1 = 35 pF
$t_{XZBIDIRPLL}$	Synchronous output enable register to output buffer disable delay with PLL	C1 = 35 pF
$t_{ZXBIDIRPLL}$	Synchronous output enable register to output buffer enable delay with PLL	C1 = 35 pF

Note to tables:
(1) These timing parameters are sample-tested only.

Table 50. EP20K200C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.4					ns
t_{ESBSRC}		2.5					ns
t_{ESBAWC}		3.1					ns
t_{ESBSWC}		3.0					ns
$t_{ESBWASU}$	0.5						ns
t_{ESBWAH}	0.5						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.5						ns
$t_{ESBRASU}$	1.4						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.3						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.2						ns
$t_{ESBRADDRSU}$	0.2						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.3					ns
t_{ESBDD}		2.7					ns
t_{PD}		1.6					ns
$t_{PTERMSU}$	1.0						ns
$t_{PTERMCO}$		1.0					ns

Table 51. EP20K200C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	1.0						ns

Table 52. EP20K200C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.2						ns
t_{CL}	2.3						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.3						ns
t_{ESBCL}	2.3						ns
t_{ESBWP}	1.1						ns
t_{ESBRP}	0.9						ns

Table 53. EP20K200C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.0						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.3						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 62. EP20K600C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.4					ns
t_{ESBSRC}		2.5					ns
t_{ESBAWC}		3.1					ns
t_{ESBSWC}		3.0					ns
$t_{ESBWASU}$	0.5						ns
t_{ESBWAH}	0.5						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.5						ns
$t_{ESBRASU}$	1.4						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.3						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.2						ns
$t_{ESBRADDRSU}$	0.2						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.3					ns
t_{ESBDD}		2.7					ns
t_{PD}		1.6					ns
$t_{PTERMSU}$	1.0						ns
$t_{PTERMCO}$		1.0					ns

Table 63. EP20K600C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	2.2						ns

Table 66. EP20K600C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.4						ns
$t_{INHBIDIR}$	0.0						ns
$t_{OUTCOBIDIR}$	2.0	5.0					ns
$t_{XZBIDIR}$		7.1					ns
$t_{ZXBIDIR}$		7.1					ns
$t_{INSUBIDIRPLL}$	3.9						ns
$t_{INHBIDIRPLL}$	0.0						ns
$t_{OUTCOBIDIRPLL}$	0.5	2.1					ns
$t_{XZBIDIRPLL}$		4.2					ns
$t_{ZXBIDIRPLL}$		4.2					ns

Table 67. EP20K1000C f_{MAX} LE Timing Parameters Note (1)

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 74. EP20K1500C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 75. EP20K1500C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	1.4						ns
t_{F20+}	2.8						ns

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com