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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	159
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100cq208c9

…and More Features

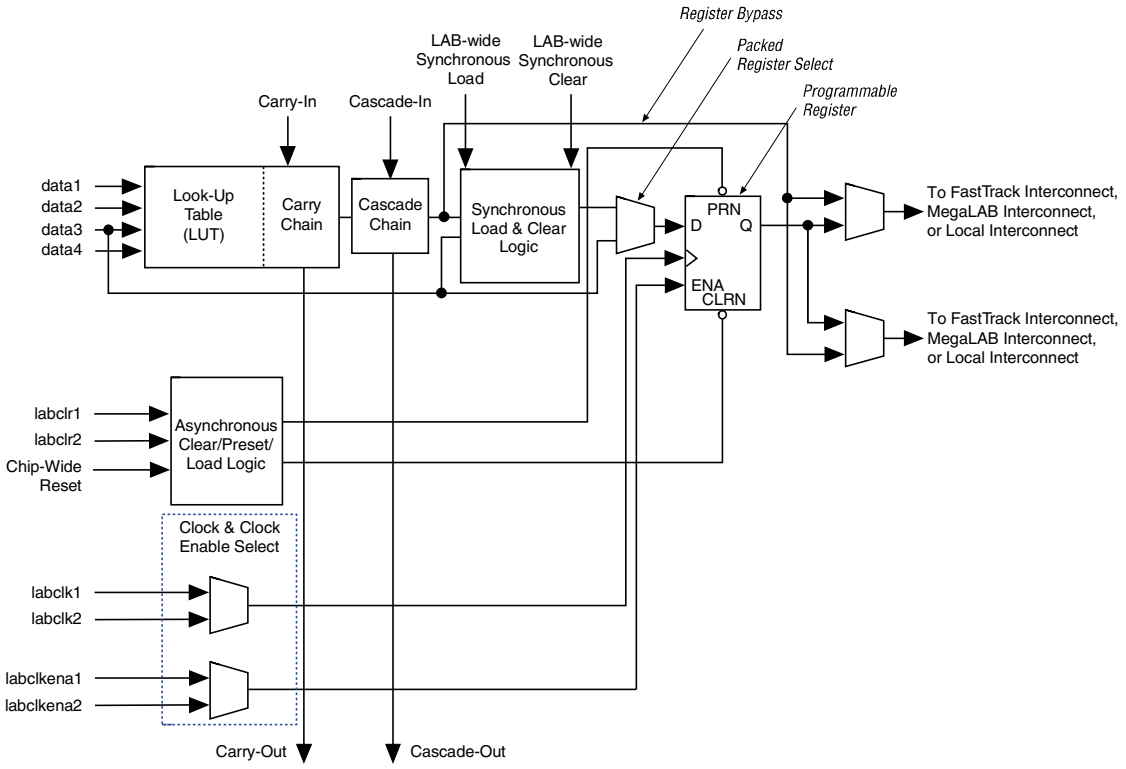
- Low-power operation design
  - 1.8-V supply voltage (see Table 2)
  - Copper interconnect reduces power consumption
  - MultiVolt™ I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - ESBs offering programmable power-saving mode
- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication and division
  - ClockShift™ feature providing programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR synchronous dynamic RAM (SDRAM) and ZBT static RAM (SRAM)
  - 16 input and 16 output LVDS channels
  - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
  - MultiVolt I/O support for 1.8-V, 2.5-V, and 3.3-V interfaces
  - Programmable clamp to V_{CCIO}
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, SSTL-3 and SSTL-2, GTL+, and HSTL Class I
  - Supports hot-socketing operation
  - Pull-up on I/O pins before and during configuration

Table 2. APEX 20KC Supply Voltages

Feature	Voltage
Internal supply voltage (V_{CCINT})	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)*

Note:
(1) APEX 20KC devices can be 5.0-V tolerant by using an external resistor.

Figure 5. APEX 20KC Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

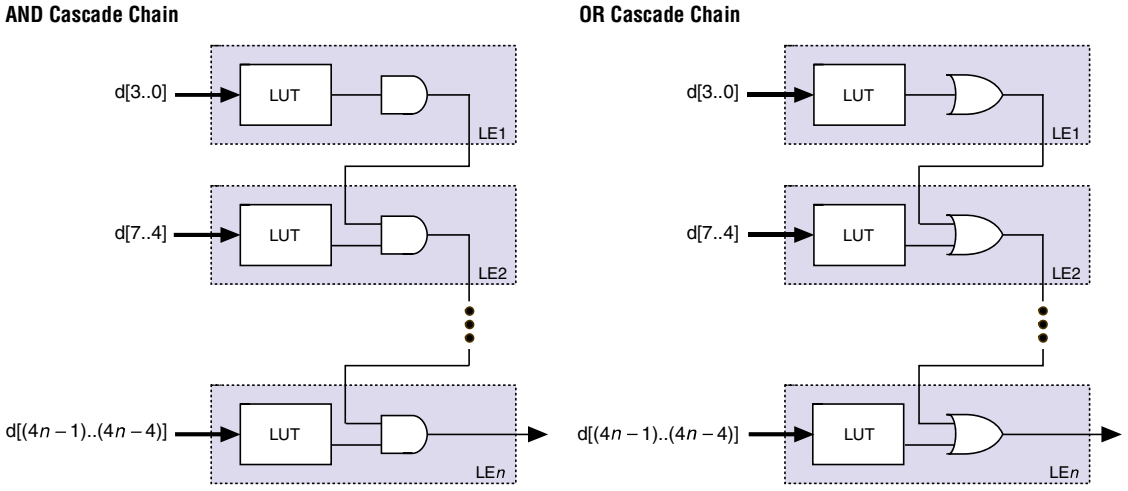
Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

Cascade Chain

With the cascade chain, the APEX 20KC architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical `AND` or logical `OR` (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20KC Cascade Chain



LE Operating Modes

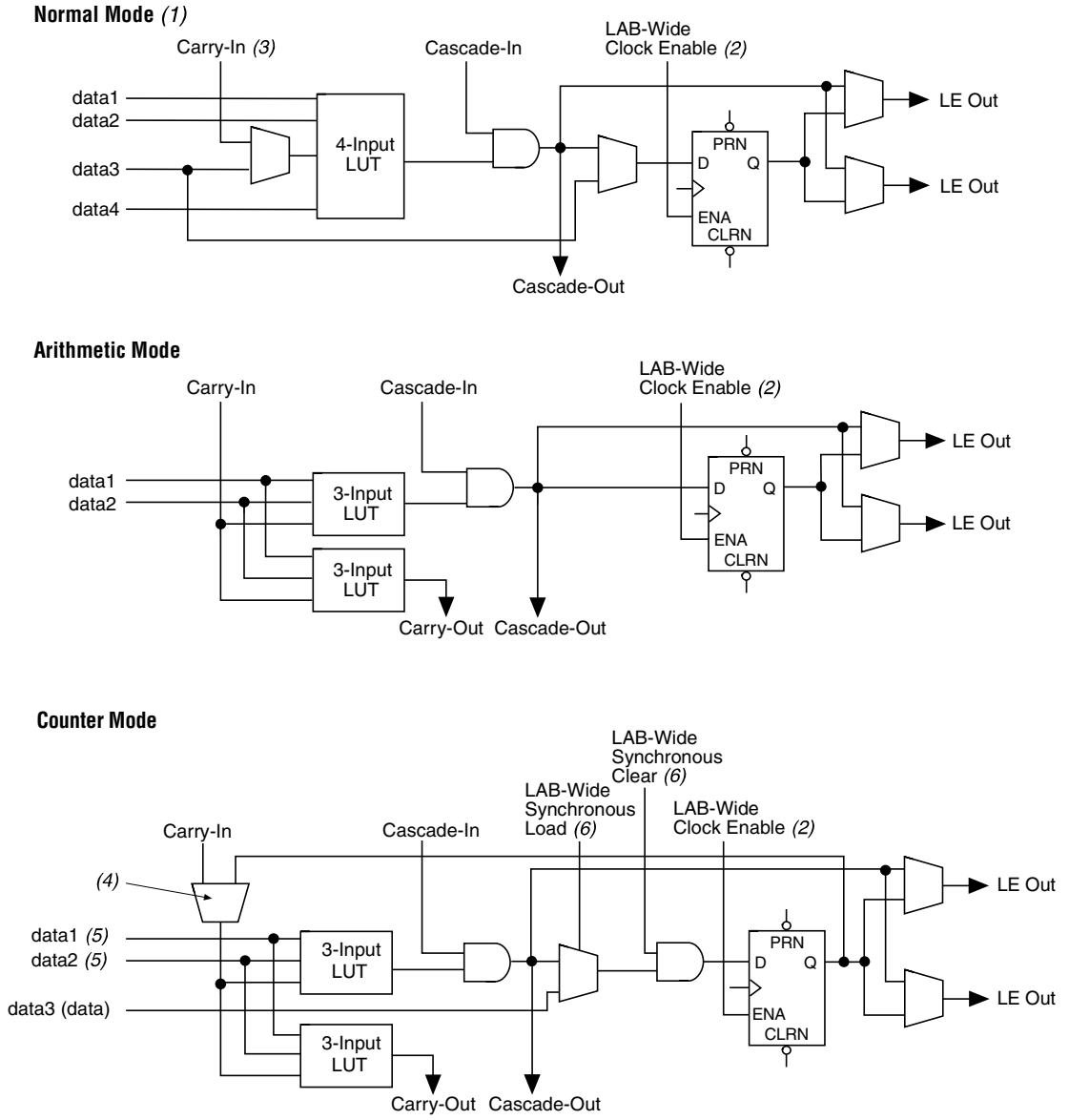
The APEX 20KC LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

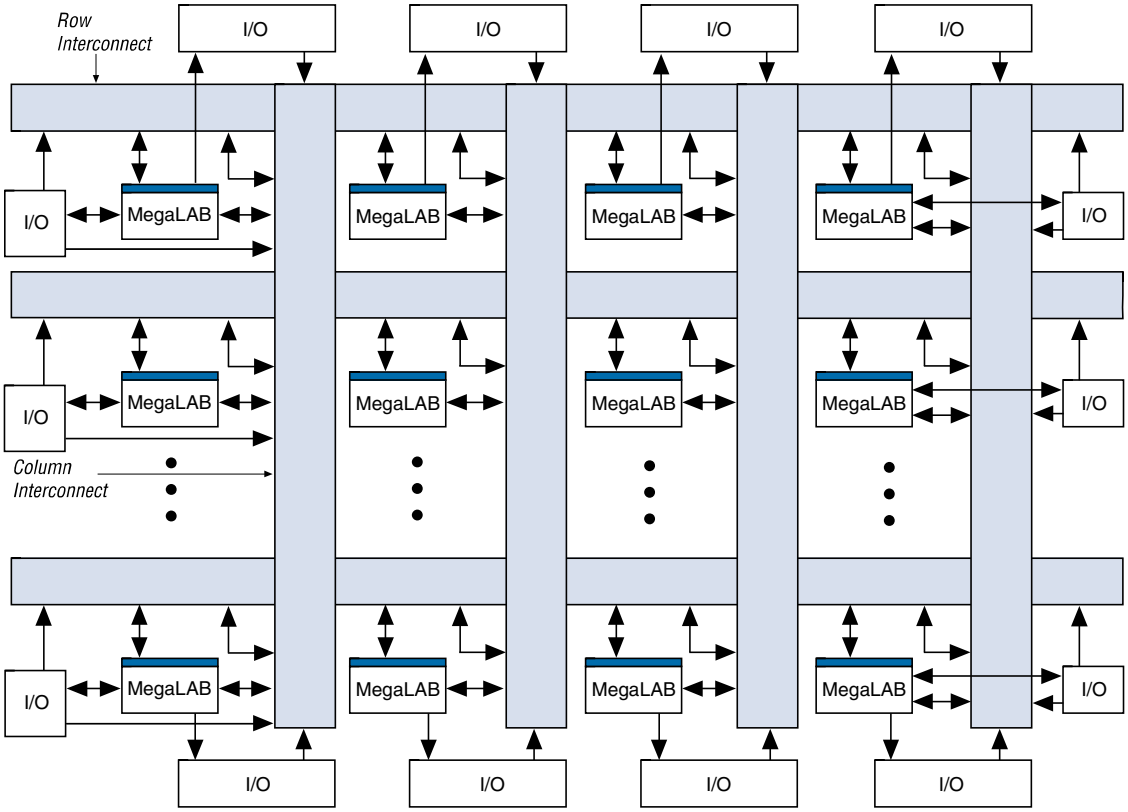
The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 8. APEX 20KC LE Operating Modes



Notes:
(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

Figure 9. APEX 20KC Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

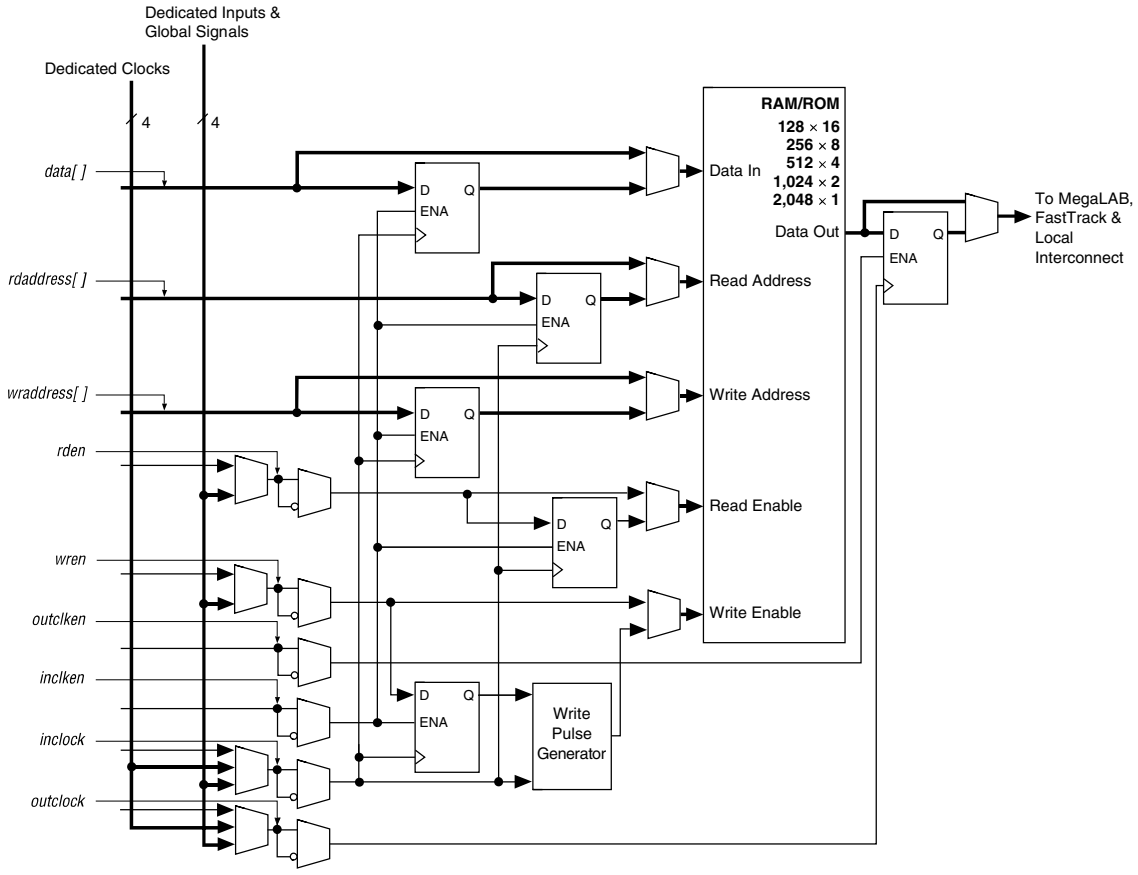
A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode *Note (1)*



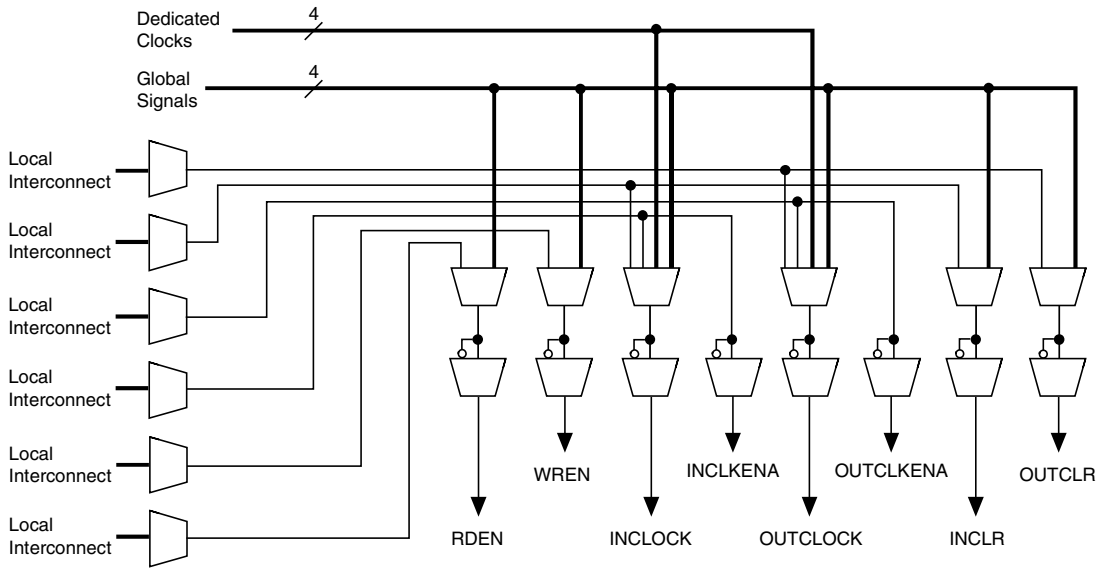
Note:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

For more information on APEX 20KC devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation



An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ (1)	✓ (1)		✓			
2.5		✓	✓ (1)			✓		
3.3		✓	✓	✓ (2)		✓ (3)	✓	✓

Notes:
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.
(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor.
(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Clock Multiplication

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KC ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

Table 12. APEX 20KC Clock Input & Output Parameters (Part 2 of 2) Note (1)

Symbol	Parameter	I/O Standard	-7 Speed Grade		-8 Speed Grade		Units
			Min	Max	Min	Max	
f_{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3-V LVTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz
f_{IN}	Input clock frequency	3.3-V LVTTL	(5)	(5)	(5)	(5)	MHz
		2.5-V LVTTL	(5)	(5)	(5)	(5)	MHz
		1.8-V LVTTL	(5)	(5)	(5)	(5)	MHz
		GTL+	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-2 Class II	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class I	(5)	(5)	(5)	(5)	MHz
		SSTL-3 Class II	(5)	(5)	(5)	(5)	MHz
		LVDS	(5)	(5)	(5)	(5)	MHz

Notes to tables:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2,000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs remain disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ≤ f_{VCO} ≤ 840 MHz for LVDS mode.
(5) Contact Altera Applications for information on these parameters.

SignalTap Embedded Logic Analyzer

APEX 20KC devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20KC device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

Table 18. APEX 20KC Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2)*, *(5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time (10% to 90%)			40	ns
t_F	Input fall time (90% to 10%)			40	ns

Table 19. APEX 20KC Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input pin leakage current *(8)*	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current *(8)*	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

☞ DC Operating Specifications on APEX 20KC I/O standards are listed in Tables 21 to 36.

Table 20. APEX 20KC Device Capacitance *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20KC device recommended operating conditions, shown in Table 18 on page 53.
(8) This value is specified for normal device operation. The value may vary during power-up.
(9) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(10) Capacitance is sample-tested only.

Tables 21 through 36 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

Table 21. LVTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or 3.3 V	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –12 mA, V_{CCIO} = 3.0 V *(1)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA, V_{CCIO} = 3.0 V *(2)*		0.4	V

Table 36. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF} *(3)*	Termination and reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high Z)	$GND \le V_{OUT} \le V_{CCIO}$	–10		10	µA

Notes to tables:

(1) The I_{OH} parameter refers to high-level output current.
(2) The I_{OL} parameter refers to low-level output current. This parameter applies to open-drain pins as well as output pins.
(3) V_{REF} specifies center point of switching range.

Figure 32 shows the output drive characteristics of APEX 20KC devices.

Table 48. EP20K100C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.9						ns
$t_{INHBIDIR}$	0.0						ns
$t_{OUTCOBIDIR}$	2.0	5.0					ns
$t_{XZBIDIR}$		7.1					ns
$t_{ZXBIDIR}$		7.1					ns
$t_{INSUBIDIRPLL}$	3.9						ns
$t_{INHBIDIRPLL}$	0.0						ns
$t_{OUTCOBIDIRPLL}$	0.5	2.1					ns
$t_{XZBIDIRPLL}$		4.2					ns
$t_{ZXBIDIRPLL}$		4.2					ns

Table 49. EP20K200C f_{MAX} LE Timing Parameters Note (1)

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.7					ns

Table 50. EP20K200C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.4					ns
t_{ESBSRC}		2.5					ns
t_{ESBAWC}		3.1					ns
t_{ESBSWC}		3.0					ns
$t_{ESBWASU}$	0.5						ns
t_{ESBWAH}	0.5						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.5						ns
$t_{ESBRASU}$	1.4						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.3						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.2						ns
$t_{ESBRADDRSU}$	0.2						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.3					ns
t_{ESBDD}		2.7					ns
t_{PD}		1.6					ns
$t_{PTERMSU}$	1.0						ns
$t_{PTERMCO}$		1.0					ns

Table 51. EP20K200C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	1.0						ns

Table 68. EP20K1000C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.5						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 69. EP20K1000C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	1.3						ns
t_{F20+}	2.6						ns

Table 72. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.4						ns
$t_{INHBIDIR}$	0.0						ns
$t_{OUTCOBIDIR}$	2.0	5.0					ns
$t_{XZBIDIR}$		7.1					ns
$t_{ZXBIDIR}$		7.1					ns
$t_{INSUBIDIRPLL}$	3.8						ns
$t_{INHBIDIRPLL}$	0.0						ns
$t_{OUTCOBIDIRPLL}$	0.5	2.1					ns
$t_{XZBIDIRPLL}$		4.2					ns
$t_{ZXBIDIRPLL}$		4.2					ns

Table 73. EP20K1500C f_{MAX} LE Timing Parameters Note (1)

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 76. EP20K1500C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.0						ns
t_{CL}	2.0						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.0						ns
t_{ESBCL}	2.0						ns
t_{ESBWP}	1.0						ns
t_{ESBRP}	0.8						ns

Table 77. EP20K1500C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.2						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 79. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade (1)		-9 Speed Grade (1)		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.1					ns
1.8 V		0.5					ns
PCI		0.4					ns
GTL+		–0.3					ns
SSTL-3 Class I		–0.4					ns
SSTL-3 Class II		–0.4					ns
SSTL-2 Class I		–0.3					ns
SSTL-2 Class II		–0.3					ns
LVDS		–0.2					ns
CTT		–0.3					ns
AGP		0.0					ns

Table 80. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grade (1)		-9 Speed Grade (1)		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.5					ns
1.8 V		1.7					ns
PCI		–0.2					ns
GTL+		–0.4					ns
SSTL-3 Class I		–0.1					ns
SSTL-3 Class II		–0.6					ns
SSTL-2 Class I		0.0					ns
SSTL-2 Class II		–0.4					ns
LVDS		–0.8					ns
CTT		–0.2					ns
AGP		–0.4					ns

Note to tables:
(1) Timing information will be released in a future version of this data sheet.