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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	189
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100cq240c7es

- Advanced interconnect structure
 - Copper interconnect for high performance
 - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
 - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
 - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions optimized for APEX 20KC architecture available
 - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
 - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
 - Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20KC QFP & BGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
EP20K100C	92	151	183	246	
EP20K200C		136	168	271	376
EP20K400C					488
EP20K600C					488
EP20K1000C					488
EP20K1500C					488

Table 4. APEX 20KC FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K100C	93	246			
EP20K200C			376	376	
EP20K400C				488 (3)	
EP20K600C				508 (3)	588
EP20K1000C				508 (3)	708
EP20K1500C					808

Notes to tables:

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20KC device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 5. APEX 20KC QFP & BGA Package Sizes

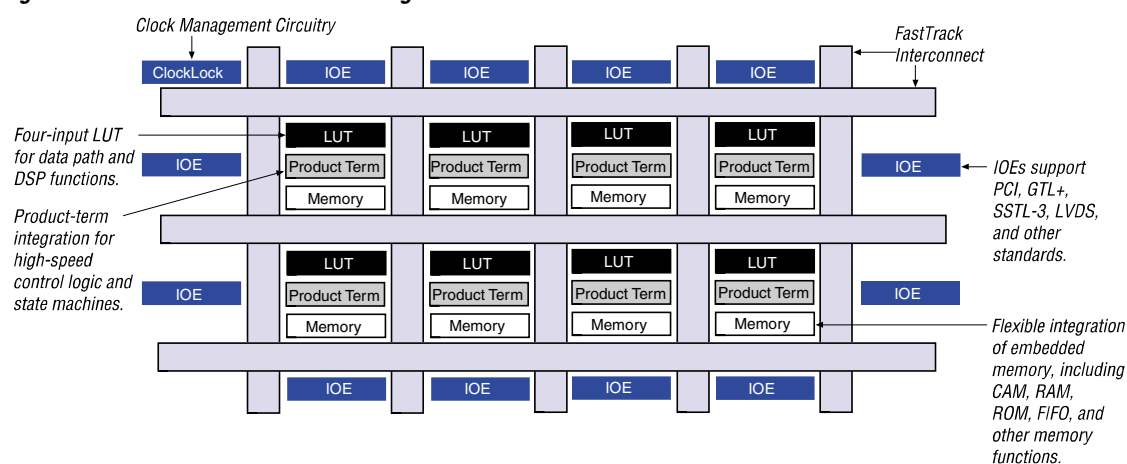
Feature	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27
Area (mm ²)	484	924	1,218	1,225	2,025
Length × Width (mm × mm)	22.0 × 22.0	30.4 × 30.4	34.9 × 34.9	35.0 × 35.0	45.0 × 45.0

Table 6. APEX 20KC FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm ²)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

Figure 1. APEX 20KC Device Block Diagram



APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

LE Operating Modes

The APEX 20KC LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

Figure 12. APEX 20KC FastRow Interconnect

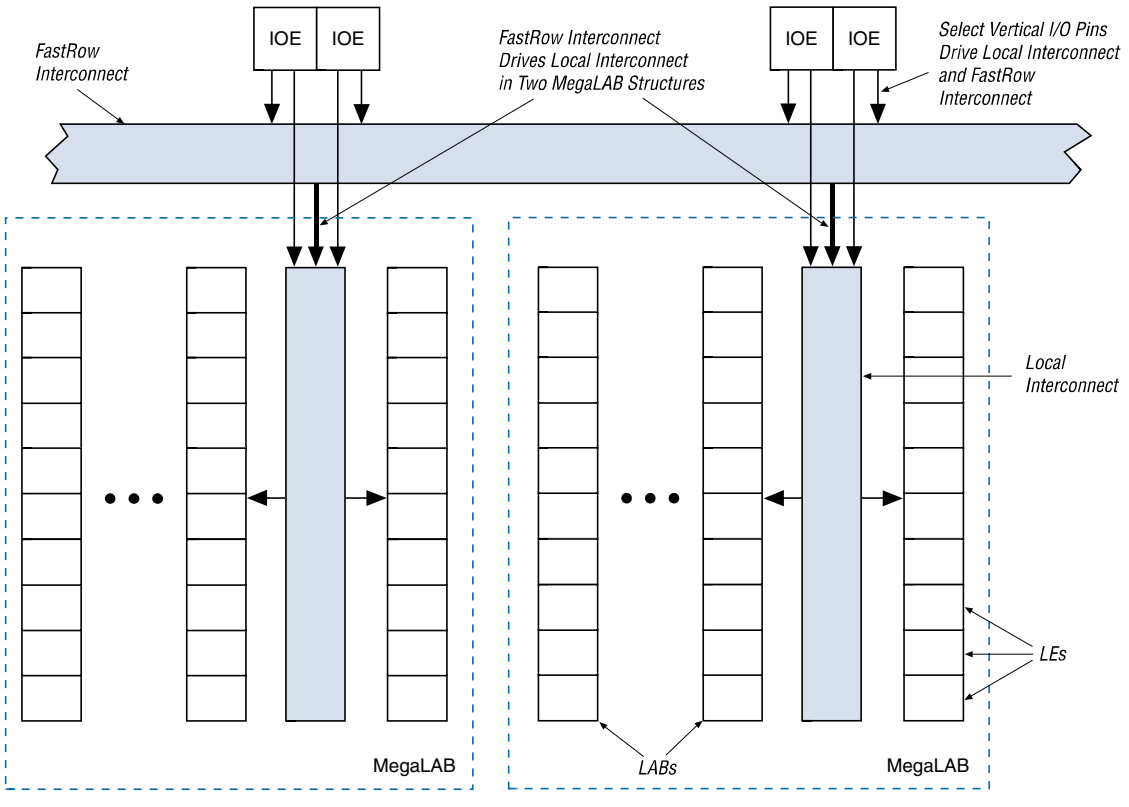
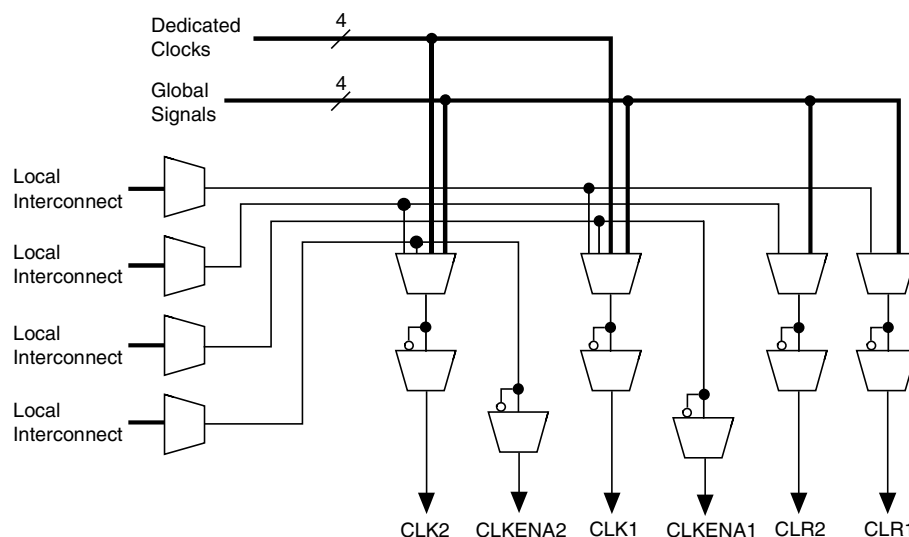


Table 8 summarizes how various elements of the APEX 20KC architecture drive each other.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

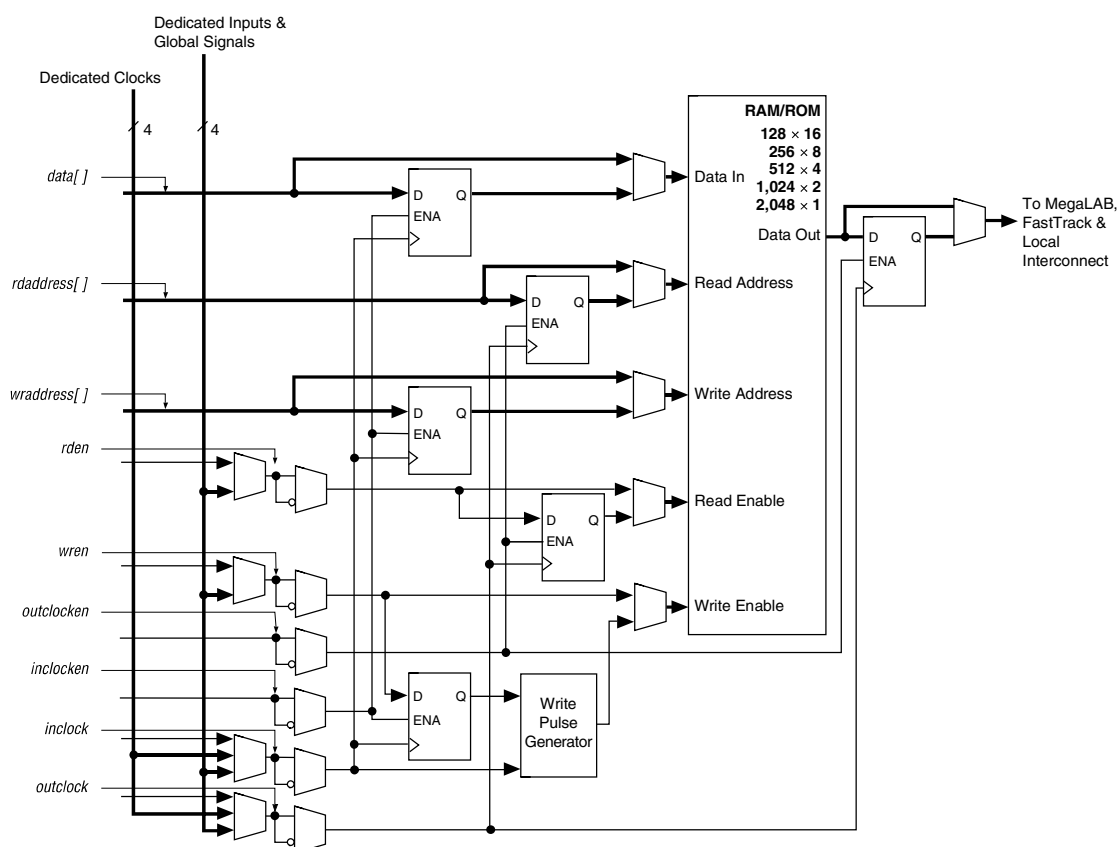
The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, **WE**, and write address. The other clock controls all registers associated with reading: read enable (**RE**), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies.

Figure 20 shows the ESB in read/write clock mode.

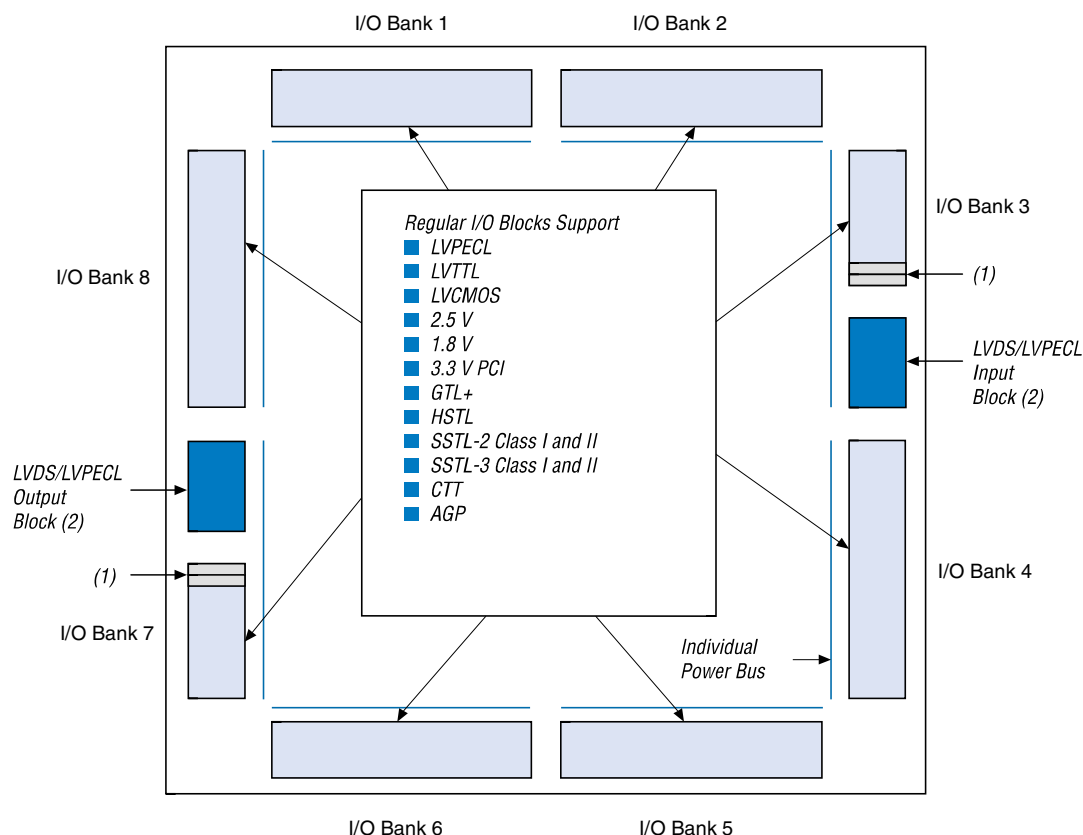
Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Note:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

Figure 28. APEX 20KC I/O Banks

**Notes:**

- (1) Any I/O pin within two pads of the LVDS pins can only be used as an input to maintain an acceptable noise level on the V_{CCIO} plane. No output pin can be placed within two pads of LVDS pins unless separated by a power or ground pin. Use the **Show Pads** view in the Quartus II software's Floor Plan Editor to locate these pads. The Quartus II software will give an error message for illegal output or bidirectional pin placement next to the LVDS pin.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20KC devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V VCCINT level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support								
V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ (1)	✓ (1)		✓			
2.5		✓	✓ (1)			✓		
3.3		✓	✓	✓ (2)		✓ (3)	✓	✓

Notes:

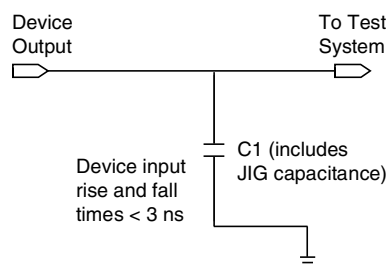
- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.
- (2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor.
- (3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Generic Testing

Each APEX 20KC device is functionally tested. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20KC devices are made under conditions equivalent to those shown in Figure 31. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Figure 31. APEX 20KC AC Test Conditions



Operating Conditions

Tables 17 through 20 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KC devices.

Table 17. APEX 20KC Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground (2)	-0.5	2.5	V
V_{CCIO}			-0.5	4.6	V
V_I	DC input voltage		-0.5	4.6	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

Table 20. APEX 20KC Device Capacitance *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance on dedicated clock pin	V _{IN} = 0 V, f = 1.0 MHz		12	pF
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (6) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
- (7) These values are specified under the APEX 20KC device recommended operating conditions, shown in [Table 18 on page 53](#).
- (8) This value is specified for normal device operation. The value may vary during power-up.
- (9) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
- (10) Capacitance is sample-tested only.

Tables 21 through 36 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

Table 21. LVTTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V _{CCIO}	Output supply voltage		3.0	3.6	V
V _{IH}	High-level input voltage		2.0	V _{CCIO} + 0.3	V
V _{IL}	Low-level input voltage		–0.3	0.8	V
I _I	Input pin leakage current	V _{IN} = 0 V or 3.3 V	–10	10	μA
V _{OH}	High-level output voltage	I _{OH} = –12 mA, V _{CCIO} = 3.0 V (1)	2.4		V
V _{OL}	Low-level output voltage	I _{OL} = 12 mA, V _{CCIO} = 3.0 V (2)		0.4	V

Table 28. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		$V_{REF} + 0.1$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.1$	V
V_{OL}	Low-level output voltage	$I_{OL} = 36 \text{ mA}$ (2)			0.65	V

Table 29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		$V_{REF} + 0.18$		$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		$V_{REF} - 0.18$	V
V_{OH}	High-level output voltage	$I_{OH} = -7.6 \text{ mA}$ (1)	$V_{TT} + 0.57$			V
V_{OL}	Low-level output voltage	$I_{OL} = 7.6 \text{ mA}$ (2)			$V_{TT} - 0.57$	V

Figure 33 shows the f_{MAX} timing model for APEX 20KC devices.

Figure 33. f_{MAX} Timing Model

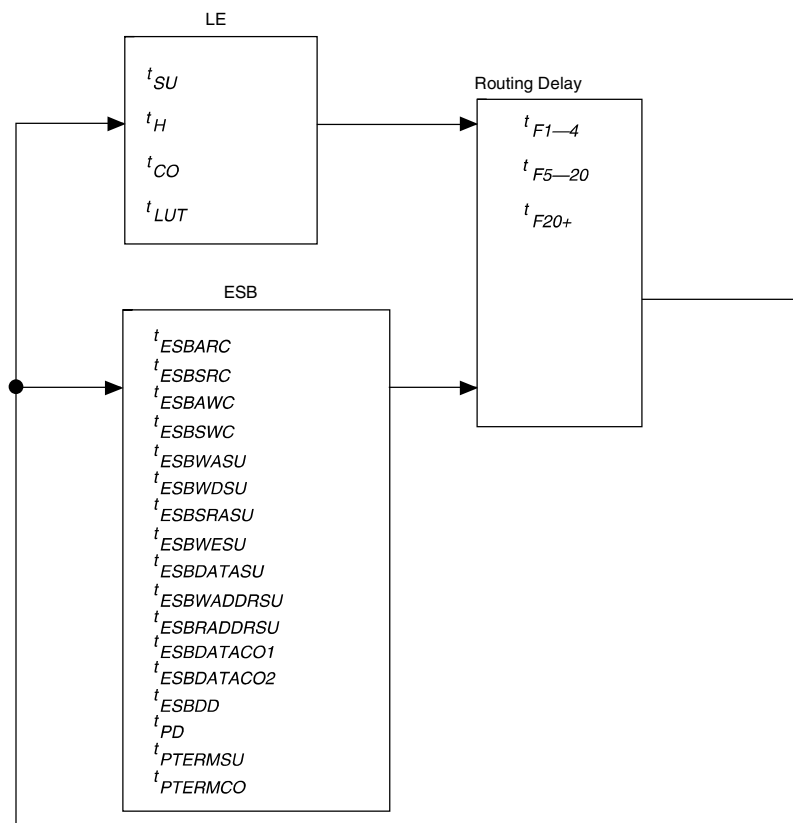


Figure 34 shows the timing model for bidirectional I/O pin timing.

Table 42. APEX 20KC External Bidirectional Timing Parameters *Note (1)*

Symbol	Parameter	Condition
$t_{\text{INSUBIDIR}}$	Setup time for bidirectional pins with global clock at LAB-adjacent input register	
t_{INHBIDIR}	Hold time for bidirectional pins with global clock at LAB-adjacent input register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
t_{XZBIDIR}	Synchronous output enable register to output buffer disable delay	C1 = 35 pF
t_{ZXBIDIR}	Synchronous output enable register to output buffer enable delay	C1 = 35 pF
$t_{\text{INSUBIDIRPLL}}$	Setup time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{\text{INHBIDIRPLL}}$	Hold time for bidirectional pins with PLL clock at LAB-adjacent input register	
$t_{\text{OUTCOBIDIRPLL}}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE register	C1 = 35 pF
$t_{\text{XZBIDIRPLL}}$	Synchronous output enable register to output buffer disable delay with PLL	C1 = 35 pF
$t_{\text{ZXBIDIRPLL}}$	Synchronous output enable register to output buffer enable delay with PLL	C1 = 35 pF

Note to tables:

(1) These timing parameters are sample-tested only.

Table 48. EP20K100C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	1.9						ns
t_{INHBIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.9						ns
$t_{\text{INHBIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 49. EP20K200C t_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.7					ns

Table 58. EP20K400C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.0						ns
t_{CL}	2.0						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.0						ns
t_{ESBCL}	2.0						ns
t_{ESBWP}	1.0						ns
t_{ESBRP}	0.8						ns

Table 59. EP20K400C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.2						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 60. EP20K400C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.4						ns
t_{INHIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.8						ns
$t_{\text{INHIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 61. EP20K600C t_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.7					ns

Table 66. EP20K600C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.4						ns
t_{INHBIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.9						ns
$t_{\text{INHBIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 67. EP20K1000C f_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 78. EP20K1500C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade ⁽²⁾		-9 Speed Grade ⁽²⁾		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	2.6						ns
t _{INHBIDIR}	0.0						ns
t _{OUTCOBIDIR}	2.0	5.0					ns
t _{XZBIDIR}		7.1					ns
t _{ZXBIDIR}		7.1					ns
t _{INSUBIDIRPLL}	3.9						ns
t _{INHBIDIRPLL}	0.0						ns
t _{OUTCOBIDIRPLL}	0.5	2.1					ns
t _{XZBIDIRPLL}		4.2					ns
t _{ZXBIDIRPLL}		4.2					ns

Notes to tables:

- (1) Timing information is preliminary. Final timing information will be released in a future version of this data sheet.
 (2) Timing information for these devices will be released in a future version of this data sheet.

Tables 79 and 80 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Table 79. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade ⁽¹⁾		-9 Speed Grade ⁽¹⁾		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.1					ns
1.8 V		0.5					ns
PCI		0.4					ns
GTL+		−0.3					ns
SSTL-3 Class I		−0.4					ns
SSTL-3 Class II		−0.4					ns
SSTL-2 Class I		−0.3					ns
SSTL-2 Class II		−0.3					ns
LVDS		−0.2					ns
CTT		−0.3					ns
AGP		0.0					ns

Table 80. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grade ⁽¹⁾		-9 Speed Grade ⁽¹⁾		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.5					ns
1.8 V		1.7					ns
PCI		−0.2					ns
GTL+		−0.4					ns
SSTL-3 Class I		−0.1					ns
SSTL-3 Class II		−0.6					ns
SSTL-2 Class I		0.0					ns
SSTL-2 Class II		−0.4					ns
LVDS		−0.8					ns
CTT		−0.2					ns
AGP		−0.4					ns

Note to tables:

(1) Timing information will be released in a future version of this data sheet.