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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	189
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100cq240c8

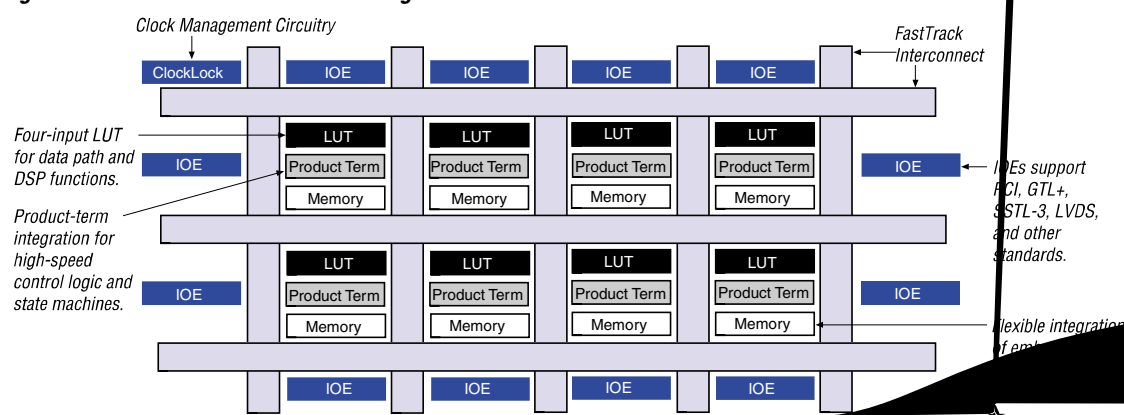
- Advanced interconnect structure
 - Copper interconnect for high performance
 - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
 - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
 - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions optimized for APEX 20KC architecture available
 - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
 - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
 - Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20KC QFP & BGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
EP20K100C	92	151	183	246	
EP20K200C		136	168	271	376
EP20K400C					488
EP20K600C					488
EP20K1000C					488
EP20K1500C					488

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs allows APEX 20KC devices to implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. Additionally, designers can use the ESBs to create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20KC device.

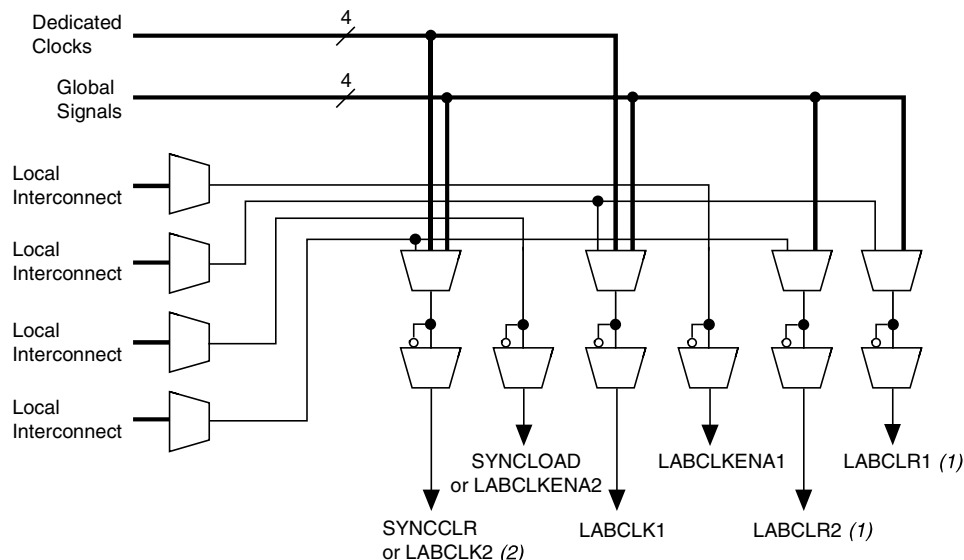
Figure 1. APEX 20KC Device Block Diagram



APEX 20KC devices provide four dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals, which use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20KC devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



Notes:

- (1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
- (2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE, the smallest unit of logic in the APEX 20KC architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Cascade Chain

With the cascade chain, the APEX 20KC architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20KC Cascade Chain

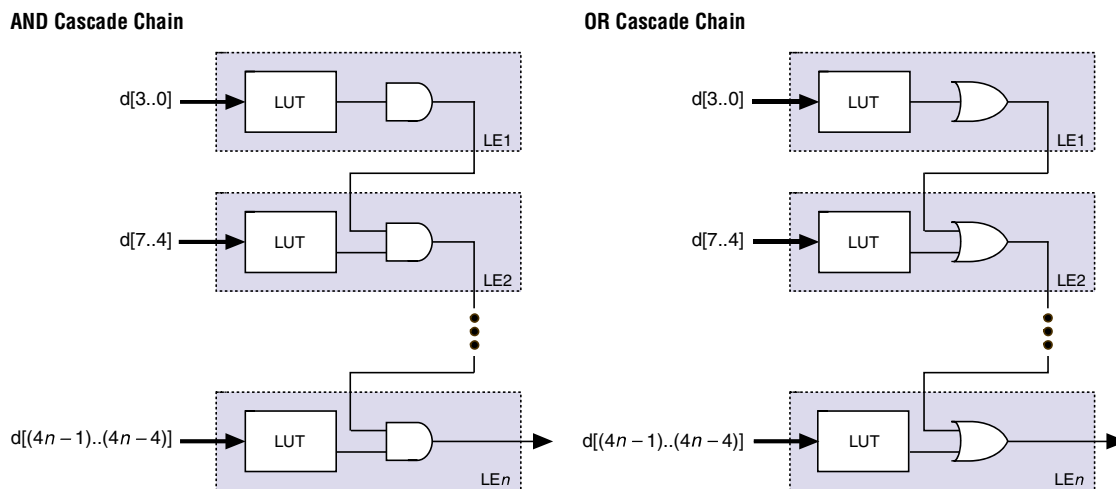
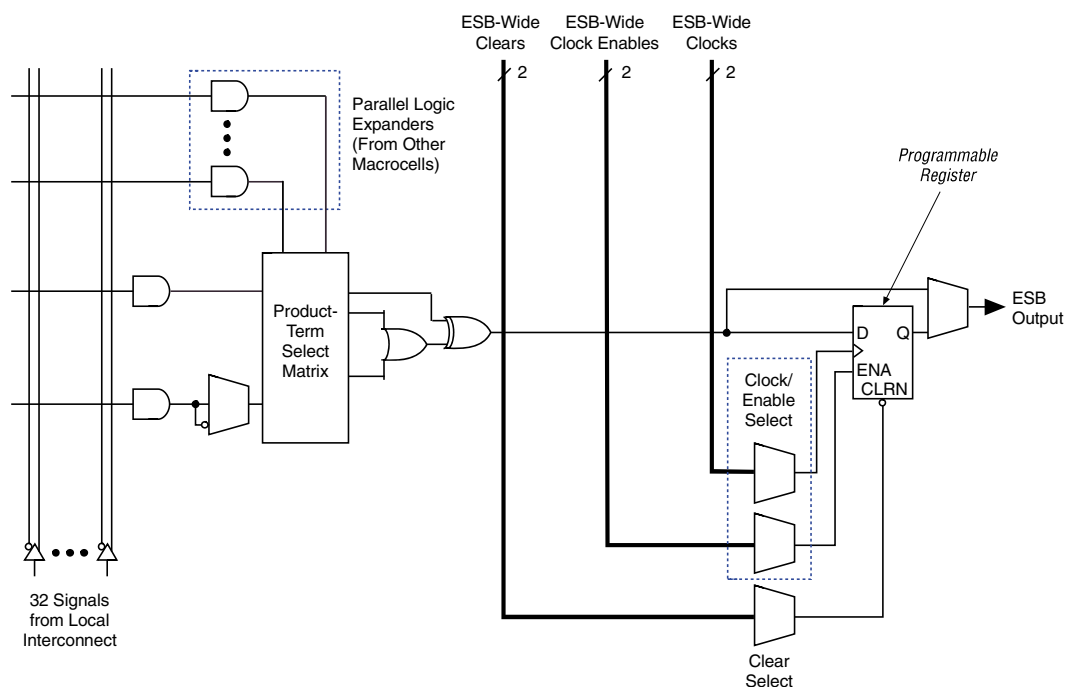


Figure 14. APEX 20KC Macrocell

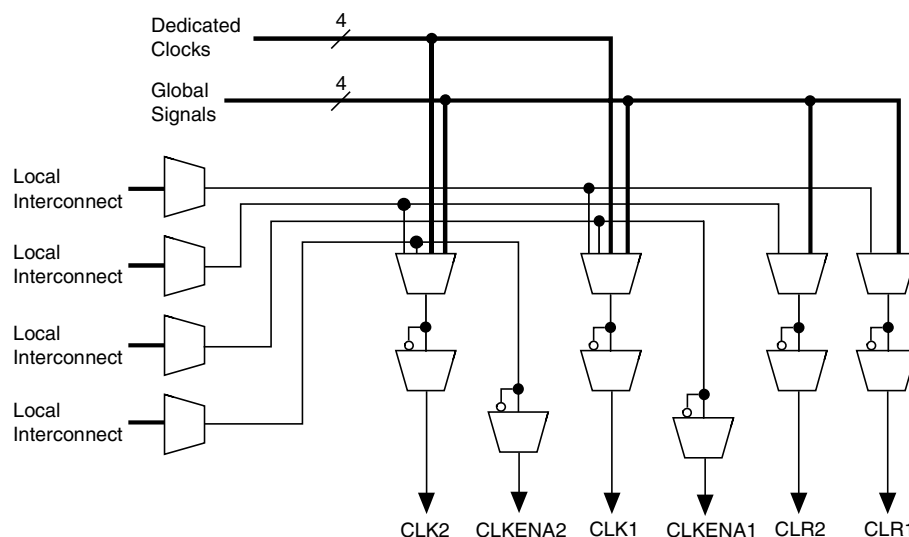
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinational operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

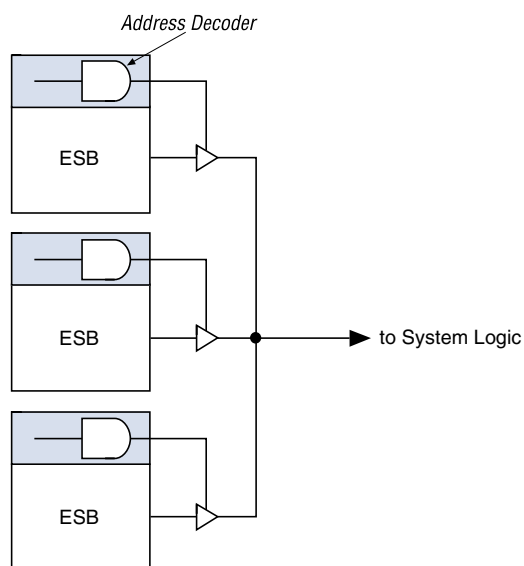
Figure 15. ESB Product-Term Mode Control Logic



Parallel Expanders

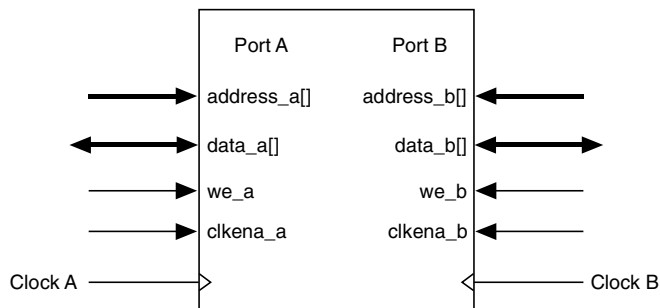
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.

Figure 18. Deep Memory Block Implemented with Multiple ESBs

The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two ESBs are used to support two simultaneous reads or writes.

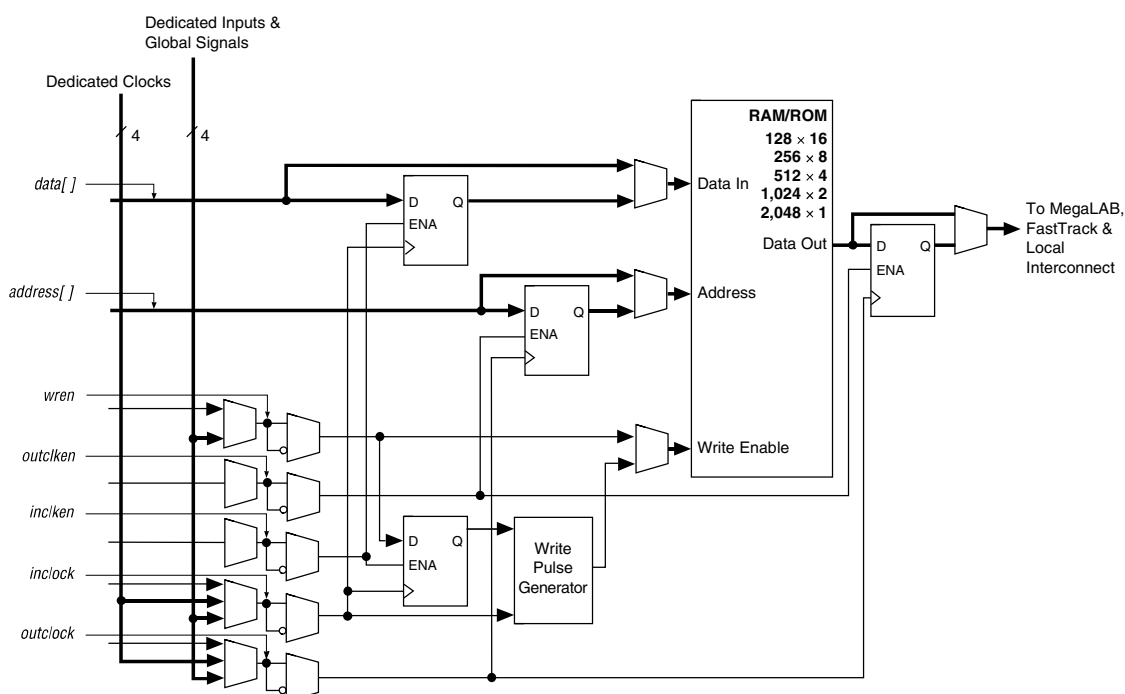
The ESB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in [Figure 19](#).

Figure 19. APEX 20KC ESB Implementing Dual-Port RAM

Single-Port Mode

The APEX 20KC ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



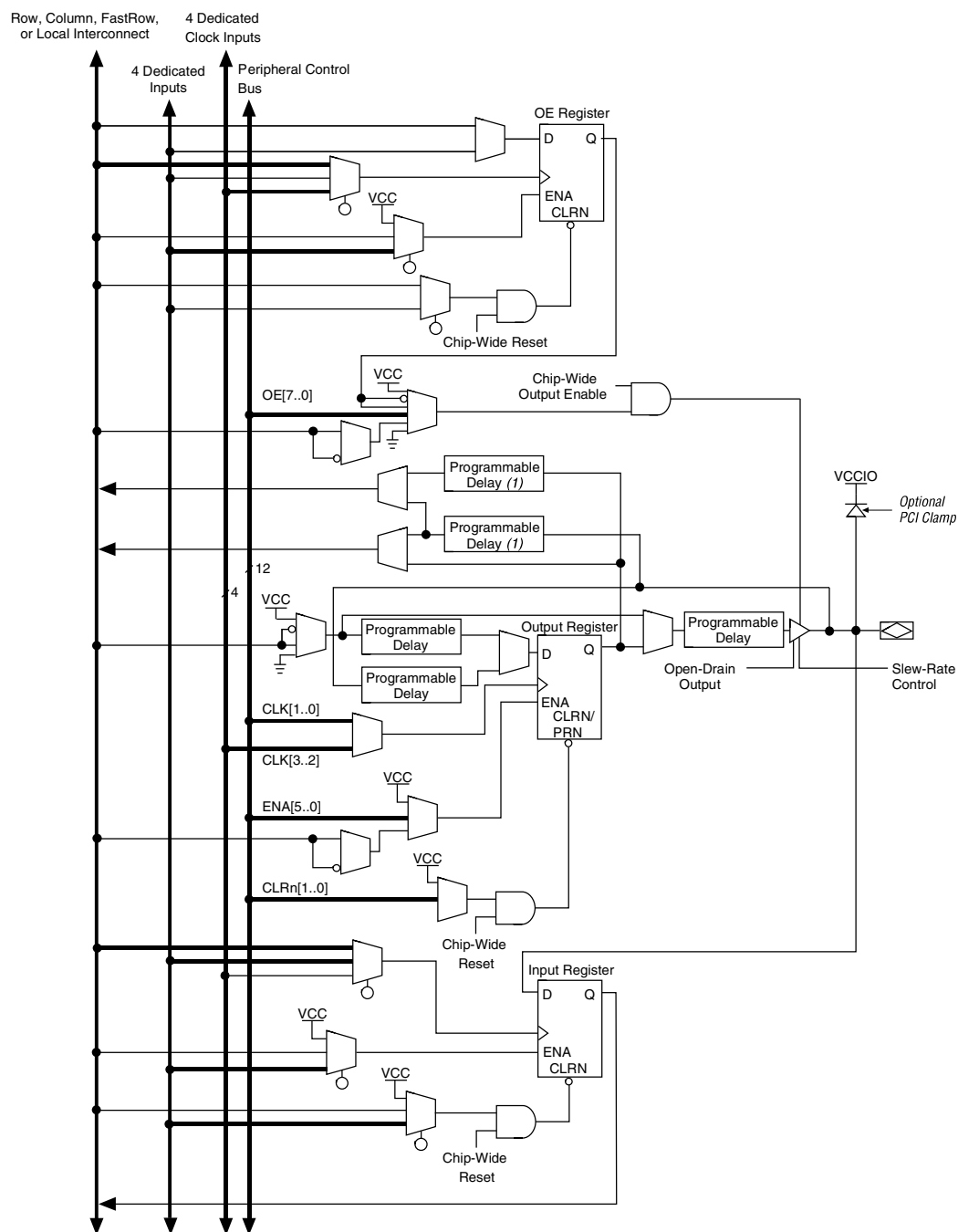
Note:

- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

Content-Addressable Memory

In APEX 20KC devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Figure 25. APEX 20KC Bidirectional I/O Registers *Notes (1), (2)***Notes:**

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CCINT} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC V_{CCINT} pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The V_{CCIO} pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the V_{CCIO} pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When V_{CCIO} pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When V_{CCIO} pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support								
V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ (1)	✓ (1)		✓			
2.5		✓	✓ (1)			✓		
3.3		✓	✓	✓ (2)		✓ (3)	✓	✓

Notes:

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO} , except for the 5.0-V input case.
- (2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor.
- (3) When $V_{CCIO} = 3.3$ V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Table 18. APEX 20KC Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V _I	Input voltage	(2), (5)	−0.5	4.1	V
V _O	Output voltage		0	V _{CCIO}	V
T _J	Junction temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
t _R	Input rise time (10% to 90%)			40	ns
t _F	Input fall time (90% to 10%)			40	ns

Table 19. APEX 20KC Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _I	Input pin leakage current (8)	V _I = 4.1 to −0.5 V	−10		10	μA
I _{OZ}	Tri-stated I/O pin leakage current (8)	V _O = 4.1 to −0.5 V	−10		10	μA
I _{CC0}	V _{CC} supply current (standby) (All ESBs in power-down mode)	V _I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V _I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R _{CONF}	Value of I/O pin pull-up resistor before and during configuration	V _{CCIO} = 3.0 V (9)	20		50	kΩ
		V _{CCIO} = 2.375 V (9)	30		80	kΩ
		V _{CCIO} = 1.71 V (9)	60		150	kΩ



DC Operating Specifications on APEX 20KC I/O standards are listed in Tables 21 to 36.

Table 20. APEX 20KC Device Capacitance *Note (10)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V . During transitions, the inputs may undershoot to -0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms , and V_{CC} must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (6) Typical values are for $T_A = 25^\circ\text{C}$, $V_{CCINT} = 1.8\text{ V}$, and $V_{CCIO} = 1.8\text{ V}$, 2.5 V or 3.3 V .
- (7) These values are specified under the APEX 20KC device recommended operating conditions, shown in [Table 18 on page 53](#).
- (8) This value is specified for normal device operation. The value may vary during power-up.
- (9) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO} .
- (10) Capacitance is sample-tested only.

Tables 21 through 36 list the DC operating specifications for the supported I/O standards. These tables list minimal specifications only; APEX 20KC devices may exceed these specifications.

Table 21. LVTTTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		2.0	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_I	Input pin leakage current	$V_{IN} = 0\text{ V}$ or 3.3 V	-10	10	μA
V_{OH}	High-level output voltage	$I_{OH} = -12\text{ mA}$, $V_{CCIO} = 3.0\text{ V}$ (1)	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 12\text{ mA}$, $V_{CCIO} = 3.0\text{ V}$ (2)		0.4	V

Tables 43 through 78 show the f_{MAX} and external timing parameters for EPC20K100C, EPC20K200C, EP20K400C, EP20K600C, EP20K1000C, and EP20K1500C devices.

Table 43. EP20K100C f_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_H	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.7					ns

Table 44. EP20K100C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.4					ns
t_{ESBSRC}		2.5					ns
t_{ESBAWC}		3.1					ns
t_{ESBSWC}		3.0					ns
$t_{ESBWASU}$	0.5						ns
t_{ESBWAH}	0.5						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.5						ns
$t_{ESBRASU}$	1.4						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.3						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.2						ns
$t_{ESBRADDRSU}$	0.2						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.3					ns
t_{ESBDD}		2.7					ns
t_{PD}		1.6					ns
$t_{PTERMSU}$	1.0						ns
$t_{PTERMCO}$		1.0					ns

Table 54. EP20K200C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.0						ns
t_{INHBIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.9						ns
$t_{\text{INHBIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 55. EP20K400C t_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 60. EP20K400C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.4						ns
t_{INHBIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.8						ns
$t_{\text{INHBIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 61. EP20K600C t_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.7					ns

Table 70. EP20K1000C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.0						ns
t_{CL}	2.0						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.0						ns
t_{ESBCL}	2.0						ns
t_{ESBWP}	1.0						ns
t_{ESBRP}	0.8						ns

Table 71. EP20K1000C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.2						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 72. EP20K1000C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.4						ns
t_{INHBIDIR}	0.0						ns
$t_{\text{OUTCOBIDIR}}$	2.0	5.0					ns
t_{XZBIDIR}		7.1					ns
t_{ZXBIDIR}		7.1					ns
$t_{\text{INSUBIDIRPLL}}$	3.8						ns
$t_{\text{INHBIDIRPLL}}$	0.0						ns
$t_{\text{OUTCOBIDIRPLL}}$	0.5	2.1					ns
$t_{\text{XZBIDIRPLL}}$		4.2					ns
$t_{\text{ZXBIDIRPLL}}$		4.2					ns

Table 73. EP20K1500C f_{MAX} LE Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 78. EP20K1500C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade ⁽²⁾		-9 Speed Grade ⁽²⁾		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	2.6						ns
t _{INHBIDIR}	0.0						ns
t _{OUTCOBIDIR}	2.0	5.0					ns
t _{XZBIDIR}		7.1					ns
t _{ZXBIDIR}		7.1					ns
t _{INSUBIDIRPLL}	3.9						ns
t _{INHBIDIRPLL}	0.0						ns
t _{OUTCOBIDIRPLL}	0.5	2.1					ns
t _{XZBIDIRPLL}		4.2					ns
t _{ZXBIDIRPLL}		4.2					ns

Notes to tables:

- (1) Timing information is preliminary. Final timing information will be released in a future version of this data sheet.
 (2) Timing information for these devices will be released in a future version of this data sheet.

Tables 79 and 80 show selectable I/O standard input and output delays for APEX 20KC devices. If you select an I/O standard input or output delay other than LVCMOS, add the delay for the selected speed grade to the LVCMOS value.

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at <http://www.altera.com>.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20KC devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20KC device can be loaded with one of five configuration schemes (see Table 81), chosen on the basis of the target application. An EPC16, EPC2, or EPC1 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20KC device. When a configuration device is used, the system can configure automatically at system power-up.



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