Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

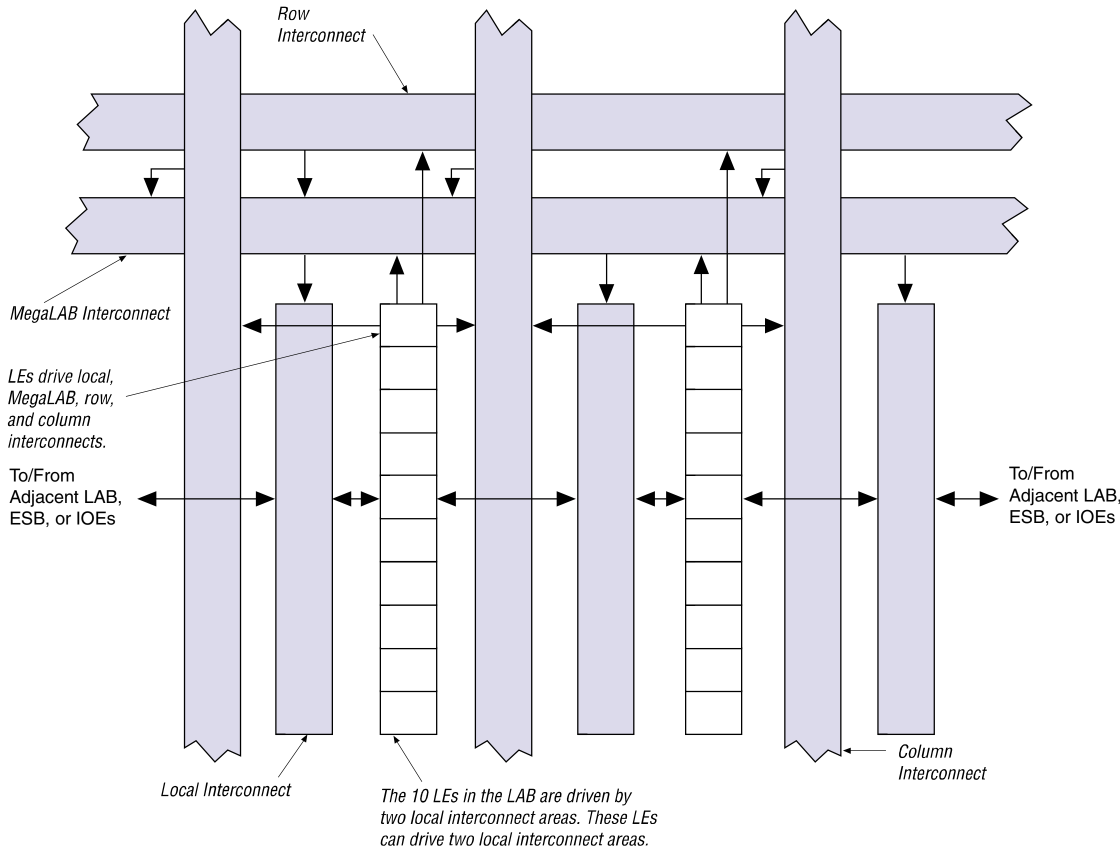
Details	
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	189
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100cq240c8es

- Advanced interconnect structure
  - Copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX 20KC architecture available
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
  - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
  - Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20KC QFP &BGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
EP20K100C	92	151	183	246	
EP20K200C		136	168	271	376
EP20K400C					488
EP20K600C					488
EP20K1000C					488
EP20K1500C					488

Figure 3. LAB Structure



Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

Figure 6. APEX 20KC Carry Chain

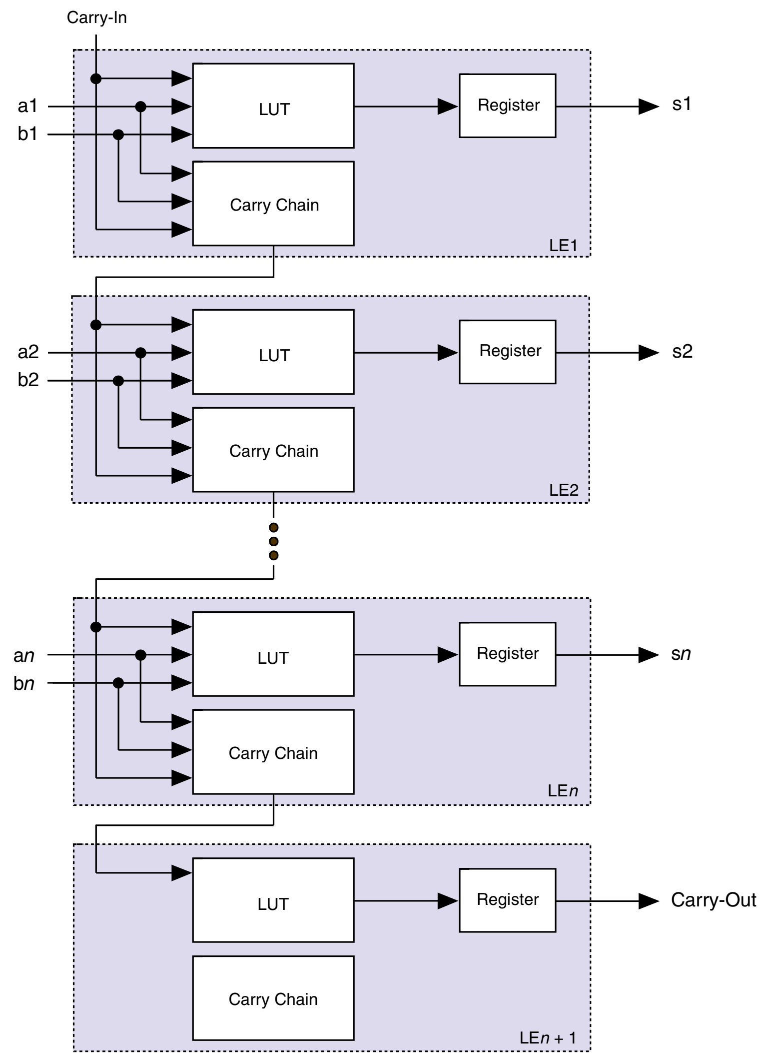
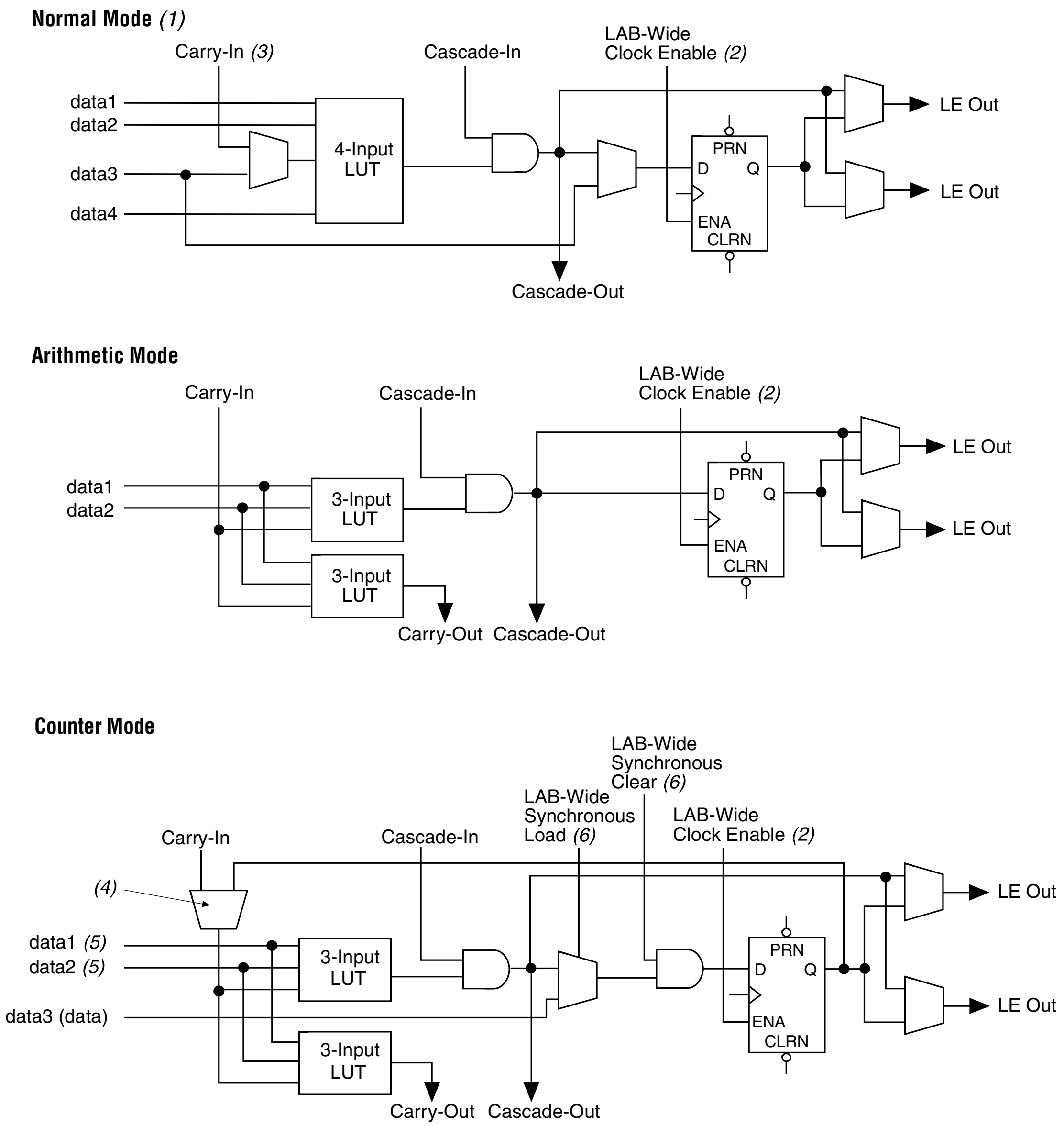


Figure 8. APEX 20KC LE Operating Modes



Notes:

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The `DATA1` and `DATA2` input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

The counter mode uses two 3-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset or to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

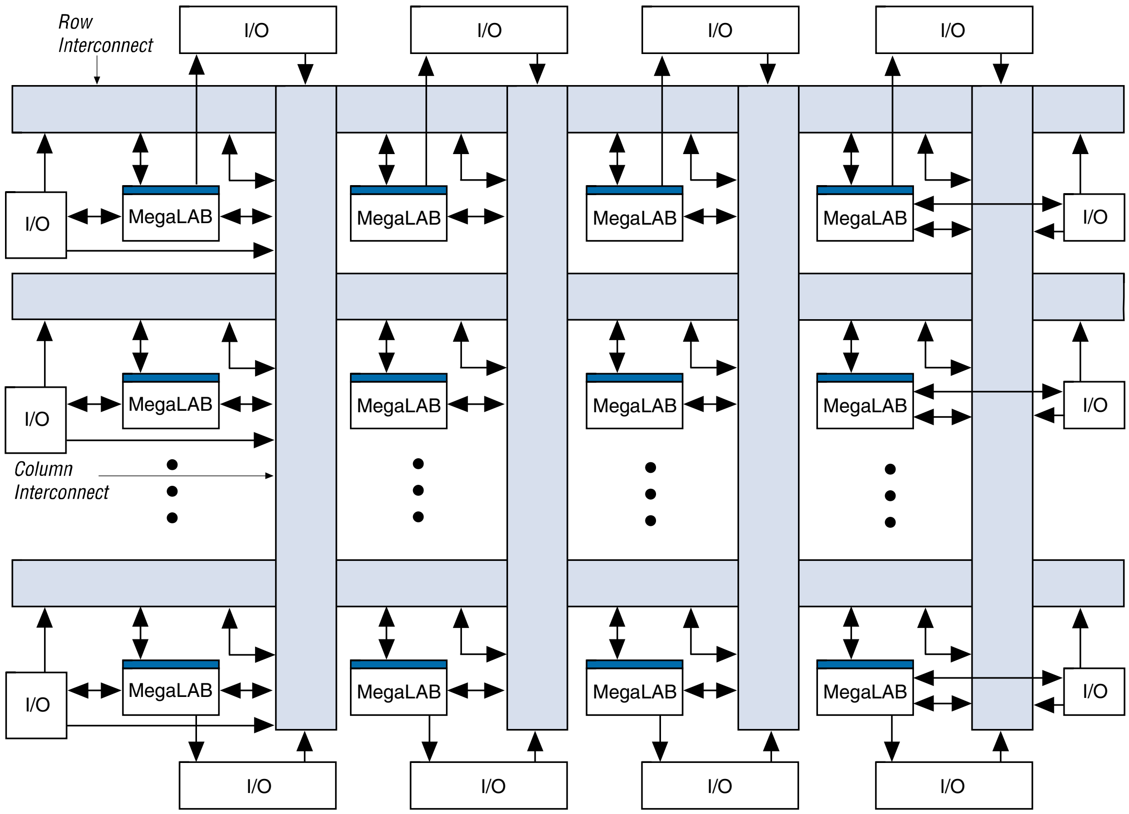
In addition to the two clear and preset modes, APEX 20KC devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20KC architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX 20KC Interconnect Structure

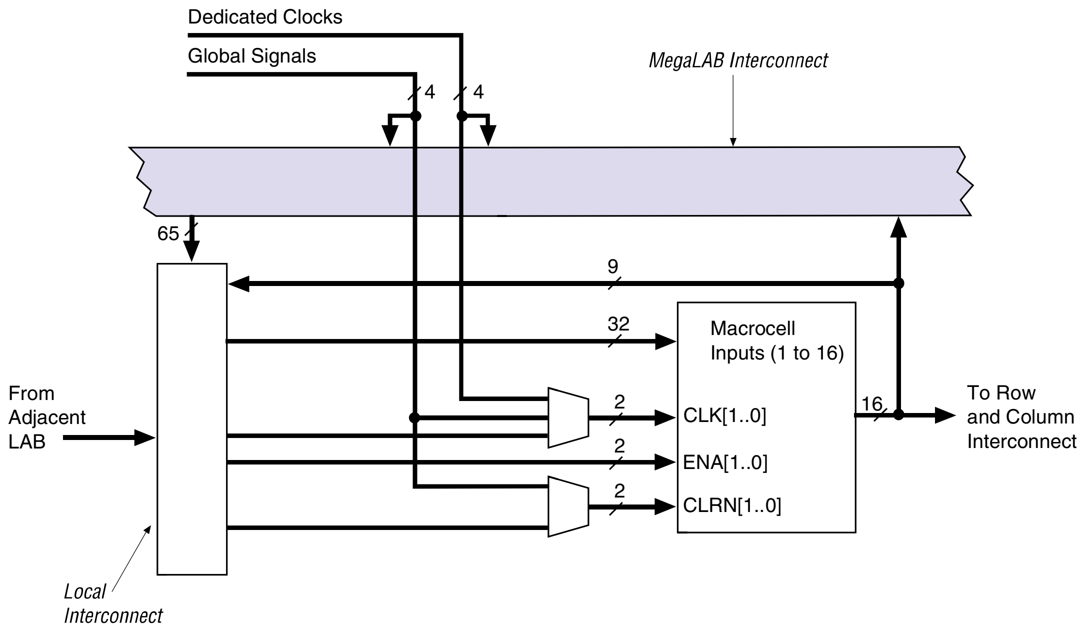


A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 13. Product-Term Logic in ESB

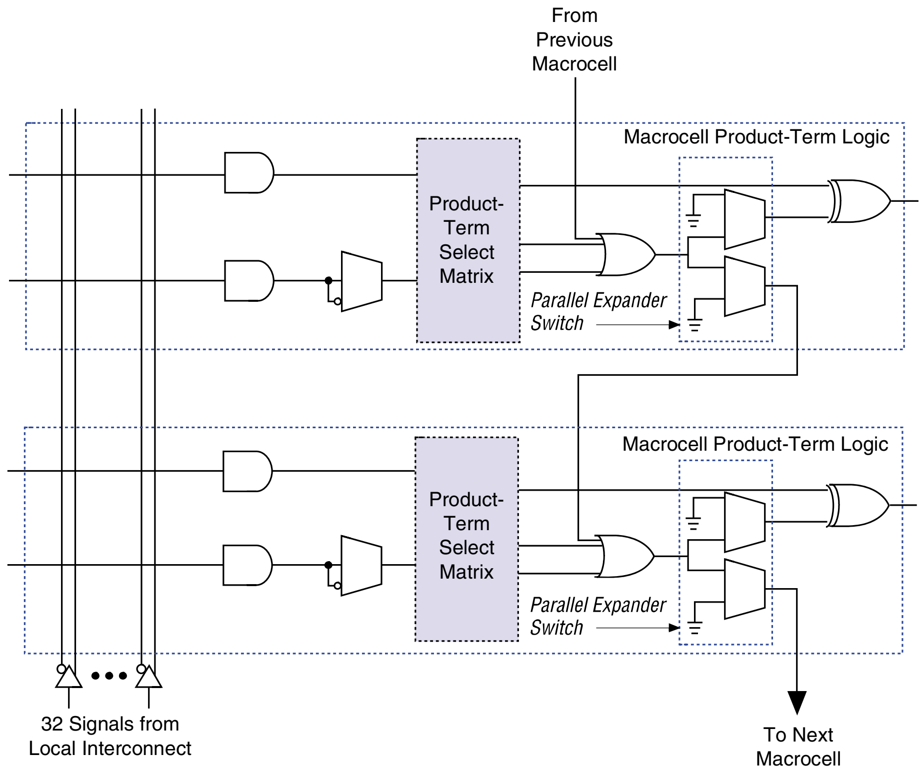


Macrocells

APEX 20KC macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform De Morgan's inversion for more efficient implementation of wide `OR` functions. The Quartus II Compiler can use a `NOT`-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20KC macrocell.

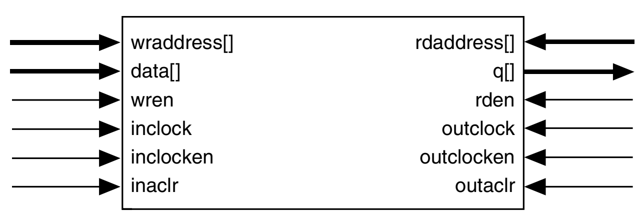
Figure 16. APEX 20KC Parallel Expanders



Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

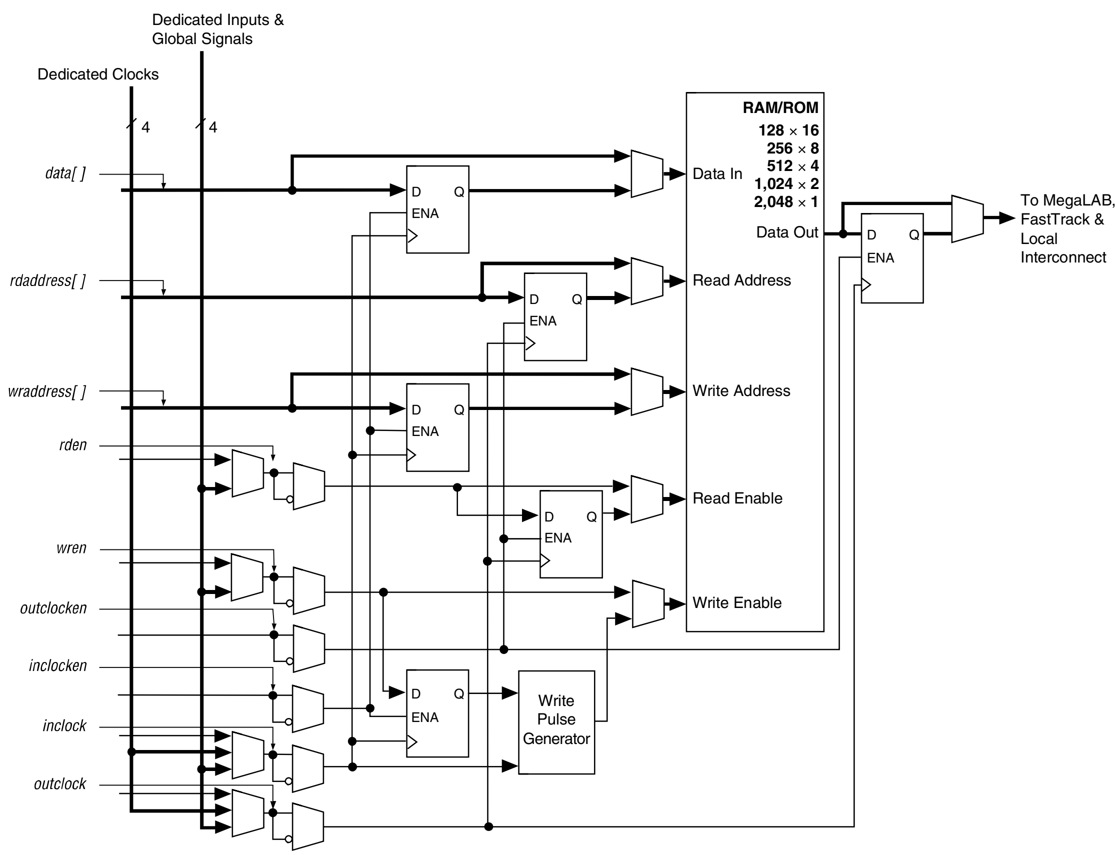
Figure 17. ESB Block Diagram



Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode Note (1)



Note:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20KC ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20KC device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20KC IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins.

APEX 20KC devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KC IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KC IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II Compiler sets these delays by default to minimize setup time while providing a zero hold time.

Advanced I/O Standard Support

APEX 20KC IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KC devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KC device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own `VCCIO` pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K400C and larger APEX 20KC devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K400C and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400C devices and larger add a serializer/deserializer circuit and PLL for support up to 840 Mbit per channel.

Each bank can support multiple standards with the same `VCCIO` for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same `VCCIO` voltage level. For example, when `VCCIO` is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used for the LVDS I/O standard, they support all of the other I/O standards. Figure 28 shows the arrangement of the APEX 20KC I/O banks.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ *(1)*	✓ *(1)*		✓			
2.5		✓	✓ *(1)*			✓		
3.3		✓	✓	✓ *(2)*		✓ *(3)*	✓	✓

Notes:
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.
(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor.
(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

The APEX 20KC device instruction register length is 10 bits. The APEX 20KC device USERCODE register length is 32 bits. Tables 14 and 15 show the boundary-scan register length and device IDCODE information for APEX 20KC devices.

Table 14. APEX 20KC Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K100C	774
EP20K200C	1,164
EP20K400C	1,506
EP20K600C	1,806
EP20K1000C	2,190
EP20K1500C	2,502

Table 15. 32-Bit APEX 20KC Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K100C	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K200C	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K400C	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600C	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000C	0000	1001 0000 0000 0000	000 0110 1110	1
EP20K1500C	0000	1001 0101 0000 0000	000 0110 1110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 30 shows the timing requirements for the JTAG signals.

Table 38. APEX 20KC f_{MAX} ESB Timing Parameters

Symbol	Parameter
t_{ESBARC}	ESB asynchronous read cycle time
t_{ESBSRC}	ESB synchronous read cycle time
t_{ESBAWC}	ESB asynchronous write cycle time
t_{ESBSWC}	ESB synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay

Table 39. APEX 20KC f_{MAX} Routing Delays

Symbol	Parameter
t_{F1-4}	Fan-out delay estimate using local interconnect
t_{F5-20}	Fan-out delay estimate using MegaLab interconnect
t_{F20+}	Fan-out delay estimate using FastTrack interconnect

Table 45. EP20K100C f_{MAX} Routing Delays *Note (1)*							
Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	1.0						ns

Table 46. EP20K100C Minimum Pulse Width Timing Parameters *Note (1)*							
Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.3						ns
t_{CL}	2.3						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.3						ns
t_{ESBCL}	2.3						ns
t_{ESBWP}	1.1						ns
t_{ESBRP}	0.9						ns

Table 47. EP20K100C External Timing Parameters							
Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.0						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.3						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 54. EP20K200C External Bidirectional Timing Parameters							
Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.0						ns
$t_{INHBIDIR}$	0.0						ns
$t_{OUTCOBIDIR}$	2.0	5.0					ns
$t_{XZBIDIR}$		7.1					ns
$t_{ZXBIDIR}$		7.1					ns
$t_{INSUBIDIRPLL}$	3.9						ns
$t_{INHBIDIRPLL}$	0.0						ns
$t_{OUTCOBIDIRPLL}$	0.5	2.1					ns
$t_{XZBIDIRPLL}$		4.2					ns
$t_{ZXBIDIRPLL}$		4.2					ns

Table 55. EP20K400C f_{MAX} LE Timing Parameters Note (1)							
Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 68. EP20K1000C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.5						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 69. EP20K1000C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	1.3						ns
t_{F20+}	2.6						ns

Table 74. EP20K1500C f_{MAX} ESB Timing Parameters Note (1)							
Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.3					ns
t_{ESBSRC}		2.3					ns
t_{ESBAWC}		2.9					ns
t_{ESBSWC}		2.7					ns
$t_{ESBWASU}$	0.4						ns
t_{ESBWAH}	0.4						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.4						ns
$t_{ESBRASU}$	1.3						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.0						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.1						ns
$t_{ESBRADDRSU}$	0.1						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.0					ns
t_{ESBDD}		2.4					ns
t_{PD}		1.4					ns
$t_{PTERMSU}$	0.9						ns
$t_{PTERMCO}$		1.0					ns

Table 75. EP20K1500C f_{MAX} Routing Delays Note (1)							
Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	1.4						ns
t_{F20+}	2.8						ns

Table 79. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade (1)		-9 Speed Grade (1)		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.1					ns
1.8 V		0.5					ns
PCI		0.4					ns
GTL+		–0.3					ns
SSTL-3 Class I		–0.4					ns
SSTL-3 Class II		–0.4					ns
SSTL-2 Class I		–0.3					ns
SSTL-2 Class II		–0.3					ns
LVDS		–0.2					ns
CTT		–0.3					ns
AGP		0.0					ns

Table 80. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grade (1)		-9 Speed Grade (1)		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.5					ns
1.8 V		1.7					ns
PCI		–0.2					ns
GTL+		–0.4					ns
SSTL-3 Class I		–0.1					ns
SSTL-3 Class II		–0.6					ns
SSTL-2 Class I		0.0					ns
SSTL-2 Class II		–0.4					ns
LVDS		–0.8					ns
CTT		–0.2					ns
AGP		–0.4					ns

Note to tables:

(1) Timing information will be released in a future version of this data sheet.

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20KC architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20KC devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20KC device can be loaded with one of five configuration schemes (see Table 81), chosen on the basis of the target application. An EPC16, EPC2, or EPC1 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20KC device. When a configuration device is used, the system can configure automatically at system power-up.