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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 416 |
| Number of Logic Elements/Cells | 4160 |
| Total RAM Bits | 53248 |
| Number of I/O | 93 |
| Number of Gates | 263000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k100ct144c7es |

- Advanced interconnect structure
  - Copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX 20KC architecture available
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
  - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
  - Supports popular revision-control software packages including PVCS, RCS, and SCCS

**Table 3. APEX 20KC QFP &BGA Package Options & I/O Count** *Notes (1), (2)*

| Device | 144-Pin TQFP | 208-Pin PQFP | 240-Pin PQFP | 356-Pin BGA | 652-Pin BGA |
|---|---|---|---|---|---|
| EP20K100C | 92 | 151 | 183 | 246 | |
| EP20K200C | | 136 | 168 | 271 | 376 |
| EP20K400C | | | | | 488 |
| EP20K600C | | | | | 488 |
| EP20K1000C | | | | | 488 |
| EP20K1500C | | | | | 488 |

**Table 4. APEX 20KC FineLine BGA Package Options & I/O Count** *Notes (1), (2)*

| Device | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| EP20K100C | 93 | 246 | | | |
| EP20K200C | | | 376 | 376 | |
| EP20K400C | | | | 488 *(3)* | |
| EP20K600C | | | | 508 *(3)* | 588 |
| EP20K1000C | | | | 508 *(3)* | 708 |
| EP20K1500C | | | | | 808 |

*Notes to tables:*

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20KC device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

**Table 5. APEX 20KC QFP & BGA Package Sizes**

| Feature | 144-Pin TQFP | 208-Pin PQFP | 240-Pin PQFP | 356-Pin BGA | 652-Pin BGA |
|---|---|---|---|---|---|
| Pitch (mm) | 0.50 | 0.50 | 0.50 | 1.27 | 1.27 |
| Area ($mm^2$) | 484 | 924 | 1,218 | 1,225 | 2,025 |
| Length × Width (mm × mm) | 22.0 × 22.0 | 30.4 × 30.4 | 34.9 × 34.9 | 35.0 × 35.0 | 45.0 × 45.0 |

**Table 6. APEX 20KC FineLine BGA Package Sizes**

| Feature | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 169 | 361 | 529 | 729 | 1,089 |
| Length × Width (mm × mm) | 13 × 13 | 19 × 19 | 23 × 23 | 27 × 27 | 33 × 33 |

## General Description

Similar to APEX 20K and APEX 20KE devices, APEX 20KC devices offer the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20KC architecture uniquely suited for SOPC designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20KC device.

APEX 20KC devices include additional features such as enhanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. Table 7 shows the features included in APEX 20KC devices.

**Table 7. APEX 20KC Device Features (Part 1 of 2)**

| Feature | APEX 20KC Devices |
|---|---|
| MultiCore system integration | Full support |
| Hot-socketing support | Full support |
| SignalTap logic analysis | Full support |
| 32-/64-bit, 33-MHz PCI | Full compliance |
| 32-/64-bit, 66-MHz PCI | Full compliance in -7 speed grade |
| MultiVolt I/O | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected bank by bank<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>$m/(n \times v)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift circuitry<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Eight |

After an APEX 20KC device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20KC devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20KC devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20KC architecture.

## Functional Description

APEX 20KC devices incorporate LUT-based logic, product-term-based logic, and memory into one device on an all-copper technology process. Signal interconnections within APEX 20KC devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KC devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The APEX 20KC architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

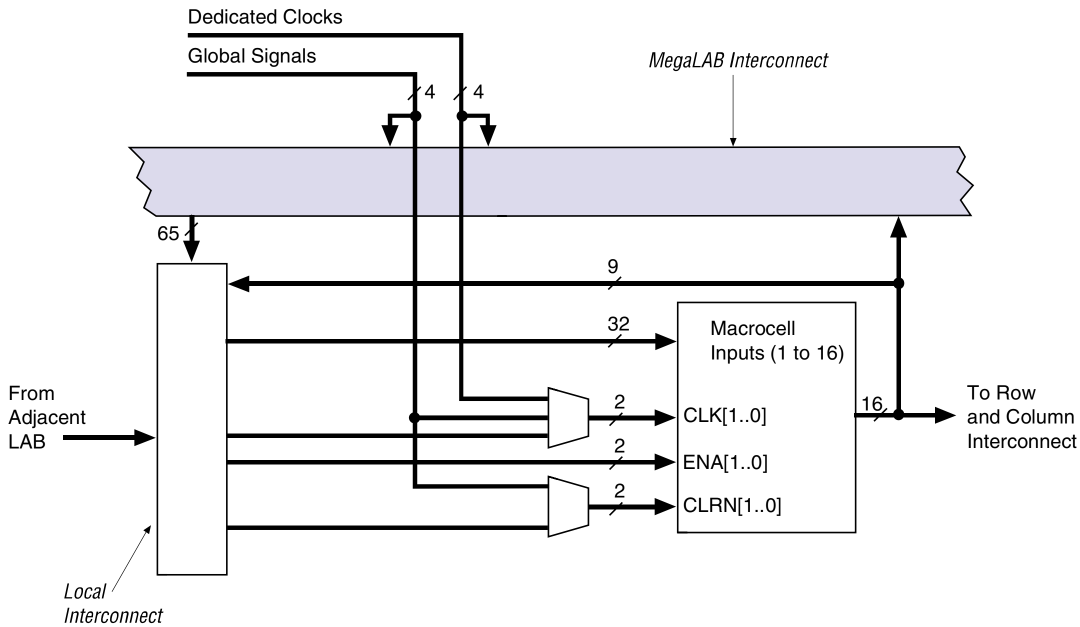
### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20KC architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than ten LEs by automatically linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an $n$-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

*Figure 13. Product-Term Logic in ESB*

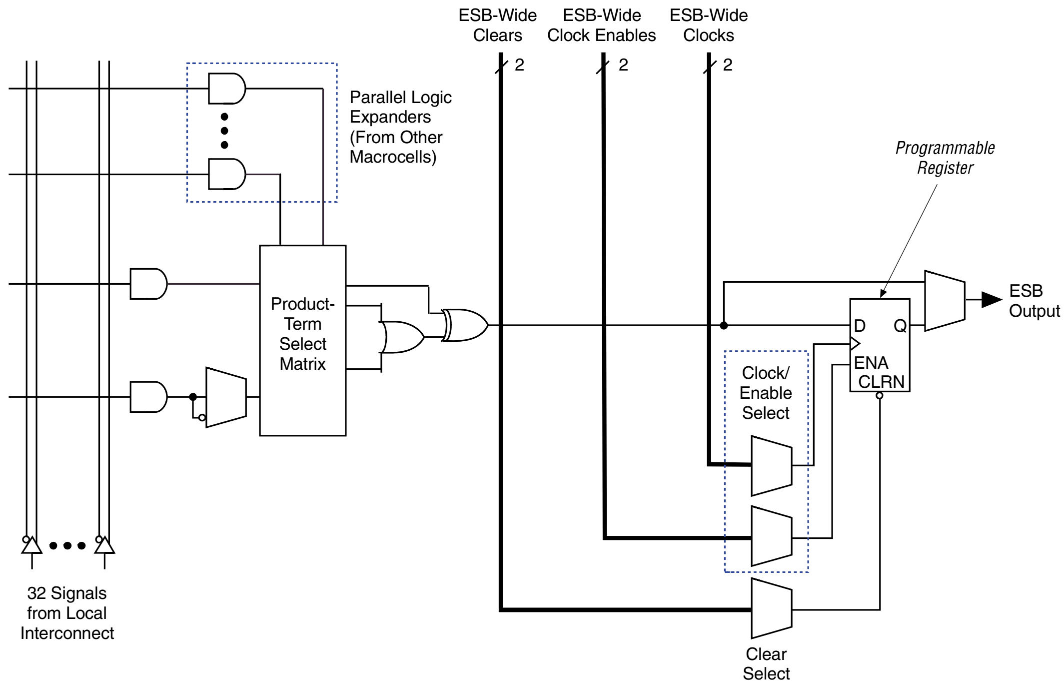



## *Macrocells*

APEX 20KC macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform De Morgan's inversion for more efficient implementation of wide `OR` functions. The Quartus II Compiler can use a `NOT`-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20KC macrocell.

*Figure 14. APEX 20KC Macrocell*




For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the FastTrack or MegaLAB interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the FastTrack and MegaLAB interconnects. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

The Quartus II Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20KC IOE offers one output enable per pin, the Quartus II Compiler can emulate open-drain operation efficiently.

The APEX 20KC IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 9 describes the APEX 20KC programmable delays and their logic options in the Quartus II software.

*Table 9. APEX 20KC Programmable Delay Chains*

| Programmable Delay | Quartus II Logic Option |
|---|---|
| Input pin to core delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input registers |
| Core to output register delay | Decrease input delay to output register |
| Output register $t_{CO}$ delay | Increase delay to output pin |
| Clock enable delay | Increase clock enable delay |

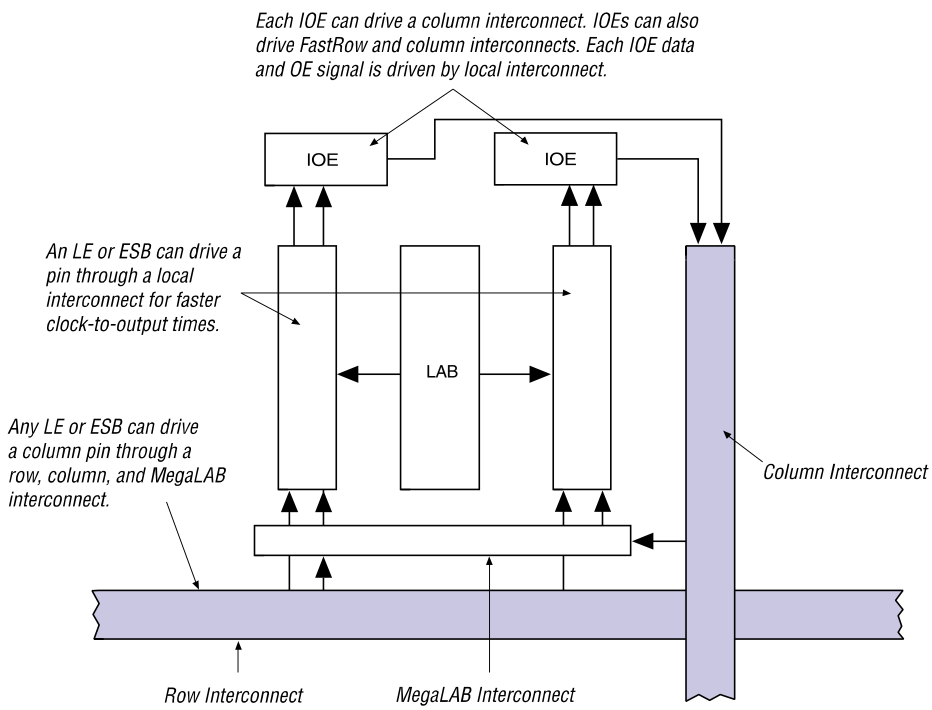
The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time.

The register in the APEX 20KC IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. This feature is useful for cases where the APEX 20KC device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 25 shows how fast bidirectional I/O pins are implemented in APEX 20KC devices. This feature is useful for cases where the APEX 20KC device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 27 shows how a column IOE connects to the interconnect.

*Figure 27. Column IOE Connection to the Interconnect*




## Dedicated Fast I/O Pins

APEX 20KC devices incorporate an enhancement to support bidirectional pins with high internal fan-out such as PCI control signals. These pins are called dedicated fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fan-out logic signal distribution. They also can drive out. The dedicated fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

The APEX 20KC device instruction register length is 10 bits. The APEX 20KC device USERCODE register length is 32 bits. Tables 14 and 15 show the boundary-scan register length and device IDCODE information for APEX 20KC devices.

**Table 14. APEX 20KC Boundary-Scan Register Length**

| Device | Boundary-Scan Register Length |
|---|---|
| EP20K100C | 774 |
| EP20K200C | 1,164 |
| EP20K400C | 1,506 |
| EP20K600C | 1,806 |
| EP20K1000C | 2,190 |
| EP20K1500C | 2,502 |

**Table 15. 32-Bit APEX 20KC Device IDCODE**

| Device | IDCODE (32 Bits) *(1)* | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | 1 (1 Bit) *(2)* |
| EP20K100C | 0000 | 1000 0001 0000 0000 | 000 0110 1110 | 1 |
| EP20K200C | 0000 | 1000 0010 0000 0000 | 000 0110 1110 | 1 |
| EP20K400C | 0000 | 1000 0100 0000 0000 | 000 0110 1110 | 1 |
| EP20K600C | 0000 | 1000 0110 0000 0000 | 000 0110 1110 | 1 |
| EP20K1000C | 0000 | 1001 0000 0000 0000 | 000 0110 1110 | 1 |
| EP20K1500C | 0000 | 1001 0101 0000 0000 | 000 0110 1110 | 1 |

*Notes:*
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 30 shows the timing requirements for the JTAG signals.

*Table 18. APEX 20KC Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 1.71 (1.71) | 1.89 (1.89) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(2)*, *(5)* | –0.5 | 4.1 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time (10% to 90%) | | | 40 | ns |
| $t_F$ | Input fall time (90% to 10%) | | | 40 | ns |

*Table 19. APEX 20KC Device DC Operating Conditions* *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current *(8)* | $V_I$ = 4.1 to –0.5 V | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current *(8)* | $V_O$ = 4.1 to –0.5 V | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -7 speed grade | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -8, -9 speed grades | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(9)* | 20 | | 50 | kΩ |
| | | $V_{CCIO}$ = 2.375 V *(9)* | 30 | | 80 | kΩ |
| | | $V_{CCIO}$ = 1.71 V *(9)* | 60 | | 150 | kΩ |

☞ DC Operating Specifications on APEX 20KC I/O standards are listed in Tables 21 to 36.

| *Table 32. SSTL-3 Class II Specifications* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Minimum** | **Typical** | **Maximum** | **Units** |
| $V_{CCIO}$ | I/O supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16 mA *(1)* | $V_{TT}$ + 0.8 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16 mA *(2)* | | | $V_{TT}$ – 0.8 | V |

| *Table 33. HSTL Class I I/O Specifications* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Minimum** | **Typical** | **Maximum** | **Units** |
| $V_{CCIO}$ | I/O supply voltage | | 1.71 | 1.8 | 1.89 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 0.68 | 0.75 | 0.90 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.1 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.1 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(1)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(2)* | | | 0.4 | V |

*Table 36. CTT I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}/V_{REF}$ *(3)* | Termination and reference voltage | | 1.35 | 1.5 | 1.65 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $I_I$ | Input pin leakage current | $0 < V_{IN} < V_{CCIO}$ | –10 | | 10 | μA |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –8 mA *(1)* | $V_{REF}$ + 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA *(2)* | | | $V_{REF}$ – 0.4 | V |
| $I_O$ | Output leakage current (when output is high Z) | $GND \leq V_{OUT} \leq V_{CCIO}$ | –10 | | 10 | μA |

***Notes to tables:***

(1) The $I_{OH}$ parameter refers to high-level output current.
(2) The $I_{OL}$ parameter refers to low-level output current. This parameter applies to open-drain pins as well as output pins.
(3) $V_{REF}$ specifies center point of switching range.

Figure 32 shows the output drive characteristics of APEX 20KC devices.

Figure 33 shows the $f_{MAX}$ timing model for APEX 20KC devices.

*Figure 33. $f_{MAX}$ Timing Model*

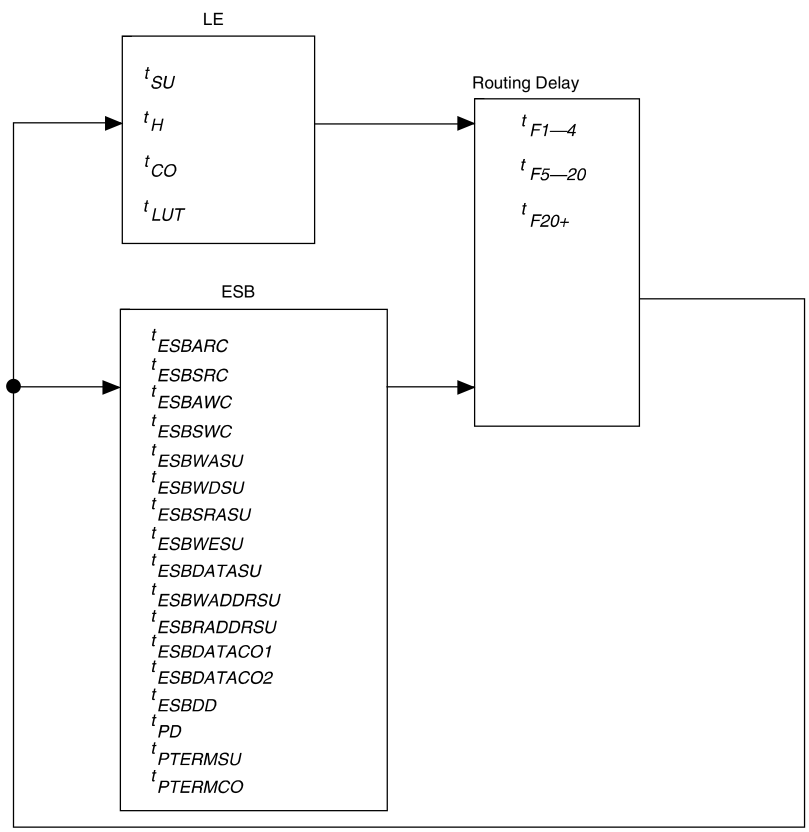



Figure 34 shows the timing model for bidirectional I/O pin timing.

| Table 40. APEX 20KC Minimum Pulse Width Timing Parameters | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

Tables 41 and 42 describe APEX 20KC external timing parameters.

| Table 41. APEX 20KC External Timing Parameters *Note (1)* | | |
|---|---|---|
| **Symbol** | **Clock Parameter** | **Conditions** |
| $t_{INSU}$ | Setup time with global clock at IOE register | |
| $t_{INH}$ | Hold time with global clock at IOE register | |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE output register | C1 = 35 pF |
| $t_{INSUPLL}$ | Setup time with PLL clock at IOE input register | |
| $t_{INHPLL}$ | Hold time with PLL clock at IOE input register | |
| $t_{OUTCOPLL}$ | Clock-to-output delay with PLL clock at IOE output register | C1 = 35 pF |

| *Table 54. EP20K200C External Bidirectional Timing Parameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-7 Speed Grade** | | **-8 Speed Grade** *(2)* | | **-9 Speed Grade** *(2)* | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{INSUBIDIR}$ | 2.0 | | | | | | ns |
| $t_{INHBIDIR}$ | 0.0 | | | | | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 5.0 | | | | | ns |
| $t_{XZBIDIR}$ | | 7.1 | | | | | ns |
| $t_{ZXBIDIR}$ | | 7.1 | | | | | ns |
| $t_{INSUBIDIRPLL}$ | 3.9 | | | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.0 | | | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.5 | 2.1 | | | | | ns |
| $t_{XZBIDIRPLL}$ | | 4.2 | | | | | ns |
| $t_{ZXBIDIRPLL}$ | | 4.2 | | | | | ns |

| *Table 55. EP20K400C $f_{MAX}$ LE Timing Parameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-7 Speed Grade** | | **-8 Speed Grade** *(2)* | | **-9 Speed Grade** *(2)* | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{SU}$ | 0.3 | | | | | | ns |
| $t_{H}$ | 0.3 | | | | | | ns |
| $t_{CO}$ | | 0.3 | | | | | ns |
| $t_{LUT}$ | | 0.6 | | | | | ns |

*Table 66. EP20K600C External Bidirectional Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade (2) | | -9 Speed Grade (2) | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.4 | | | | | | ns |
| $t_{INHBIDIR}$ | 0.0 | | | | | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 5.0 | | | | | ns |
| $t_{XZBIDIR}$ | | 7.1 | | | | | ns |
| $t_{ZXBIDIR}$ | | 7.1 | | | | | ns |
| $t_{INSUBIDIRPLL}$ | 3.9 | | | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.0 | | | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.5 | 2.1 | | | | | ns |
| $t_{XZBIDIRPLL}$ | | 4.2 | | | | | ns |
| $t_{ZXBIDIRPLL}$ | | 4.2 | | | | | ns |

*Table 67. EP20K1000C $f_{MAX}$ LE Timing Parameters* Note (1)

| Symbol | -7 Speed Grade | | -8 Speed Grade (2) | | -9 Speed Grade (2) | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.3 | | | | | | ns |
| $t_{H}$ | 0.3 | | | | | | ns |
| $t_{CO}$ | | 0.3 | | | | | ns |
| $t_{LUT}$ | | 0.6 | | | | | ns |

Multiple APEX 20KC devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 81. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC16, EPC2, or EPC1 configuration device |
| Passive serial (PS) | MasterBlaster or ByteBlasterMV download cable or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam Standard Test and Programming Language (STAPL) or JBC File |

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices.)*

## Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information.

## Revision History

The information contained in the *APEX 20KC Programmable Logic Device Data Sheet* version 1.1 supersedes information published in pervious versions.

The following changes were made to the *APEX 20KC Programmable Logic Device Data Sheet* version 1.1: updated maximum user I/O pins in Table 1.

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