Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	93
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100ct144c9

- Advanced interconnect structure
  - Copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX 20KC architecture available
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
  - Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
  - Supports popular revision-control software packages including PVCS, RCS, and SCCS

Table 3. APEX 20KC QFP &BGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
EP20K100C	92	151	183	246	
EP20K200C		136	168	271	376
EP20K400C					488
EP20K600C					488
EP20K1000C					488
EP20K1500C					488

Table 4. APEX 20KC FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K100C	93	246			
EP20K200C			376	376	
EP20K400C				488 *(3)*	
EP20K600C				508 *(3)*	588
EP20K1000C				508 *(3)*	708
EP20K1500C					808

Notes to tables:

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20KC device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), and 1.00-mm pitch FineLine BGA packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

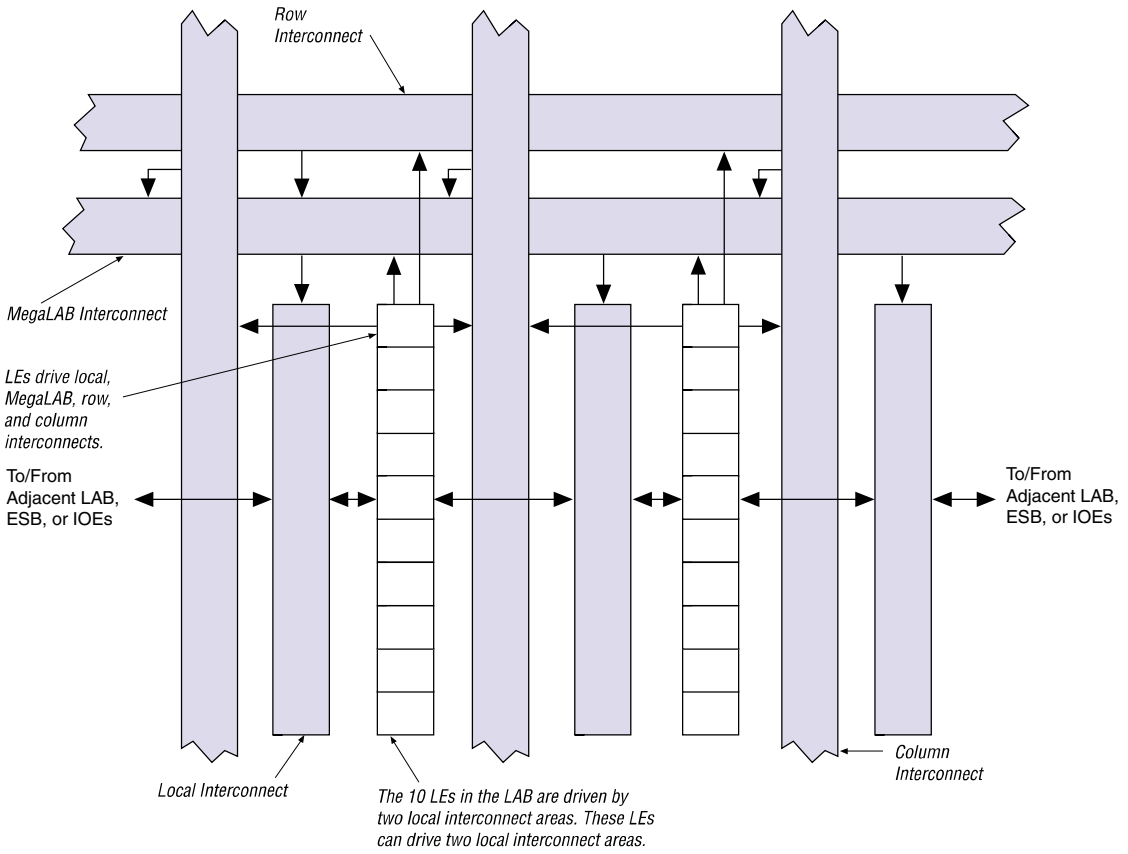
Table 5. APEX 20KC QFP & BGA Package Sizes

Feature	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	356-Pin BGA	652-Pin BGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27
Area (mm^2)	484	924	1,218	1,225	2,025
Length × Width (mm × mm)	22.0 × 22.0	30.4 × 30.4	34.9 × 34.9	35.0 × 35.0	45.0 × 45.0

Table 6. APEX 20KC FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

Figure 3. LAB Structure



Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

LE Operating Modes

The APEX 20KC LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

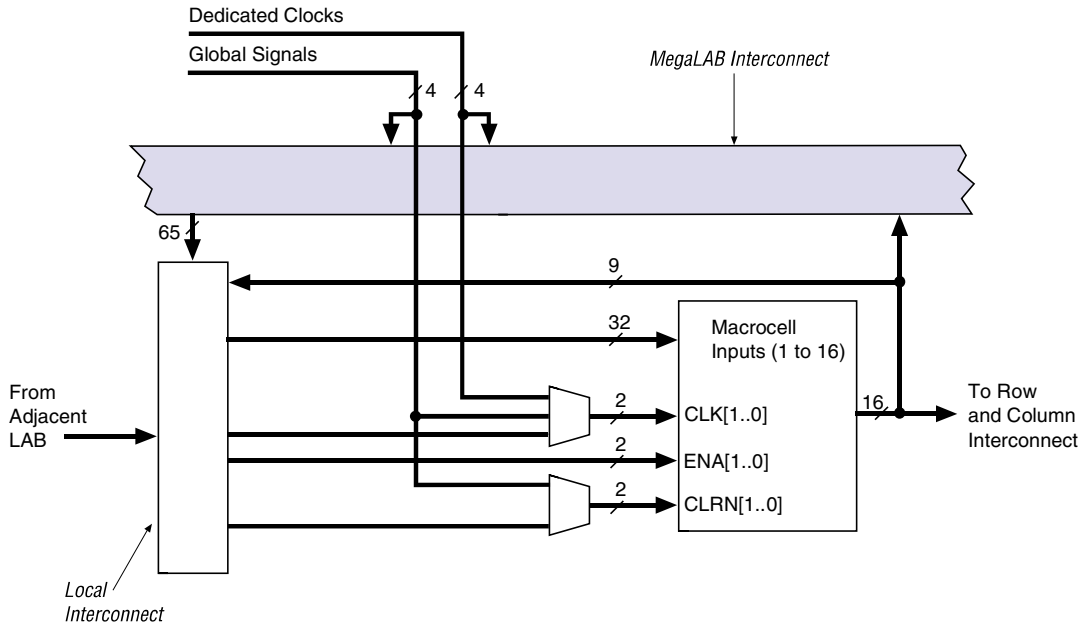
The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 13. Product-Term Logic in ESB

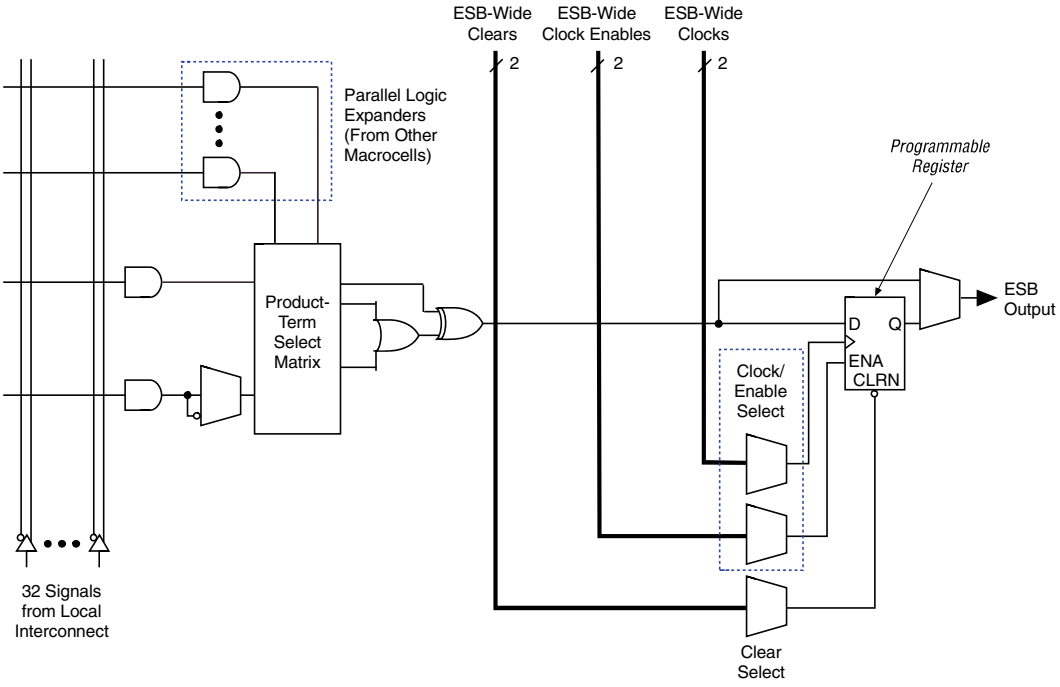


Macrocells

APEX 20KC macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform De Morgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20KC macrocell.

Figure 14. APEX 20KC Macrocell



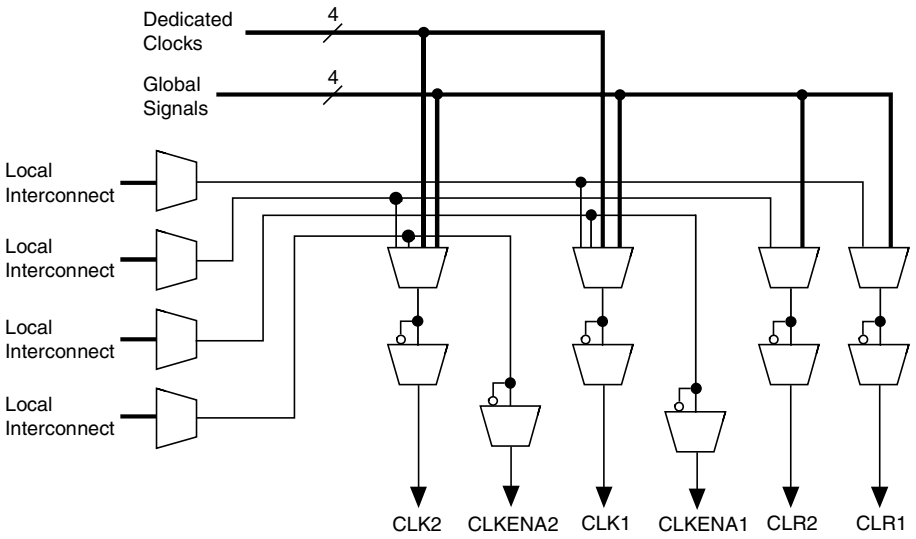
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20KC parallel expanders.

Signals can be driven into APEX 20KC devices before and during power-up without damaging the device. In addition, APEX 20KC devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20KC devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

APEX 20KC devices support the MultiVolt I/O interface feature. The APEX 20KC VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KC device is 5.0-V tolerant with the addition of a resistor.

Table 10 summarizes APEX 20KC MultiVolt I/O support.

Table 10. APEX 20KC MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓ (1)	✓ (1)		✓			
2.5		✓	✓ (1)			✓		
3.3		✓	✓	✓ (2)		✓ (3)	✓	✓

Notes:
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.
(2) An APEX 20KC device can be made 5.0-V tolerant with the addition of an external resistor.
(3) When V_{CCIO} = 3.3 V, an APEX 20KC device can drive a 2.5-V device with 3.3-V tolerant inputs.

Clock Multiplication

The APEX 20KC ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KC ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

All APEX 20KC devices support differential LVDS buffers on the input and output clock signals that interface with external devices. This is controlled in the Quartus II software by assigning the clock pins with an LVDS I/O standard assignment.

Two high-speed PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 Mbps LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400C and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KC ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

The APEX 20KC device instruction register length is 10 bits. The APEX 20KC device USERCODE register length is 32 bits. Tables 14 and 15 show the boundary-scan register length and device IDCODE information for APEX 20KC devices.

Table 14. APEX 20KC Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K100C	774
EP20K200C	1,164
EP20K400C	1,506
EP20K600C	1,806
EP20K1000C	2,190
EP20K1500C	2,502

Table 15. 32-Bit APEX 20KC Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K100C	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K200C	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K400C	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600C	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000C	0000	1001 0000 0000 0000	000 0110 1110	1
EP20K1500C	0000	1001 0101 0000 0000	000 0110 1110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 30 shows the timing requirements for the JTAG signals.

Table 32. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(1)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(2)*			V_{TT} – 0.8	V

Table 33. HSTL Class I I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.71	1.8	1.89	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		0.68	0.75	0.90	V
V_{IH}	High-level input voltage		V_{REF} + 0.1		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			0.4	V

Table 36. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF} *(3)*	Termination and reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(1)*	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(2)*			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high Z)	$GND \le V_{OUT} \le V_{CCIO}$	–10		10	µA

Notes to tables:

(1) The I_{OH} parameter refers to high-level output current.
(2) The I_{OL} parameter refers to low-level output current. This parameter applies to open-drain pins as well as output pins.
(3) V_{REF} specifies center point of switching range.

Figure 32 shows the output drive characteristics of APEX 20KC devices.

Table 48. EP20K100C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.9						ns
$t_{INHBIDIR}$	0.0						ns
$t_{OUTCOBIDIR}$	2.0	5.0					ns
$t_{XZBIDIR}$		7.1					ns
$t_{ZXBIDIR}$		7.1					ns
$t_{INSUBIDIRPLL}$	3.9						ns
$t_{INHBIDIRPLL}$	0.0						ns
$t_{OUTCOBIDIRPLL}$	0.5	2.1					ns
$t_{XZBIDIRPLL}$		4.2					ns
$t_{ZXBIDIRPLL}$		4.2					ns

Table 49. EP20K200C f_{MAX} LE Timing Parameters Note (1)

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.7					ns

Table 50. EP20K200C f_{MAX} ESB Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.4					ns
t_{ESBSRC}		2.5					ns
t_{ESBAWC}		3.1					ns
t_{ESBSWC}		3.0					ns
$t_{ESBWASU}$	0.5						ns
t_{ESBWAH}	0.5						ns
$t_{ESBWDSU}$	0.6						ns
t_{ESBWDH}	0.5						ns
$t_{ESBRASU}$	1.4						ns
t_{ESBRAH}	0.0						ns
$t_{ESBWESU}$	2.3						ns
$t_{ESBDATASU}$	0.0						ns
$t_{ESBWADDRSU}$	0.2						ns
$t_{ESBRADDRSU}$	0.2						ns
$t_{ESBDATACO1}$		1.0					ns
$t_{ESBDATACO2}$		2.3					ns
t_{ESBDD}		2.7					ns
t_{PD}		1.6					ns
$t_{PTERMSU}$	1.0						ns
$t_{PTERMCO}$		1.0					ns

Table 51. EP20K200C f_{MAX} Routing Delays *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.2						ns
t_{F5-20}	0.9						ns
t_{F20+}	1.0						ns

Table 54. EP20K200C External Bidirectional Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.0						ns
$t_{INHBIDIR}$	0.0						ns
$t_{OUTCOBIDIR}$	2.0	5.0					ns
$t_{XZBIDIR}$		7.1					ns
$t_{ZXBIDIR}$		7.1					ns
$t_{INSUBIDIRPLL}$	3.9						ns
$t_{INHBIDIRPLL}$	0.0						ns
$t_{OUTCOBIDIRPLL}$	0.5	2.1					ns
$t_{XZBIDIRPLL}$		4.2					ns
$t_{ZXBIDIRPLL}$		4.2					ns

Table 55. EP20K400C f_{MAX} LE Timing Parameters Note (1)

Symbol	-7 Speed Grade		-8 Speed Grade (2)		-9 Speed Grade (2)		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.3						ns
t_{H}	0.3						ns
t_{CO}		0.3					ns
t_{LUT}		0.6					ns

Table 70. EP20K1000C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.0						ns
t_{CL}	2.0						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.0						ns
t_{ESBCL}	2.0						ns
t_{ESBWP}	1.0						ns
t_{ESBRP}	0.8						ns

Table 71. EP20K1000C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.2						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 76. EP20K1500C Minimum Pulse Width Timing Parameters *Note (1)*

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.0						ns
t_{CL}	2.0						ns
t_{CLRP}	0.2						ns
t_{PREP}	0.2						ns
t_{ESBCH}	2.0						ns
t_{ESBCL}	2.0						ns
t_{ESBWP}	1.0						ns
t_{ESBRP}	0.8						ns

Table 77. EP20K1500C External Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade *(2)*		-9 Speed Grade *(2)*		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.1						ns
t_{INH}	0.0						ns
t_{OUTCO}	2.0	5.0					ns
$t_{INSUPLL}$	3.2						ns
t_{INHPLL}	0.0						ns
$t_{OUTCOPLL}$	0.5	2.1					ns

Table 79. Selectable I/O Standard Input Delays

Symbol	-7 Speed Grade		-8 Speed Grade (1)		-9 Speed Grade (1)		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.1					ns
1.8 V		0.5					ns
PCI		0.4					ns
GTL+		–0.3					ns
SSTL-3 Class I		–0.4					ns
SSTL-3 Class II		–0.4					ns
SSTL-2 Class I		–0.3					ns
SSTL-2 Class II		–0.3					ns
LVDS		–0.2					ns
CTT		–0.3					ns
AGP		0.0					ns

Table 80. Selectable I/O Standard Output Delays

Symbol	-7 Speed Grade		-8 Speed Grade (1)		-9 Speed Grade (1)		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0					ns
LVTTL		0.0					ns
2.5 V		0.5					ns
1.8 V		1.7					ns
PCI		–0.2					ns
GTL+		–0.4					ns
SSTL-3 Class I		–0.1					ns
SSTL-3 Class II		–0.6					ns
SSTL-2 Class I		0.0					ns
SSTL-2 Class II		–0.4					ns
LVDS		–0.8					ns
CTT		–0.2					ns
AGP		–0.4					ns

Note to tables:
(1) Timing information will be released in a future version of this data sheet.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com