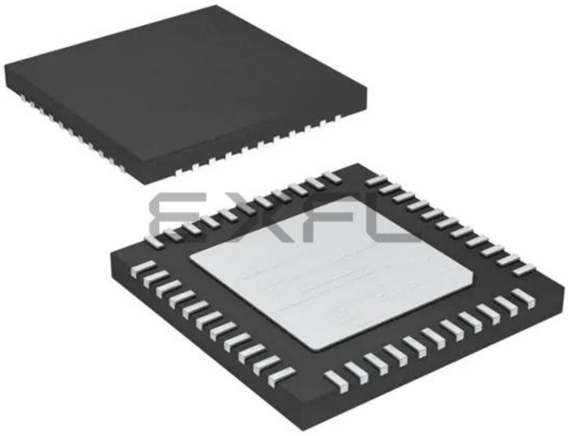

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	363 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f707t-i-ml

TABLE 2-2: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 0											
00h(2)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
01h	TMR0	Timer0 Module Register								0000 0000	0000 0000
02h(2)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
03h(2)	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
04h(2)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
05h	PORTA	PORTA Data Latch when written: PORTA pins when read								xxxx xxxx	uuuu uuuu
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu
08h	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	uuuu uuuu
09h	PORTE	—	—	—	—	RE3	RE2	RE1	RE0	---- xxxx	---- uuuu
0Ah(1),(2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh(2)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	TMR3GIF	TMR3IF	TMRBIF	TMRAIF	—	—	—	CCP2IF	0000 ---0	0000 ---0
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
11h	TMR2	Timer2 Module Register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	USART Transmit Data Register								0000 0000	0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: Accessible only when SSPM<3:0> = 1001.

7.4 Oscillator Control

The Oscillator Control (OSCCON) register (Figure 7-1) displays the status and allows frequency selection of the internal oscillator (INTOSC) system clock. The OSCCON register contains the following bits:

- Frequency selection bits (IRCF)
- Status Locked bits (ICSL)
- Status Stable bits (ICSS)

REGISTER 7-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	U-0	R/W-1	R/W-0	R-q	R-q	U-0	U-0
—	—	IRCF1	IRCF0	ICSL	ICSS	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
q = Value depends on condition			

bit 7-6	**Unimplemented:** Read as ‘0’
bit 5-4	**IRCF<1:0>:** Internal Oscillator Frequency Select bits When PLLEN = 1 (16 MHz INTOSC) 11 = 16 MHz 10 = 8 MHz (POR value) 01 = 4 MHz 00 = 2 MHz When PLLEN = 0 (500 kHz INTOSC) 11 = 500 kHz 10 = 250 kHz (POR value) 01 = 125 kHz 00 = 62.5 kHz
bit 3	**ICSL:** Internal Clock Oscillator Status Locked bit (2% Stable) 1 = 16 MHz/500 kHz Internal Oscillator (HFIOSC) is in lock. 0 = 16 MHz/500 kHz Internal Oscillator (HFIOSC) has not yet locked.
bit 2	**ICSS:** Internal Clock Oscillator Status Stable bit (0.5% Stable) 1 = 16 MHz/500 kHz Internal Oscillator (HFIOSC) has stabilized to its maximum accuracy 0 = 16 MHz/500 kHz Internal Oscillator (HFIOSC) has not yet reached its maximum accuracy
bit 1-0	**Unimplemented:** Read as ‘0’

REGISTER 10-1: FVRCON: FIXED VOLTAGE REFERENCE REGISTER

R-q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVRRDY(1)	FVREN	—	—	CDAFVR1(2)	CDAFVR0(2)	ADFVR1(2)	ADFVR0(2)
bit 7							bit 0

Legend:
R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0'
-n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown
q = Value depends on condition

bit 7 **FVRRDY:** Fixed Voltage Reference Ready Flag bit(1)
- `0` = Fixed Voltage Reference output is not active or stable
- `1` = Fixed Voltage Reference output is ready for use

bit 6 **FVREN:** Fixed Voltage Reference Enable bit
- `0` = Fixed Voltage Reference is disabled
- `1` = Fixed Voltage Reference is enabled

bit 5-4 **Reserved:** Read as '`0`'. Maintain these bits clear

bit 3-2 **CDAFVR<1:0>:** Cap Sense and D/A Converter Fixed Voltage Reference Selection bit(2)
- `00` = CSM and D/A Converter Fixed Voltage Reference Peripheral output is off.
- `01` = CSM and D/A Converter Fixed Voltage Reference Peripheral output is 1x (1.024V)
- `10` = CSM and D/A Converter Fixed Voltage Reference Peripheral output is 2x (2.048V)
- `11` = CSM and D/A Converter Fixed Voltage Reference Peripheral output is 4x (4.096V)

bit 1-0 **ADFVR<1:0>:** A/D Converter Fixed Voltage Reference Selection bit(2)
- `00` = A/D Converter Fixed Voltage Reference Peripheral output is off.
- `01` = A/D Converter Fixed Voltage Reference Peripheral output is 1x (1.024V)
- `10` = A/D Converter Fixed Voltage Reference Peripheral output is 2x (2.048V)
- `11` = A/D Converter Fixed Voltage Reference Peripheral output is 4x (4.096V)

Note 1: FVRRDY is always '`1`' on PIC16F707 devices.
2: Fixed Voltage Reference output cannot exceed V_{DD}.

TABLE 10-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
FVRCON	FVRRDY	FVREN	Reserved	Reserved	CDAFVR1	CDAFVR0	ADFVR1	ADFVR0	`q000 0000`	`q000 0000`

Legend: Shaded cells are not used by the voltage reference module.

13.0 TIMER1/3 MODULES WITH GATE CONTROL

The Timer1 and Timer3 modules are 16-bit timers/counters with the following features:

- 16-bit timer/counter register pair (TMRxH:TMRxL)
- Programmable internal or external clock source
- 3-bit prescaler
- Dedicated LP oscillator circuit (Timer1 only)
- Synchronous or asynchronous operation
- Multiple Timer1/3 gate (count enable) sources
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function (Timer1 only)
- Special Event Trigger with CCP (Timer1 only)
- Selectable Gate Source Polarity
- Gate Toggle mode
- Gate Single-pulse mode
- Gate Value Status
- Gate Event Interrupt

Figure 13-1 is a block diagram of the Timer1/3 modules.

TABLE 13-5: TIMER1/3 GATE SOURCES

TxGSS	Timer1 Gate Source	Timer3 Gate Source
00	Timer1 Gate Pin	Timer3 Gate Pin
01	Overflow of TimerA (TMRA increments from FFh to 00h)	Overflow of TimerB (TMRB increments from FFh to 00h)
10	Timer2 match PR2 (TMR2 increments to match PR2)	Timer2 match PR2 (TMR2 increments to match PR2)
11	Count Enabled by WDT Overflow (Watchdog Time-out interval expired)	Count Enabled by WDT Overflow (Watchdog Time-out interval expired)

13.6.3 TxG PIN GATE OPERATION

The TxG pin is one source for Timer1/3 gate control. It can be used to supply an external source to the Timer1/3 gate circuitry. Timer1 gate can be configured for the T1G pin and Timer3 gate can be configured for the T3G pin.

13.6.4 TIMERA/B OVERFLOW GATE OPERATION

When TimerA/B increments from FFh to 00h a low-to-high pulse will automatically be generated and internally supplied to the Timer1/3 gate circuitry. Timer1 gate can be configured for TimerA overflow and Timer3 gate can be configured for TimerB overflow.

13.6.5 TIMER2 MATCH GATE OPERATION

The TMR2 register will increment until it matches the value in the PR2 register. On the very next increment cycle, TMR2 will be reset to 00h. When this Reset occurs, a low-to-high pulse will automatically be generated and internally supplied to the Timer1/3 gate circuitry. Both Timer1 gate and Timer3 gate can be configured for the Timer2 match.

13.6.6 WATCHDOG OVERFLOW GATE OPERATION

The Watchdog Timer oscillator, prescaler and counter will be automatically turned on when TMRxGE = 1 and TxGSS selects the WDT as a gate source for Timer1/3 (TxGSS = 11). TMRxON does not factor into the oscillator, prescaler and counter enable. See Table 13-6. Both Timer1 gate and Timer3 gate can be configured for Watchdog overflow.

The PSA and PS bits of the OPTION register still control what time-out interval is selected. Changing the prescaler during operation may result in a spurious capture.

Enabling the Watchdog Timer oscillator does not automatically enable a Watchdog Reset or wake-up from Sleep upon counter overflow.

> **Note:** When using the WDT as a gate source for Timer1/3, operations that clear the Watchdog Timer (`CLRWDT`, `SLEEP` instructions) will affect the time interval being measured for capacitive sensing. This includes waking from Sleep. All other interrupts that might wake the device from Sleep should be disabled to prevent them from disturbing the measurement period.

As the gate signal coming from the WDT counter will generate different pulse widths, depending on if the WDT is enabled, when the `CLRWDT` instruction is executed, and so on, Toggle mode must be used. A specific sequence is required to put the device into the correct state to capture the next WDT counter interval.

TABLE 13-6: WDT/TIMER1/3 GATE INTERRACTION

WDTE	TMRxGE = 1 and TxGSS = 11	WDT Oscillator Enable	WDT Reset	Wake-up	WDT Available for TxG Source
1	N	Y	Y	Y	N
1	Y	Y	Y	Y	Y
0	Y	Y	N	N	Y
0	N	N	N	N	N

REGISTER 16-2: CPSxCON1: CAPACITIVE SENSING CONTROL REGISTER 1

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	CPSxCH3	CPSxCH2	CPSxCH1	CPSxCH0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **CPSxCH<3:0>:** Capacitive Sensing Channel Select bits

If CPSxON = 0:

These bits are ignored. No channel is selected.

If CPSxON = 1:

0000 = channel 0, (CPSx0)
0001 = channel 1, (CPSx1)
0010 = channel 2, (CPSx2)
0011 = channel 3, (CPSx3)
0100 = channel 4, (CPSx4)
0101 = channel 5, (CPSx5)
0110 = channel 6, (CPSx6)
0111 = channel 7, (CPSx7)
1000 = channel 8, (CPSx8)
1001 = channel 9, (CPSx9)
1010 = channel 10, (CPSx10)
1011 = channel 11, (CPSx11)
1100 = channel 12, (CPSx12)
1101 = channel 13, (CPSx13)
1110 = channel 14, (CPSx14)
1111 = channel 15, (CPSx15)

REGISTER 17-1: CCPxCON: CCPx CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DCxB<1:0>**: PWM Duty Cycle Least Significant bits
Capture mode:
Unused
Compare mode:
Unused
PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0 **CCPxM<3:0>:** CCP Mode Select bits
0000 = Capture/Compare/PWM off (resets CCP module)
0001 = Unused (reserved)
0010 = Compare mode, toggle output on match (CCPxIF bit of the PIRx register is set)
0011 = Unused (reserved)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit of the PIRx register is set)
1001 = Compare mode, clear output on match (CCPxIF bit of the PIRx register is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set of the PIRx register, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit of the PIRx register is set, TMR1 is reset and A/D conversion(1) is started if the ADC module is enabled. CCPx pin is unaffected.)
11xx = PWM mode.

Note 1: A/D conversion start feature is available only on CCP2.

TABLE 17-3: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELB	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	1111 1111	1111 1111
ANSELC	ANSC7	ANSC6	ANSC5	—	—	ANSC2	ANSC1	ANSC0	111- -111	111- -111
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
CCPRxL	Capture/Compare/PWM Register X Low Byte								xxxx xxxx	uuuu uuuu
CCPRxH	Capture/Compare/PWM Register X High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIE2	TMR3GIE	TMR3IE	TMRBIE	TMRAIE	—	—	—	CCP2IE	0000 ---0	0000 ---0
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIR2	TMR3GIF	TMR3IF	TMRBIF	TMRAIF	—	—	—	CCP2IF	0000 ---0	0000 ---0
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	0000 00-0	uuuu uu-u
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS1	T1GSS0	0000 0x00	0000 0x00
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the capture.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

1. The first character will immediately transfer to the TSR register and transmit.
2. The second word will remain in TXREG register.
3. The TXIF bit will not be set.
4. After the first character has been shifted out of TSR, the TXREG register will transfer the second character to the TSR and the TXIF bit will now be set.
5. If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.

18.3.2.2 Synchronous Slave Transmission Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the CREN and SREN bits.
3. If using interrupts, ensure that the GIE and PEIE bits of the INTCON register are set and set the TXIE bit.
4. If 9-bit transmission is desired, set the TX9 bit.
5. Enable transmission by setting the TXEN bit.
6. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
8. Start transmission by writing the Least Significant eight bits to the TXREG register.

TABLE 18-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELC	ANSC7	ANSC6	ANSC5	—	—	ANSC2	ANSC1	ANSC0	111- -111	111- -111
INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as ‘0’. Shaded cells are not used for synchronous slave transmission.

18.3.2.3 AUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 18.3.1.4 “Synchronous Master Reception”**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a “don’t care” in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE interrupt enable bit of the PIE1 register is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

18.3.2.4 Synchronous Slave Reception Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
3. If 9-bit reception is desired, set the RX9 bit.
4. Verify address detection is disabled by clearing the ADDEN bit of the RCSTA register.
5. Set the CREN bit to enable reception.
6. The RCIF bit of the PIR1 register will be set when reception is complete. An interrupt will be generated if the RCIE bit of the PIE1 register was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register.

19.1.1.3 Master Mode Setup

In Master mode, the data is transmitted/received as soon as the SSPBUF register is loaded with a byte value. If the master is only going to receive, SDO output could be disabled (programmed and used as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate.

When initializing SPI Master mode operation, several options need to be specified. This is accomplished by programming the appropriate control bits in the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- SCK as clock output
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)
- Clock bit rate

In Master mode, the SPI clock rate (bit rate) is user selectable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 • TCY)
- FOSC/64 (or 16 • TCY)
- (Timer2 output)/2

This allows a maximum data rate of 5 Mbps (at FOSC = 20 MHz).

Figure 19-3 shows the waveforms for Master mode. The clock polarity is selected by appropriately programming the CKP bit of the SSPCON register. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The sample time of the input data is shown based on the state of the SMP bit and can occur at the middle or end of the data output time. The time when the SSPBUF is loaded with the received data is shown.

19.1.1.4 Sleep in Master Mode

In Master mode, all module clocks are halted and the transmission/reception will remain in their current state, paused, until the device wakes from Sleep. After the device wakes up from Sleep, the module will continue to transmit/receive data.

REGISTER 20-1: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

U-1	U-0	U-0	U-0	U-0	U-0	U-0	R/S-0
—	—	—	—	—	—	—	RD
bit 7							bit 0

Legend:		S = Setable bit, cleared in hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘1’

bit 6-1 **Unimplemented:** Read as ‘0’

bit 0 **RD:** Read Control bit
1 = Initiates a program memory read (The RD is cleared in hardware; the RD bit can only be set (not cleared) in software).
0 = Does not initiate a program memory read

REGISTER 20-2: PMDATH: PROGRAM MEMORY DATA HIGH REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	PMD13	PMD12	PMD11	PMD10	PMD9	PMD8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PMD<13:8>:** The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

REGISTER 20-3: PMDATL: PROGRAM MEMORY DATA LOW REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PMD<7:0>:** The value of the program memory word pointed to by PMADRH and PMADRL after a program memory read command.

REGISTER 20-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	PMA12	PMA11	PMA10	PMA9	PMA8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **PMA<12:8>:** Program Memory Read Address bits

REGISTER 20-5: PMADRL: PROGRAM MEMORY ADDRESS LOW REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
PMA7	PMA6	PMA5	PMA4	PMA3	PMA2	PMA1	PMA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PMA<7:0>:** Program Memory Read Address bits

TABLE 20-1: SUMMARY OF REGISTERS ASSOCIATED WITH PROGRAM MEMORY READ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PMCON1	—	—	—	—	—	—	—	RD	1--- ---0	1--- ---0
PMADRH	—	—	—	Program Memory Read Address Register High Byte					---x xxxx	---x xxxx
PMADRL	Program Memory Read Address Register Low Byte								xxxx xxxx	xxxx xxxx
PMDATH	—	—	Program Memory Read Data Register High Byte						--xx xxxx	--xx xxxx
PMDATL	Program Memory Read Data Register Low Byte								xxxx xxxx	xxxx xxxx

Legend: x = unknown, u = unchanged, – = unimplemented, read as ‘0’. Shaded cells are not used by the program memory read.

25.6 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

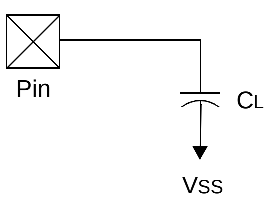
pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{\text{RD}}$
cs	$\overline{\text{CS}}$	rw	$\overline{\text{RD}}$ or $\overline{\text{WR}}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{\text{SS}}$
dt	Data in	t0	T0CKI
io	I/O PORT	t1	T1CKI
mc	$\overline{\text{MCLR}}$	wr	$\overline{\text{WR}}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

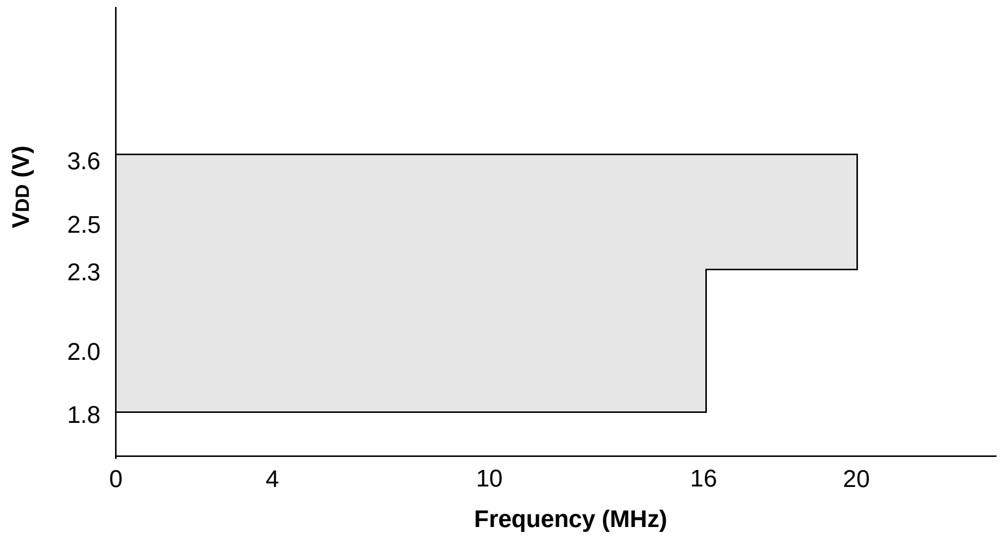
FIGURE 25-2: LOAD CONDITIONS

Load Condition



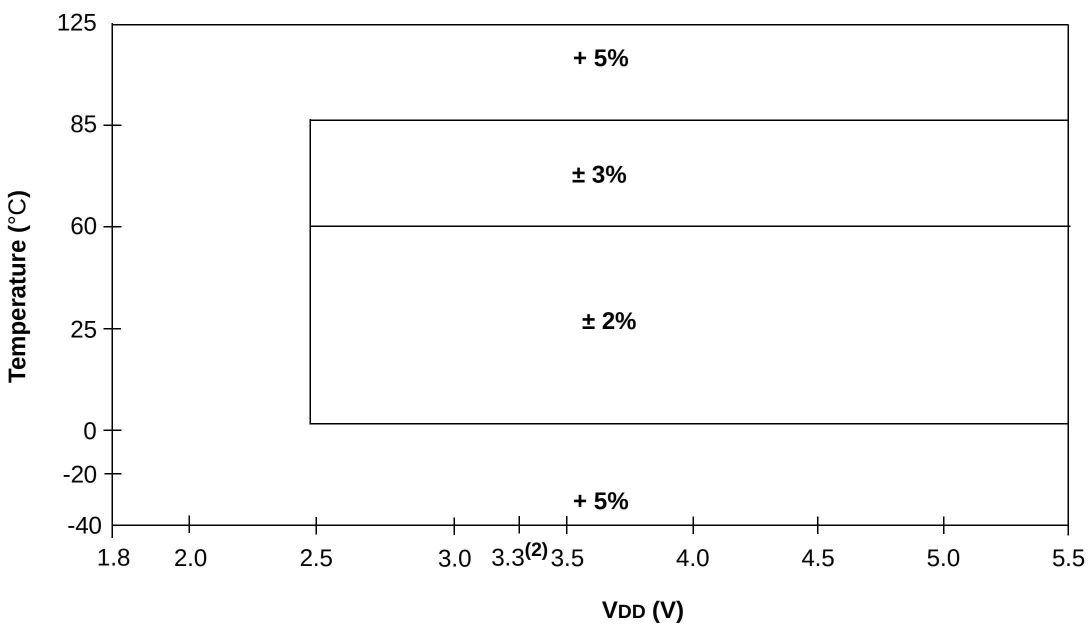
Legend: C_L = 50 pF for all pins, 15 pF for OSC2 output

FIGURE 25-5: PIC16LF707 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 25-1 for each Oscillator mode's supported frequencies.

FIGURE 25-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



Note 1: This chart covers both regulator enabled and regulator disabled states.
2: Regulator Nominal voltage.

TABLE 25-13: I^{2}C BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
SP100*	T_{HIGH}	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	$1.5T_{CY}$	—		
SP101*	T_{LOW}	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP Module	$1.5T_{CY}$	—		
SP102*	T_R	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + $0.1C_B$	300	ns	C_B is specified to be from 10-400 pF
SP103*	T_F	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + $0.1C_B$	250	ns	C_B is specified to be from 10-400 pF
SP106*	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
SP107*	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
SP109*	T_{AA}	Output valid from clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
SP110*	T_{BUF}	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
SP111	C_B	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I^{2}C bus device can be used in a Standard mode (100 kHz) I^{2}C bus system, but the requirement $T_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line T_R max. + $T_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^{2}C bus specification), before the SCL line is released.

FIGURE 26-4: PIC16LF707 TYPICAL IDD vs. FOSC OVER VDD, EC MODE

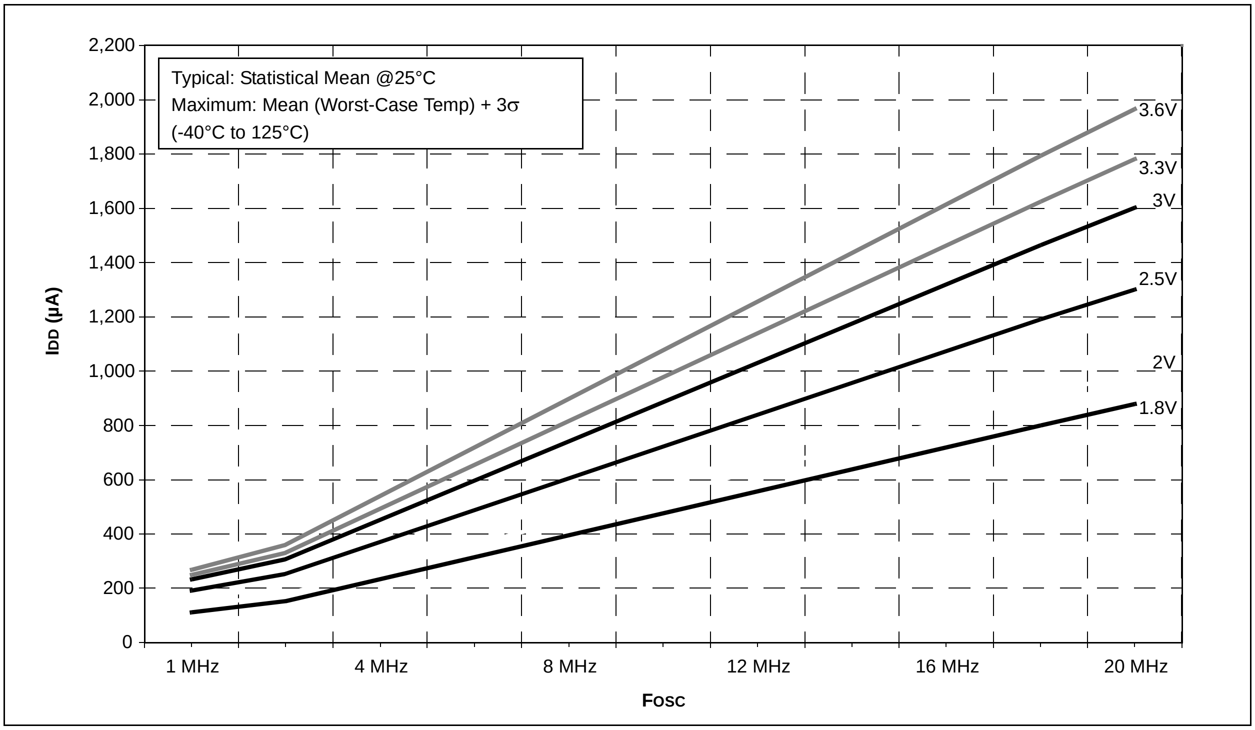


FIGURE 26-5: PIC16F707 MAXIMUM IDD vs. VDD OVER FOSC, EXTRC MODE, VCAP = 0.1µF

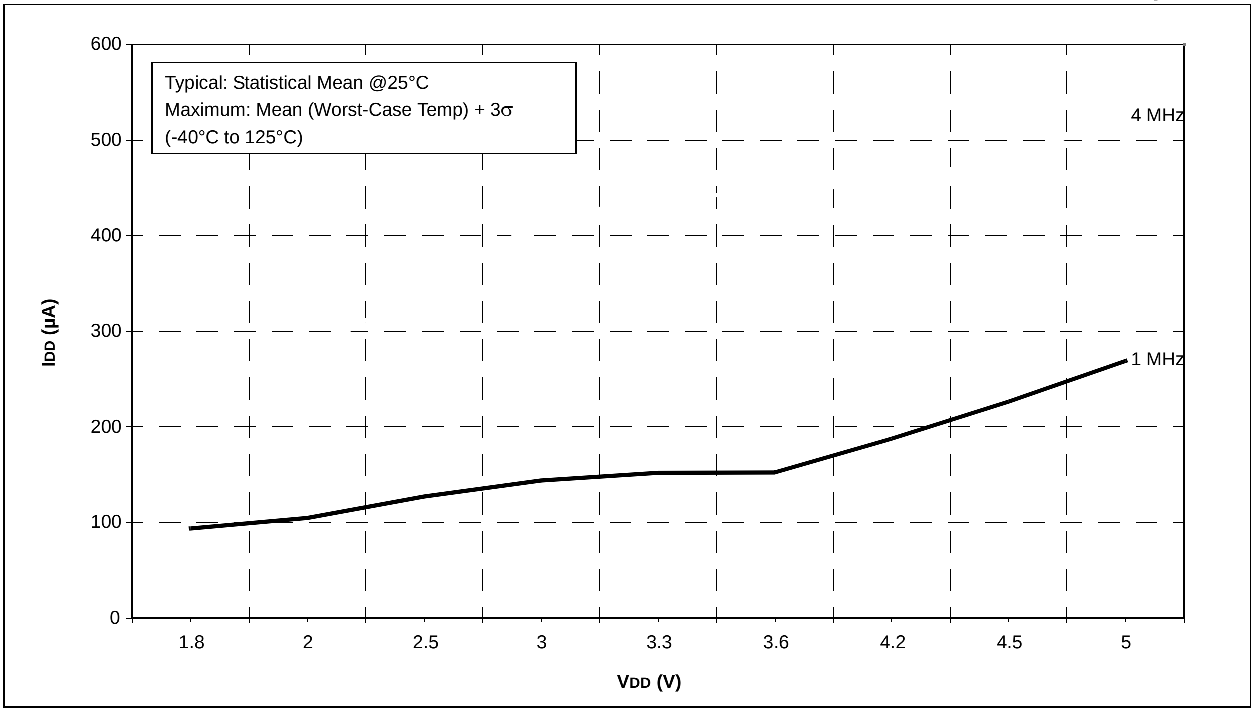


FIGURE 26-8: PIC16LF707 TYPICAL I_{DD} vs. V_{DD} OVER F_{OSC}, EXTRC MODE

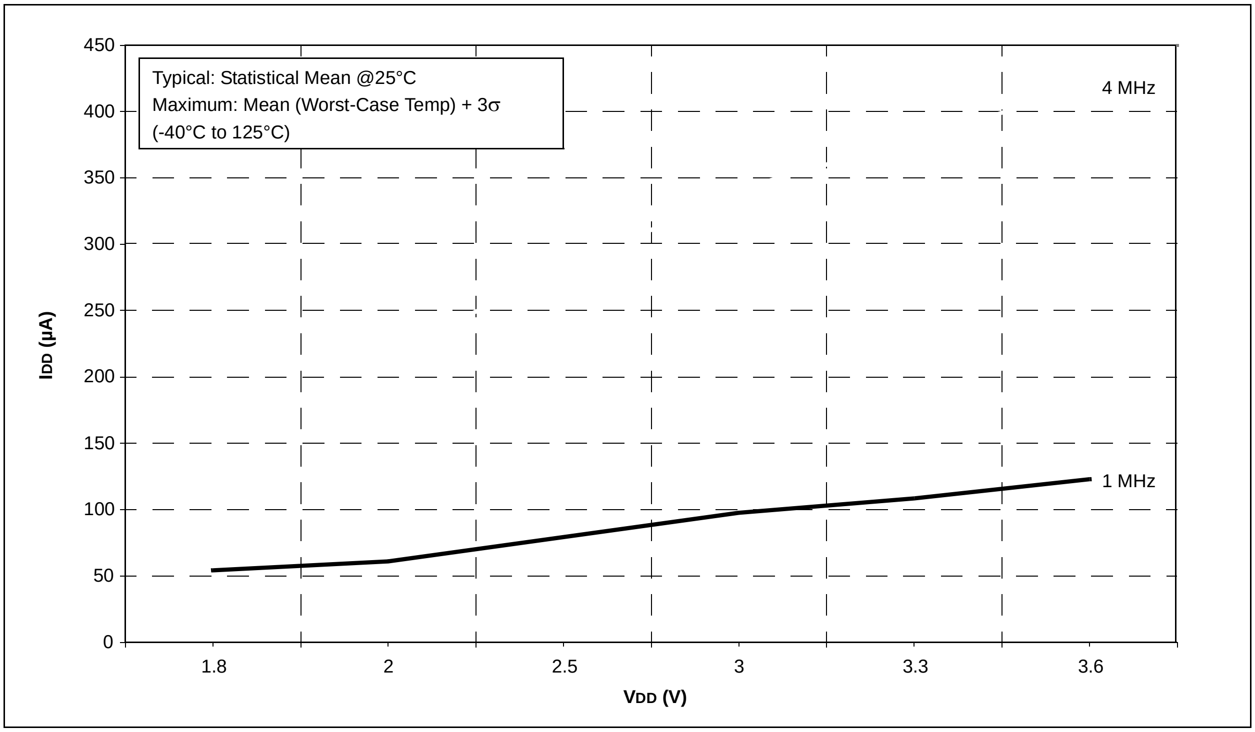


FIGURE 26-9: PIC16F707 MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD}, HS MODE, V_{CAP} = 0.1µF

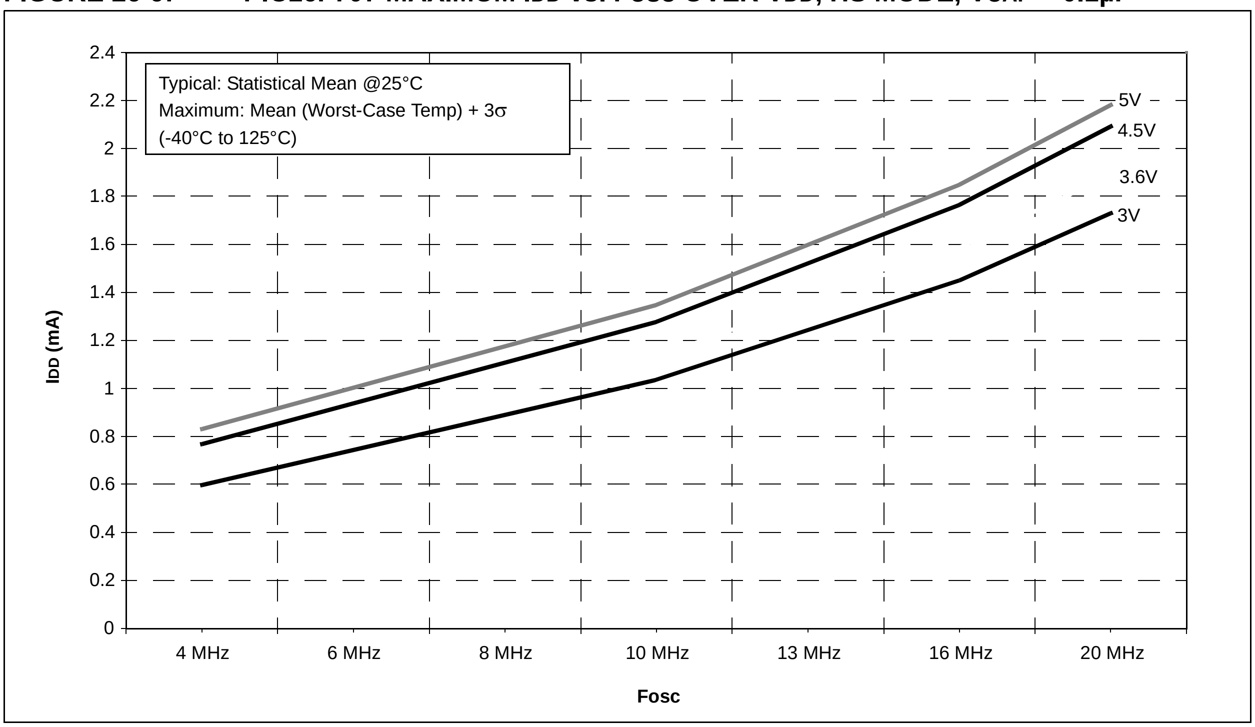


FIGURE 26-22: PIC16LF707 MAXIMUM IDD vs. FOSC OVER VDD, INTOSC MODE

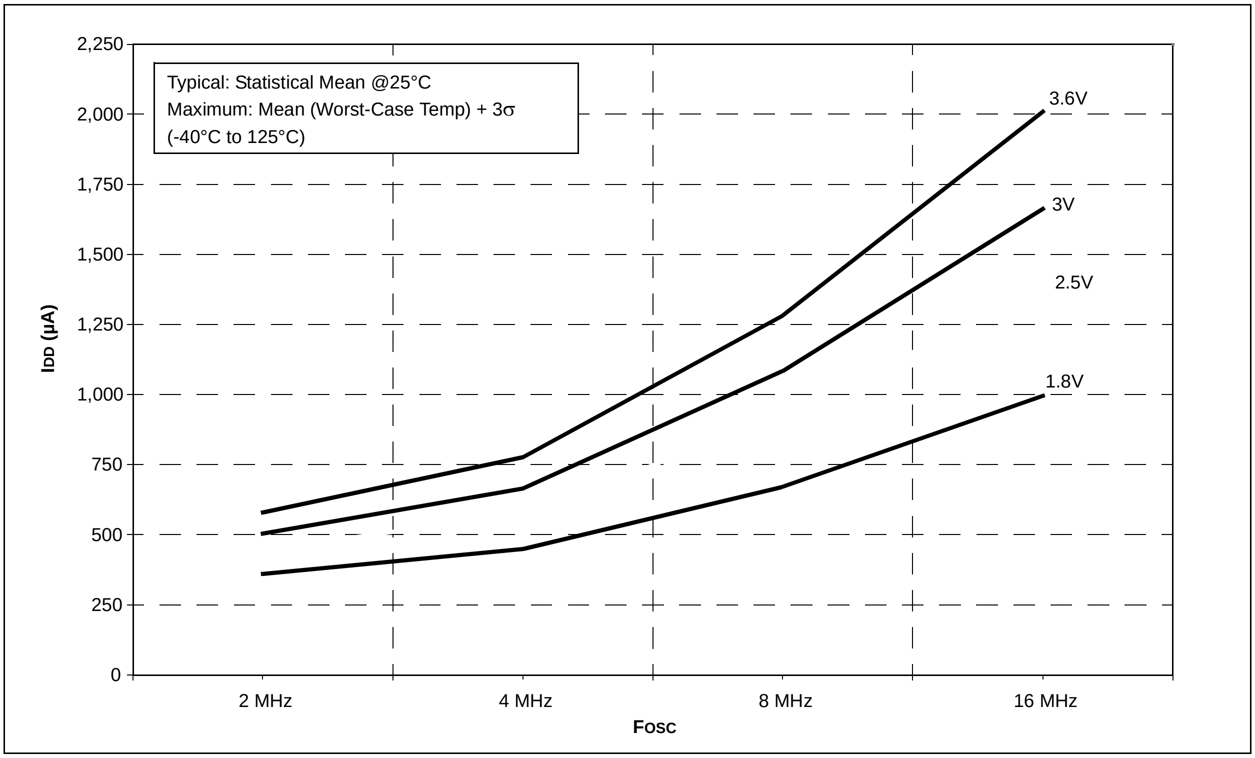


FIGURE 26-23: PIC16F707 TYPICAL IDD vs. FOSC OVER VDD, INTOSC MODE, VCAP = 0.1µF

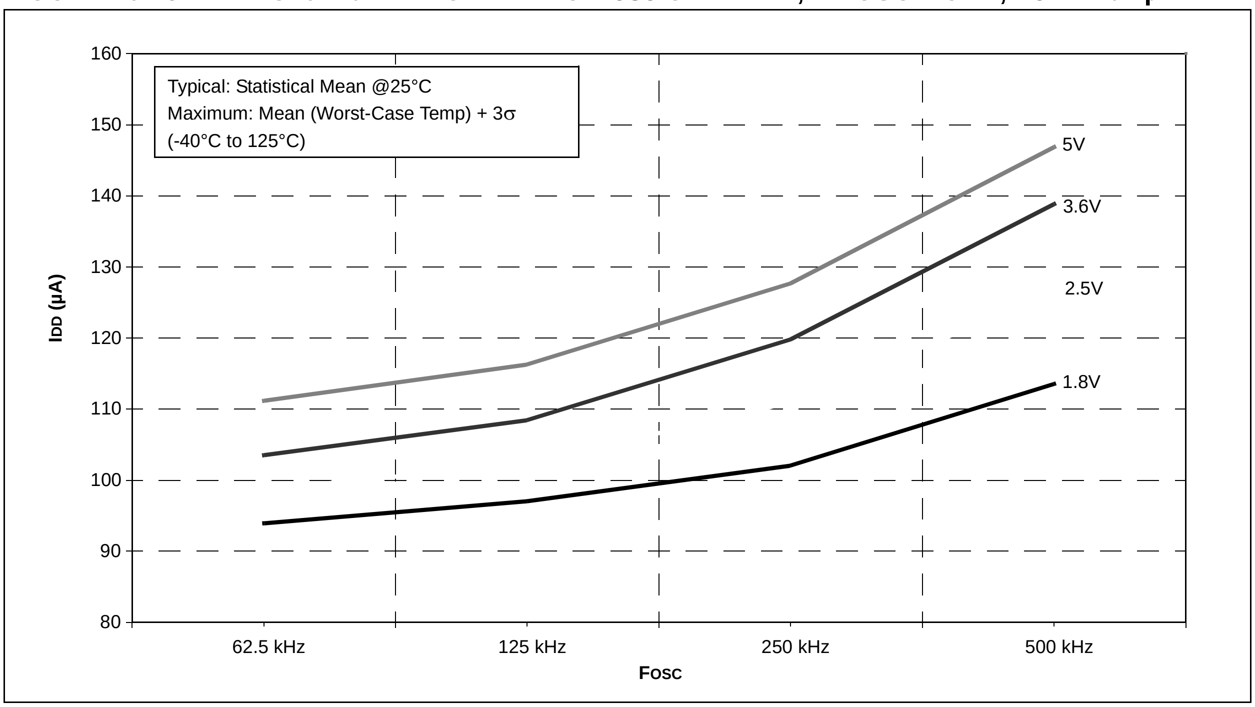


FIGURE 26-30: PIC16LF707 TYPICAL BASE IPD vs. VDD

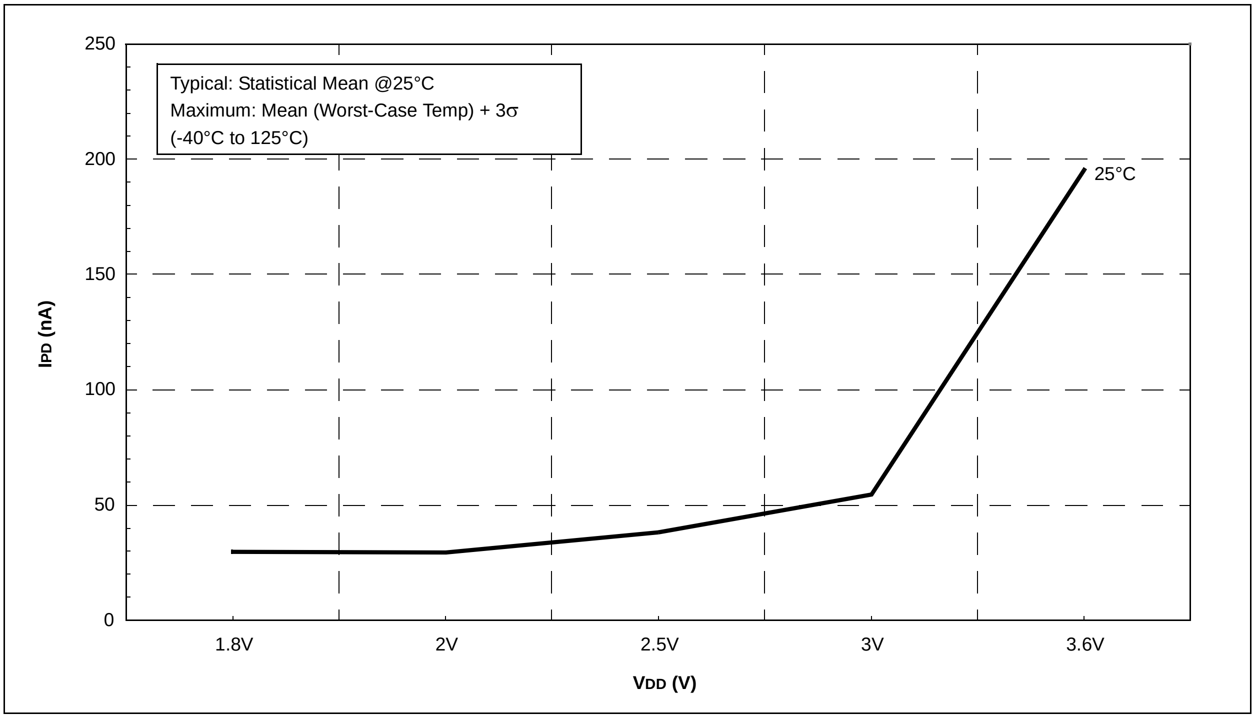
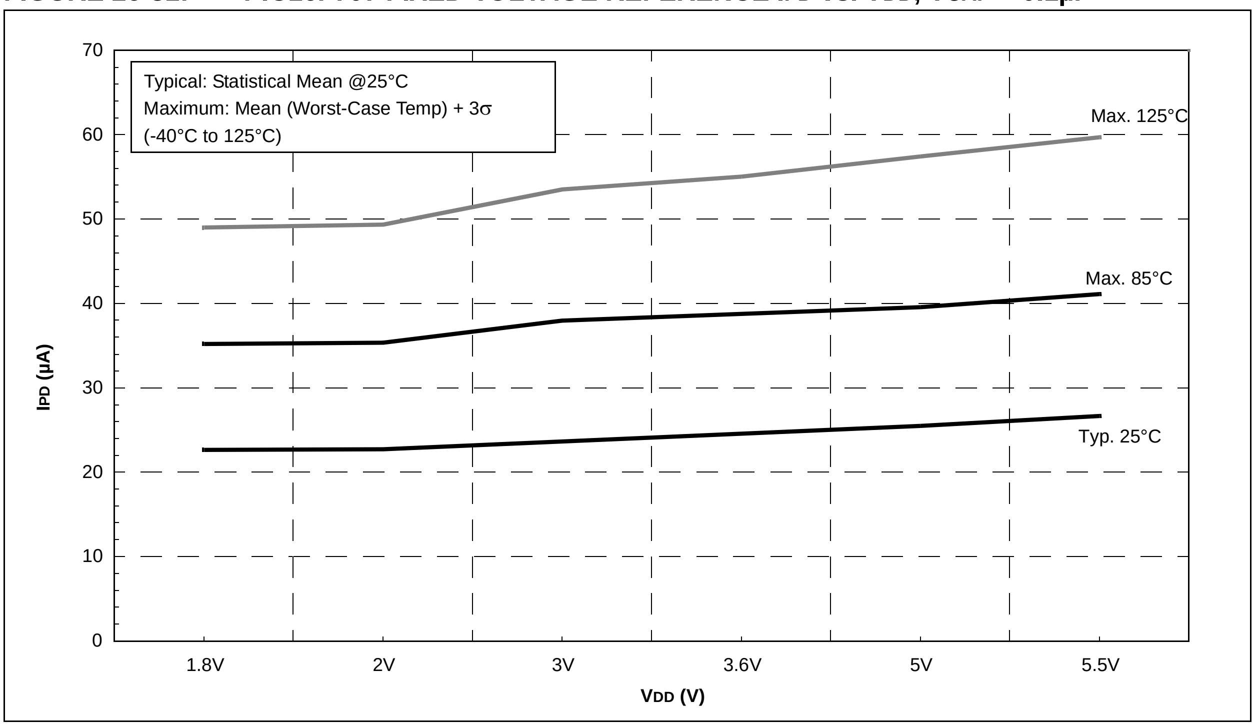


FIGURE 26-31: PIC16F707 FIXED VOLTAGE REFERENCE IPD vs. VDD, VCAP = 0.1µF



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