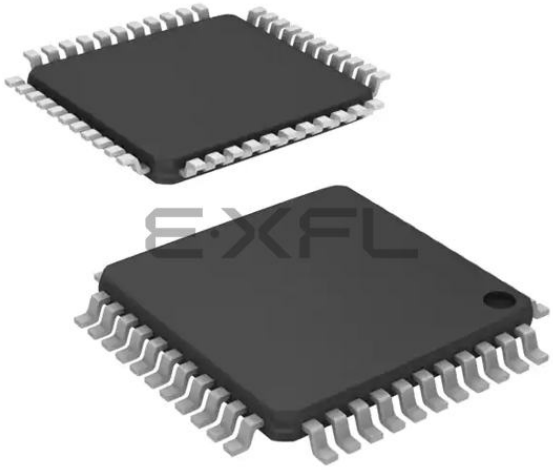

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Applications of "Embedded - Microcontrollers"

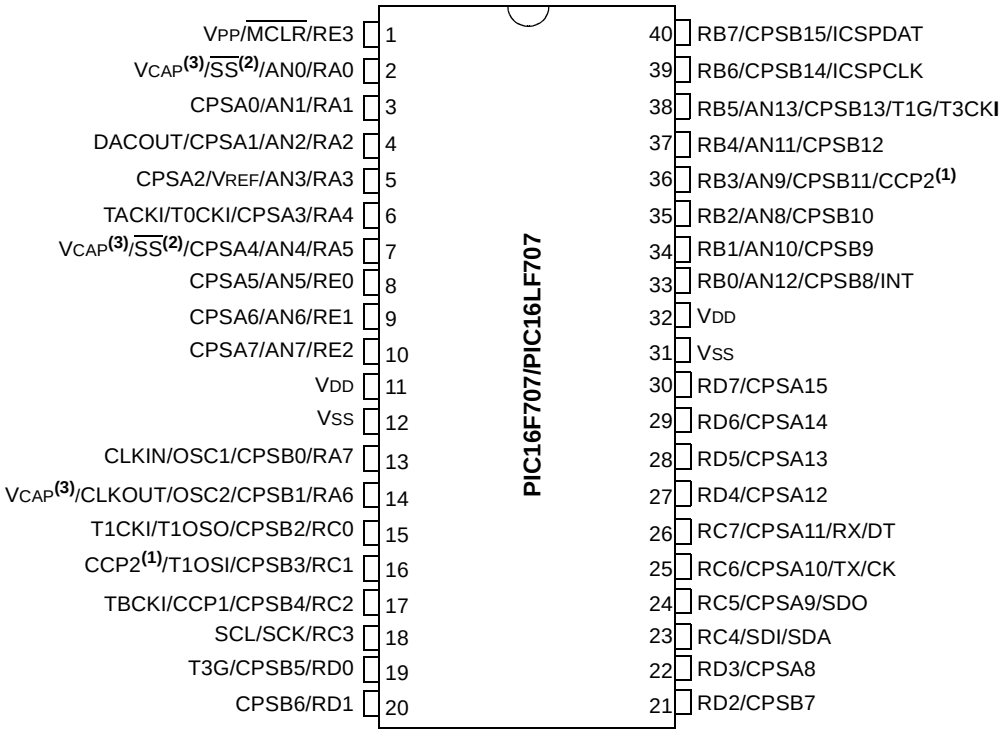
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	363 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f707t-i-pt

- Two Capture, Compare, PWM modules (CCP):
  - 16-bit Capture, max. resolution 12.5 ns
  - 16-bit Compare, max. resolution 200 ns
  - 10-bit PWM, max. frequency 20 kHz
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART)
- Synchronous Serial Port (SSP):
  - SPI (Master/Slave)
  - I^2C (Slave) with Address Mask
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive reference selection

Device	Program Memory Flash (words)	SRAM (bytes)	High Endurance Flash (bytes)	I/Os	Capacitive Touch Channels	8-bit A/D (ch)	AUSART	CCP	Timers 8/16-bit
PIC16(L)F707	8192	363	128	36	32	14	Yes	2	4/2

PIN DIAGRAMS

FIGURE 1: 40-PIN PDIP



Note 1: CCP2 pin location may be selected as RB3 or RC1.

2: $\overline{SS}$ pin location may be selected as RA5 or RA0.

3: PIC16F707 only.

TABLE 1-1: PIC16(L)F707 PINOUT DESCRIPTION

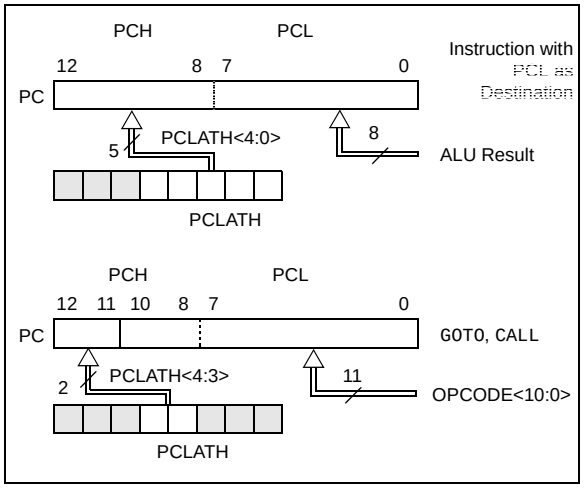
Name	Function	Input Type	Output Type	Description
RA0/AN0/$\overline{SS}$/VCAP	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	$\overline{SS}$	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F only).
RA1/AN1/CPSA0	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	CPSA0	AN	—	Capacitive sensing A input 0.
RA2/AN2/CPSA1/DACOUT	RA2	TTL	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	CPSA1	AN	—	Capacitive sensing A input 1.
	DACOUT	—	AN	Voltage Reference Output.
RA3/AN3/VREF/CPSA2	RA3	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	VREF	AN	—	A/D Voltage Reference input.
	CPSA2	AN	—	Capacitive sensing A input 2.
RA4/CPSA3/T0CKI/TACKI	RA4	TTL	CMOS	General purpose I/O.
	CPSA3	AN	—	Capacitive sensing A input 3.
	T0CKI	ST	—	Timer0 clock input.
	TACKI	ST	—	TimerA clock input.
RA5/AN4/CPSA4/$\overline{SS}$/VCAP	RA5	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPSA4	AN	—	Capacitive sensing A input 4.
	$\overline{SS}$	ST	—	Slave Select input.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F only).
RA6/OSC2/CLKOUT/VCAP/ CPSB1	RA6	TTL	CMOS	General purpose I/O.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	FOSC/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator (PIC16F only).
	CPSB1	AN	—	Capacitive sensing B input 1.
RA7/OSC1/CLKIN/CPSB0	RA7	TTL	CMOS	General purpose I/O.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	CMOS	—	External clock input (EC mode).
	CLKIN	ST	—	RC oscillator connection (RC mode).
	CPSB0	AN	—	Capacitive sensing B input 0.
RB0/AN12/CPSB8/INT	RB0	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN12	AN	—	A/D Channel 12 input.
	CPSB8	AN	—	Capacitive sensing B input 8.
	INT	ST	—	External interrupt.
RB1/AN10/CPSB9	RB1	TTL	CMOS	General purpose I/O. Individually controlled interrupt-on-change. Individually enabled pull-up.
	AN10	AN	—	A/D Channel 10 input.
	CPSB9	AN	—	Capacitive sensing B input 9.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-2 shows the two situations for the loading of the PC. The upper example in Figure 2-2 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-2 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-2: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

2.3.2 STACK

All devices have an 8-level x 13-bit wide hardware stack (refer to Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth PUSH overwrites the value that was stored from the first PUSH. The tenth PUSH overwrites the second PUSH (and so on).

Note 1: There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Program Memory Paging

All devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper two bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is POPed off the stack. Therefore, manipulation of the PCLATH<4:3> bits is not required for the RETURN instructions (which POPs the address from the stack).

Note: The contents of the PCLATH register are unchanged after a RETURN or RETFIE instruction is executed. The user must rewrite the contents of the PCLATH register for any subsequent subroutine calls or GOTO instructions.

Example 2-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the Interrupt Service Routine (if interrupts are used).

EXAMPLE 2-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```
        ORG 500h
        PAGESEL SUB_P1  ;Select page 1
                        ;(800h-FFFh)
        CALL    SUB1_P1 ;Call subroutine in
        :               ;page 1 (800h-FFFh)
        :
        ORG     900h    ;page 1 (800h-FFFh)
SUB1_P1
        :               ;called subroutine
                        ;page 1 (800h-FFFh)
        :
        RETURN          ;return to
                        ;Call subroutine
                        ;in page 0
                        ;(000h-7FFh)
```

TABLE 3-5: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset/ Brown-out Reset(1)	$\overline{\text{MCLR}}$ Reset/ WDT Reset	Wake-up from Sleep through Interrupt/Time-out
ADCON0	1Fh	--00 0000	--00 0000	--uu uuuu
OPTION_REG	81h/181h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	1111 1111	1111 1111	uuuu uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
TRISD	88h	1111 1111	1111 1111	uuuu uuuu
TRISE	89h	---- 1111	---- 1111	---- uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PIE2	8Dh	0000 ---0	0000 ---0	uuuu ---u
PCON	8Eh	---- --qq	---- --uu(1,5)	---- --uu
T1GCON	8Fh	0000 0x00	uuuu uxuu	uuuu uxuu
OSCCON	90h	--10 qq--	--10 qq--	--uu qq--
OSCTUNE	91h	--00 0000	--uu uuuu	--uu uuuu
PR2	92h	1111 1111	1111 1111	uuuu uuuu
SSPADD	93h	0000 0000	0000 0000	uuuu uuuu
SSPMSK	93h	1111 1111	1111 1111	uuuu uuuu
SSPSTAT	94h	0000 0000	0000 0000	uuuu uuuu
WPUB	95h	1111 1111	1111 1111	uuuu uuuu
IOCB	96h	0000 0000	0000 0000	uuuu uuuu
T3CON	97h	0000 -0-0	0000 -0-0	uuuu -u-u
TXSTA	98h	0000 -010	0000 -010	uuuu -uuu
SPBRG	99h	0000 0000	0000 0000	uuuu uuuu
TMR3L	9Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3H	9Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
APFCON	9Ch	---- --00	---- --00	---- --uu
FVRCON	9Dh	q000 0000	q000 0000	q000 0000
ADCON1	9Fh	-000 --00	-000 --00	-uuu --uu
TACON	105h	0-00 0000	0-00 0000	u-uu uuuu
CPSBCON0	106h	00-- 0000	00-- 0000	uu-- uuuu
CPSBCON1	107h	---- 0000	---- 0000	---- uuuu
CPSACON0	108h	00-- 0000	00-- 0000	uu-- uuuu
CPSACON1	109h	---- 0000	---- 0000	---- uuuu
PMDATL	10Ch	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMADRL	10Dh	xxxx xxxx	xxxx xxxx	uuuu uuuu
PMDATH	10Eh	--xx xxxx	--xx xxxx	--uu uuuu
PMADRH	10Fh	---x xxxx	---x xxxx	---u uuuu
TMRA	110h	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 and PIR2 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 3-2 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

4.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt enable bit(s) for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the interrupt enable bit of the interrupt event is contained in the PIE1 and PIE2 registers)

The INTCON, PIR1 and PIR2 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual Interrupt Enable bits.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- PC is loaded with the interrupt vector 0004h

The ISR determines the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack and setting the GIE bit.

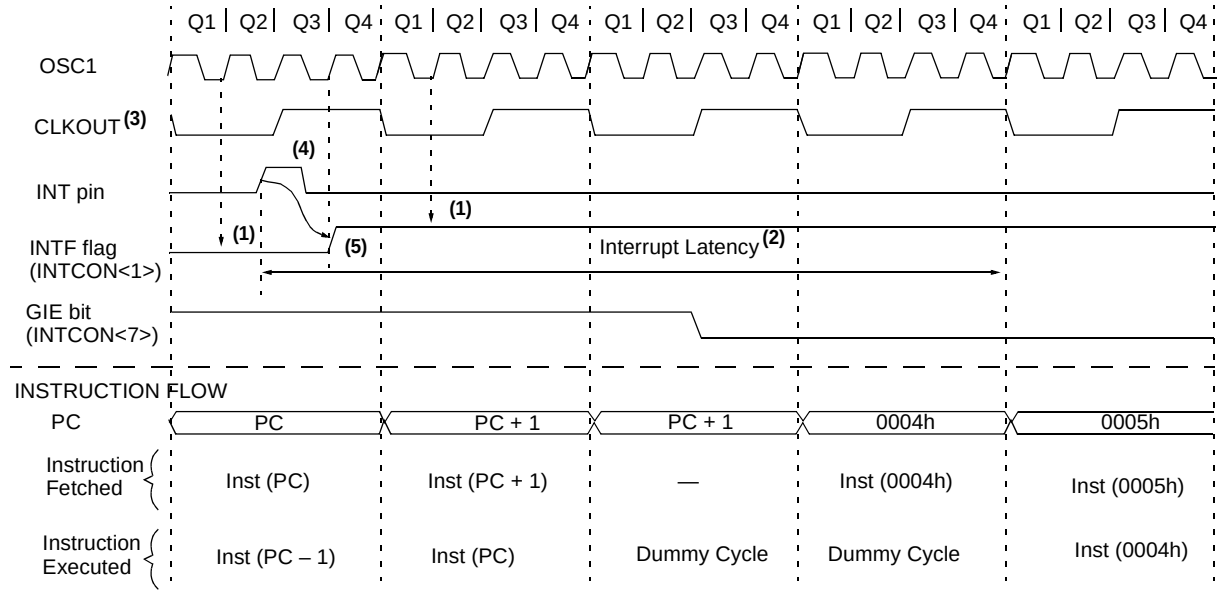
For additional information on a specific interrupt's operation, refer to its peripheral chapter.

Note 1:	Individual interrupt flag bits are set, regardless of the state of any other enable bits.
2:	All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.

4.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The latency for synchronous interrupts is three instruction cycles. For asynchronous interrupts, the latency is three to four instruction cycles, depending on when the interrupt occurs. See Figure 4-2 for timing details.

FIGURE 4-2: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 25.0 "Electrical Specifications"**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

6.4.2.3 RC2/CCP1/CPSB4/TBCKI

These pins are configurable to function as one of the following:

- General purpose I/O
- Capture 1 input, Compare 1 output, and PWM1 output
- Capacitive sensing input
- TimerB Clock input

6.4.2.4 RC3/SCK/SCL

These pins are configurable to function as one of the following:

- General purpose I/O
- SPI clock
- I^2C clock

6.4.2.5 RC4/SDI/SDA

These pins are configurable to function as one of the following:

- General purpose I/O
- SPI data input
- I^2C data I/O

6.4.2.6 RC5/SDO/CPSA9

These pins are configurable to function as one of the following:

- General purpose I/O
- SPI data output
- Capacitive sensing input

6.4.2.7 RC6/TX/CK/CPSA10

These pins are configurable to function as one of the following:

- General purpose I/O
- Asynchronous serial output
- Synchronous clock I/O
- Capacitive sensing input

6.4.2.8 RC7/RX/DT/CPSA11

These pins are configurable to function as one of the following:

- General purpose I/O
- Asynchronous serial input
- Synchronous serial data I/O
- Capacitive sensing input

TABLE 6-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELC	ANSC7	ANSC6	ANSC5	—	—	ANSC2	ANSC1	ANSC0	111- -111	111- -111
APFCON	—	—	—	—	—	—	SSSEL	CCP2SEL	---- --00	---- --00
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000
CPSACON0	CPSAON	CPSARM	—	—	CPSARNG1	CPSARNG0	CPSAOUT	TAXCS	00-- 0000	00-- 0000
CPSACON1	—	—	—	—	CPSACH3	CPSACH2	CPSACH1	CPSACH0	---- 0000	---- 0000
CPSBCON0	CPSBON	CPSBRM	—	—	CPSBRNG1	CPSBRNG0	CPSBOUT	TBXCS	00-- 0000	00-- 0000
CPSBCON1	—	—	—	—	CPSBCH3	CPSBCH2	CPSBCH1	CPSBCH0	---- 0000	---- 0000
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	xxxx xxxx
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	—	TMR1ON	0000 00-0	uuuu uu-u
TBCON	TMRBON	—	TBCS	TBSE	TBPSA	TBPS2	TBPS1	TBPS0	0-00 0000	0-00 0000
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

6.6 PORTE and TRISE Registers

PORTE is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISE. Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). The exception is RE3, which is input-only and its TRIS bit will always read as '1'. Example 6-5 shows how to initialize PORTE.

Reading the PORTE register (Register 6-16) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. RE3 reads '0' when MCLRE = 1.

The TRISE register (Register 6-17) controls the PORTE pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISE register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note:	The ANSELE register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 6-5: INITIALIZING PORTE

```
BANKSEL PORTE        ;
CLRF    PORTE        ;Init PORTE
BANKSEL ANSELE       ;
CLRF    ANSELE       ;digital I/O
BANKSEL TRISE        ;
MOVLW   B'00001100'  ;Set RE<2> as an input
MOVWF   TRISE        ;and set RE<1:0>
                     ;as outputs
```

6.6.1 ANSELE REGISTER

The ANSELE register (Register 6-18) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELE bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELE bits has no affect on digital output functions. A pin with TRIS clear and ANSELE set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

REGISTER 6-16: PORTE: PORTE REGISTER

U-0	U-0	U-0	U-0	R-x	R/W-x	R/W-x	R/W-x
—	—	—	—	RE3	RE2	RE1	RE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **RE<3:0>**: PORTE I/O Pin bits
1 = Port pin is > V_{IH}
0 = Port pin is < V_{IL}

REGISTER 10-1: FVRCON: FIXED VOLTAGE REFERENCE REGISTER

R-q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVRRDY(1)	FVREN	—	—	CDAFVR1(2)	CDAFVR0(2)	ADFVR1(2)	ADFVR0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
q = Value depends on condition			

bit 7 **FVRRDY:** Fixed Voltage Reference Ready Flag bit(1)
- 0 = Fixed Voltage Reference output is not active or stable
- 1 = Fixed Voltage Reference output is ready for use

bit 6 **FVREN:** Fixed Voltage Reference Enable bit
- 0 = Fixed Voltage Reference is disabled
- 1 = Fixed Voltage Reference is enabled

bit 5-4 **Reserved:** Read as '0'. Maintain these bits clear

bit 3-2 **CDAFVR<1:0>:** Cap Sense and D/A Converter Fixed Voltage Reference Selection bit(2)
- 00 = CSM and D/A Converter Fixed Voltage Reference Peripheral output is off.
- 01 = CSM and D/A Converter Fixed Voltage Reference Peripheral output is 1x (1.024V)
- 10 = CSM and D/A Converter Fixed Voltage Reference Peripheral output is 2x (2.048V)
- 11 = CSM and D/A Converter Fixed Voltage Reference Peripheral output is 4x (4.096V)

bit 1-0 **ADFVR<1:0>:** A/D Converter Fixed Voltage Reference Selection bit(2)
- 00 = A/D Converter Fixed Voltage Reference Peripheral output is off.
- 01 = A/D Converter Fixed Voltage Reference Peripheral output is 1x (1.024V)
- 10 = A/D Converter Fixed Voltage Reference Peripheral output is 2x (2.048V)
- 11 = A/D Converter Fixed Voltage Reference Peripheral output is 4x (4.096V)

Note 1: FVRRDY is always '1' on PIC16F707 devices.
2: Fixed Voltage Reference output cannot exceed V_{DD}.

TABLE 10-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
FVRCON	FVRRDY	FVREN	Reserved	Reserved	CDAFVR1	CDAFVR0	ADFVR1	ADFVR0	q000 0000	q000 0000

Legend: Shaded cells are not used by the voltage reference module.

13.1 Timer1/3 Operation

The Timer1 and Timer3 modules are 16-bit incrementing counters which are accessed through the TMRxH:TMRxL register pair. Writes to TMRxH or TMRxL directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1/3 is enabled by configuring the TMRxON and TMRxGE bits in the TxCON and TxGCON registers, respectively. Table 13-2 displays the Timer1/3 enable selections.

TABLE 13-2: TIMER1/3 ENABLE SELECTIONS

TMRxON	TMRxGE	Timer1/3 Operation
0	0	Off
0	1	Off
1	0	Always On
1	1	Count Enabled

13.2 Clock Source Selection

The TMRxCS<1:0> bits of the TxCON register and the T1OSCEN bit of the T1CON register are used to select the clock source for Timer1/3. Table 13-3 displays the clock source selections.

13.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMRxH:TMRxL register pair will increment on multiples of FOSC as determined by the Timer1/3 prescaler.

13.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1/3 modules may work as a timer or a counter.

When enabled to count, Timer1/3 is incremented on the rising edge of the external clock input TxCKI or a capacitive sensing oscillator signal. Either of these external clock sources can be synchronized to the microcontroller system clock or they can be run asynchronously. If set for the capacitive sensing oscillator signal, Timer1 will use the CPS A signal and Timer3 will use the CPS B signal (see Table 13-1).

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated internal oscillator circuit. Only one dedicated internal oscillator circuit is available. See **Section 13.4 "Timer1/3 Oscillator"** for more information.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- Timer1/3 enabled after POR reset
- Write to TMRxH or TMRxL
- Timer1/3 is disabled
- Timer1/3 is disabled (TMRxON = 0) when TxCKI is high, then Timer1/3 is enabled (TMRxON=1) when TxCKI is low.

TABLE 13-3: CLOCK SOURCE SELECTIONS

TMRxCS1	TMRxCS0	T1OSCEN	Timer1 Clock Source	Timer3 Clock Source
0	1	x	System Clock (FOSC)	System Clock (FOSC)
0	0	x	Instruction Clock (FOSC/4)	Instruction Clock (FOSC/4)
1	1	x	Capacitive Sensing A Oscillator	Capacitive Sensing B Oscillator
1	0	0	External Clocking on T1CKI Pin	External Clocking on T3CKI Pin
1	0	1	Oscillator Circuit on T1OSI/ T1OSO Pins	Oscillator Circuit on T1OSI/ T1OSO Pins

13.6.7 TIMER1/3 GATE TOGGLE MODE

When Timer1/3 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1/3 gate signal, as opposed to the duration of a single level pulse.

The Timer1/3 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 13-4 for timing details.

Timer1/3 Gate Toggle mode is enabled by setting the TxGTM bit of the TxGCON register. When the TxGTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note:	Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

13.6.8 TIMER1/3 GATE SINGLE-PULSE MODE

When Timer1/3 Gate Single-Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer1/3 Gate Single-Pulse mode is first enabled by setting the TxGSPM bit in the TxGCON register. Next, the TxGGO/DONE bit in the TxGCON register must be set. The Timer1/3 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the TxGGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1/3 until the TxGGO/DONE bit is once again set in software.

Clearing the TxGSPM bit of the TxGCON register will also clear the TxGGO/DONE bit. See Figure 13-5 for timing details.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1/3 gate source to be measured. See Figure 13-6 for timing details.

13.6.9 TIMER1/3 GATE VALUE STATUS

When Timer1/3 gate value status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the TxGVAL bit in the TxGCON register. The TxGVAL bit is valid even when the Timer1/3 gate is not enabled (TMRxGE bit is cleared).

13.6.10 TIMER1/3 GATE EVENT INTERRUPT

When Timer1/3 gate event interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of TxGVAL occurs, the TMRxGIF flag bit in the PIRx register will be set. If the TMRxGIE bit in the PIEx register is set, then an interrupt will be recognized. See Table 13-7 for interrupt bit locations.

The TMRxGIF flag bit operates even when the Timer1/3 gate is not enabled (TMRxGE bit is cleared).

TABLE 13-7: TIMER1/3 INTERRUPT BIT LOCATIONS

	Timer1	Timer3
Interrupt Flag	TMR1IF bit in PIR1 register	TMR3IF bit in PIR2 register
Interrupt Enable	TMR1IE bit in PIE1 register	TMR3IE bit in PIE2 register
Gate Interrupt Flag	TMR1GIF bit in PIR1 register	TMR3GIF bit in PIR2 register
Gate Interrupt Enable	TMR1GIE bit in PIE1 register	TMR3GIE bit in PIE2 register

13.7 Timer1/3 Interrupt

The Timer1/3 register pair (TMRxH:TMRxL) increments to FFFFh and rolls over to 0000h. When Timer1/3 rolls over, the Timer1/3 interrupt flag bit of the PIRx register is set. See Table 13-7 for interrupt bit locations.

To enable the interrupt on rollover, you must set these bits:

- TMRxON bit of the TxCON register
- TMRxIE bit of the PIEx register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMRxIF bit in the Interrupt Service Routine.

Note:	The TMRxH:TMRxL register pair and the TMRxIF bit should be cleared before enabling interrupts.

16.4 Power Modes

The capacitive sensing oscillator can operate in one of seven different power modes. The power modes are separated into two ranges; the low range and the high range.

When the oscillator's low range is selected, the fixed internal voltage references of the capacitive sensing oscillator are being used. When the oscillator's high range is selected, the variable voltage references supplied by the FVR and DAC modules are being used. Selection between the voltage references is controlled by the CPSxRM bit of the CPSxCON0 register. See **Section 16.3 "Voltage References"** for more information.

Within each range there are three distinct power modes; Low, Medium and High. Current consumption is dependent upon the range and mode selected. Selecting power modes within each range is accomplished by configuring the CPSxRNG <1:0> bits in the CPSxCON0 register. See Table 16-2 for proper power mode selection.

The remaining mode is a Noise Detection mode that resides within the high range. The Noise Detection mode is unique in that it disables the sinking and sourcing of current on the analog pin but leaves the rest of the oscillator circuitry active. This reduces the oscillation frequency on the analog pin to zero and also greatly reduces the current consumed by the oscillator module.

When noise is introduced onto the pin, the oscillator is driven at the frequency determined by the noise. This produces a detectable signal at the comparator output, indicating the presence of activity on the pin.

Figure 16-2 shows a more detailed drawing of the current sources and comparators associated with the oscillator.

TABLE 16-2: POWER MODE SELECTION

CPSxRM	Range	CPSxRNG<1:0>	Mode	Nominal Current (1)
0	Low	00	Off	0.0 µA
		01	Low	0.1 µA
		10	Medium	1.2 µA
		11	High	18 µA
1	High	00	Noise Detection	0.0 µA
		01	Low	9 µA
		10	Medium	30 µA
		11	High	100 µA

Note: See **Section 25.0 "Electrical Specifications"** for more information.

16.5 Timer Resources

To measure the change in frequency of the capacitive sensing oscillator, a fixed time base is required. For the period of the fixed time base, the capacitive sensing oscillator is used to clock either TimerA/B or Timer1/3 (for CPSA/B, respectively). The frequency of the capacitive sensing oscillator is equal to the number of counts in the timer divided by the period of the fixed time base.

16.6 Fixed Time Base

To measure the frequency of the capacitive sensing oscillator, a fixed time base is required. Any timer resource or software loop can be used to establish the fixed time base. It is up to the end user to determine the method in which the fixed time base is generated.

Note: The fixed time base can not be generated by the timer resource that the capacitive sensing oscillator is clocking.

REGISTER 18-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN(1)	SYNC	—	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** AUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **Unimplemented:** Read as '0'

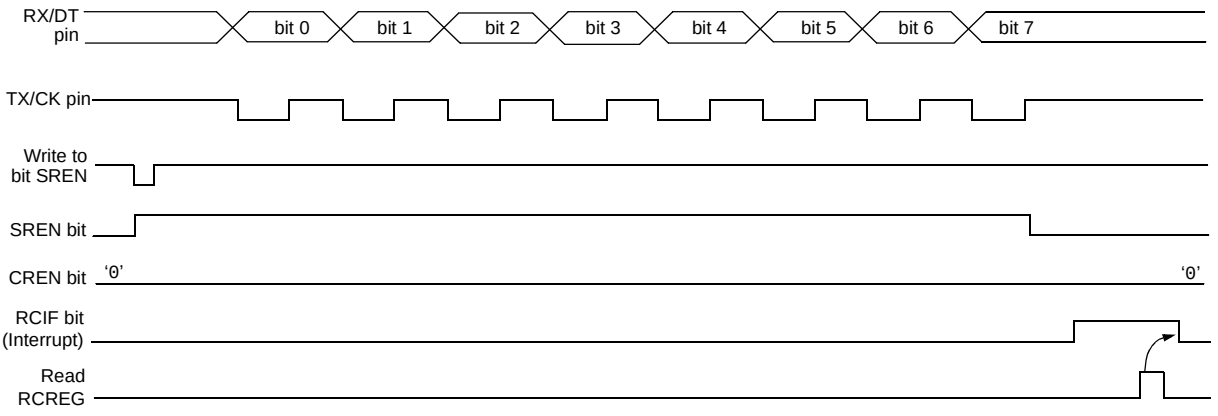
bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Synchronous mode.

FIGURE 18-8: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Synchronous Master mode with bit SREN = 1 and bit BRGH = 0.

TABLE 18-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSELC	ANSC7	ANSC6	ANSC5	—	—	ANSC2	ANSC1	ANSC0	111- -111	111- -111
INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000x
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
RCREG	AUSART Receive Data Register								0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	0000 000X
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010

Legend: x = unknown, - = unimplemented read as '0'. Shaded cells are not used for synchronous master reception.

18.3.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the AUSART for synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the AUSART.

18.3.2.1 AUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (refer to **Section 18.3.1.2 "Synchronous Master Transmission")**, except in the case of the Sleep mode.

19.1.1.3 Master Mode Setup

In Master mode, the data is transmitted/received as soon as the SSPBUF register is loaded with a byte value. If the master is only going to receive, SDO output could be disabled (programmed and used as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate.

When initializing SPI Master mode operation, several options need to be specified. This is accomplished by programming the appropriate control bits in the SSPCON and SSPSTAT registers. These control bits allow the following to be specified:

- SCK as clock output
- Idle state of SCK (CKP bit)
- Data input sample phase (SMP bit)
- Output data on rising/falling edge of SCK (CKE bit)
- Clock bit rate

In Master mode, the SPI clock rate (bit rate) is user selectable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 • TCY)
- FOSC/64 (or 16 • TCY)
- (Timer2 output)/2

This allows a maximum data rate of 5 Mbps (at FOSC = 20 MHz).

Figure 19-3 shows the waveforms for Master mode. The clock polarity is selected by appropriately programming the CKP bit of the SSPCON register. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The sample time of the input data is shown based on the state of the SMP bit and can occur at the middle or end of the data output time. The time when the SSPBUF is loaded with the received data is shown.

19.1.1.4 Sleep in Master Mode

In Master mode, all module clocks are halted and the transmission/reception will remain in their current state, paused, until the device wakes from Sleep. After the device wakes up from Sleep, the module will continue to transmit/receive data.

RLF **Rotate Left f through Carry**

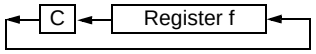
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction
```
REG1    =   1110 0110
C       =   0
```
After Instruction
```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

RRF **Rotate Right f through Carry**

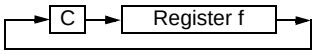
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

25.4 DC Characteristics: PIC16(L)F707-I/E (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
D130	EP	Cell Endurance	100	1k	—	E/W	Temperature during programming: 10°C ≤ TA ≤ 40°C
D131		VDD for Read	VMIN	—	—	V	
		Voltage on $\overline{\text{MCLR}}$/VPP during Erase/Program	8.0	—	9.0	V	Temperature during programming: 10°C ≤ TA ≤ 40°C
		VDD for Bulk Erase	2.7	3	—	V	Temperature during programming: 10°C ≤ TA ≤ 40°C
D132	VPEW	VDD for Write or Row Erase	2.7	—	—	V	VMIN = Minimum operating voltage VMAX = Maximum operating voltage
	IPPPGM	Current on $\overline{\text{MCLR}}$/VPP during Erase/Write	—	—	5.0	mA	Temperature during programming: 10°C ≤ TA ≤ 40°C
	IDDPGM	Current on VDD during Erase/ Write	—		5.0	mA	Temperature during programming: 10°C ≤ TA ≤ 40°C
D133	TPEW	Erase/Write cycle time	—		2.8	ms	Temperature during programming: 10°C ≤ TA ≤ 40°C
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
		VCAP Capacitor Charging					
D135		Charging current	—	200	—	µA	
D135A		Source/sink capability when charging complete	—	0.0	—	mA	

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

TABLE 25-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(2)	±2%	—	16.0	—	MHz	0°C ≤ TA ≤ +85°C, VDD ≥ 2.5V
			±5%	—	16.0	—	MHz	-40°C ≤ TA ≤ +125°C
OS08A	MFOSC	Internal Calibrated MFINTOSC Frequency(2)	±2%	—	500	—	kHz	0°C ≤ TA ≤ +85°C VDD ≥ 2.5V
			±5%	—	500	10	kHz	-40°C ≤ TA ≤ +125°C
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time	—	—	5	8	µs	
		MFINTOSC Wake-up from Sleep Start-up Time	—	—	20	30	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3: By design.

FIGURE 25-7: CLKOUT AND I/O TIMING

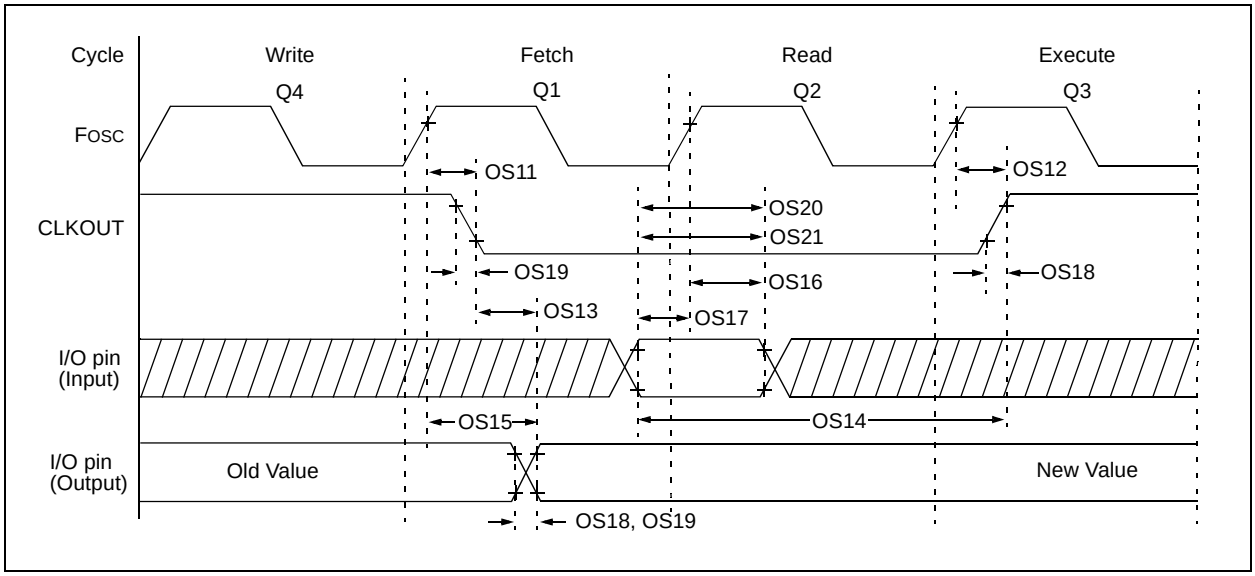


FIGURE 26-26: PIC16LF707 TYPICAL IDD vs. FOSC OVER VDD, INTOSC MODE

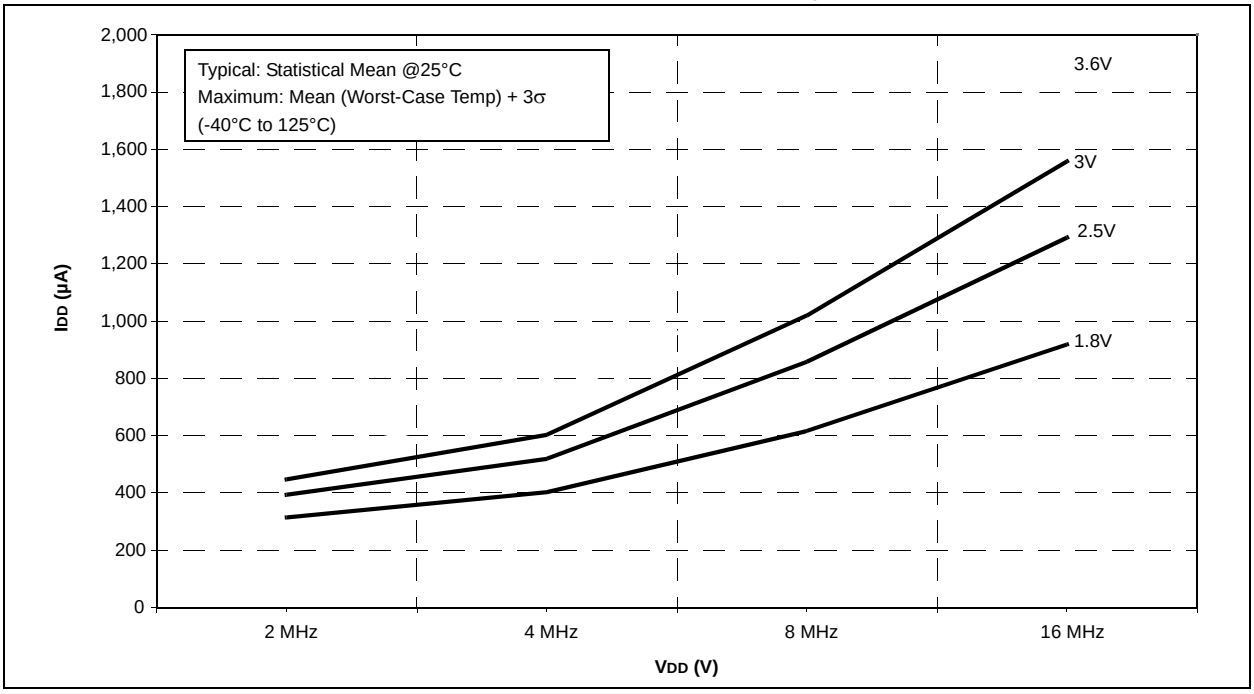
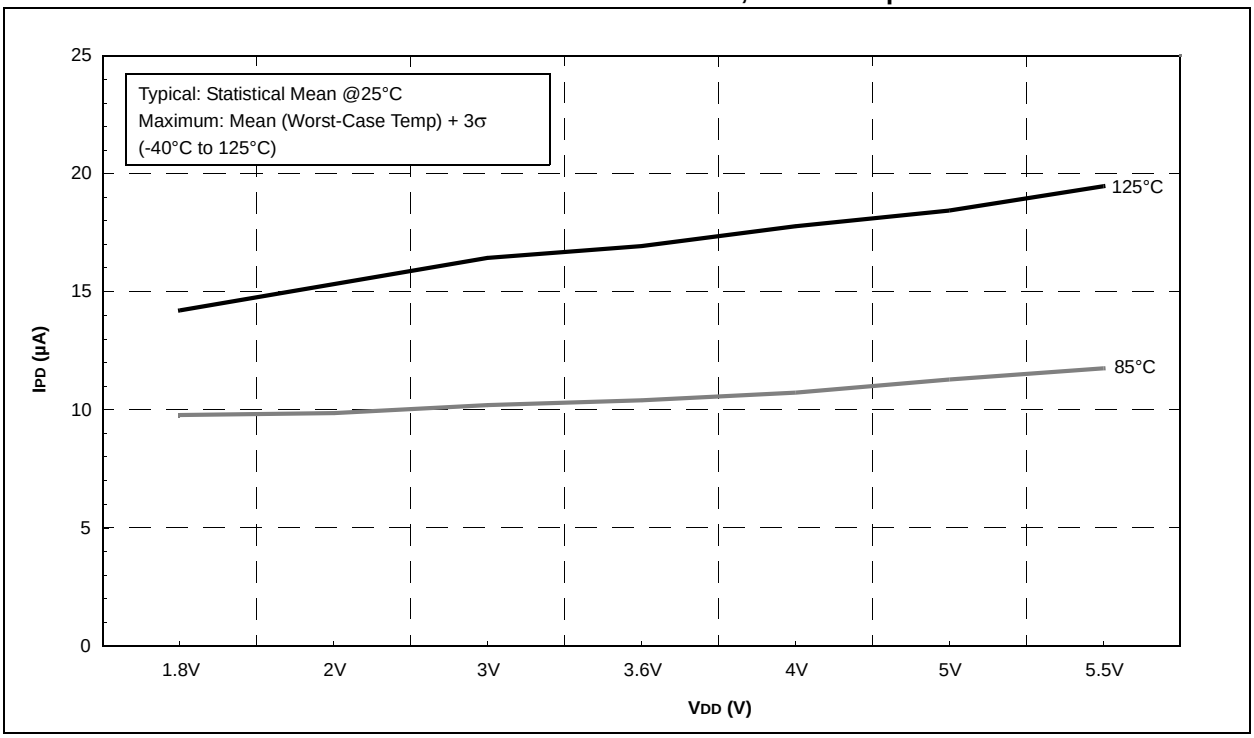


FIGURE 26-27: PIC16F707 MAXIMUM BASE IPD vs. VDD, VCAP = 0.1µF



PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX	XXX
Device	Tape and Reel Option	Temperature Range	Package	Pattern

Device:	PIC16F707, PIC16(L)F707(1)
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1)
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package:	MV = Micro Lead Frame (UQFN) ML = Micro Lead Frame (QFN) P = PDIP PT = TQFP (Thin Quad Flatpack)
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC16F707-E/P 301 = Extended Temp., PDIP package, QTP pattern #301

b) PIC16F707-I/ML = Industrial Temp., QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.