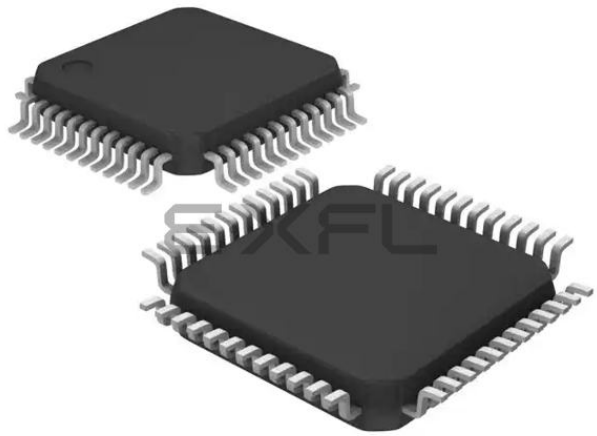

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 37 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103c8t6tr |

# List of tables

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

### 2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

### 2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

### 2.3.9 Power supply schemes

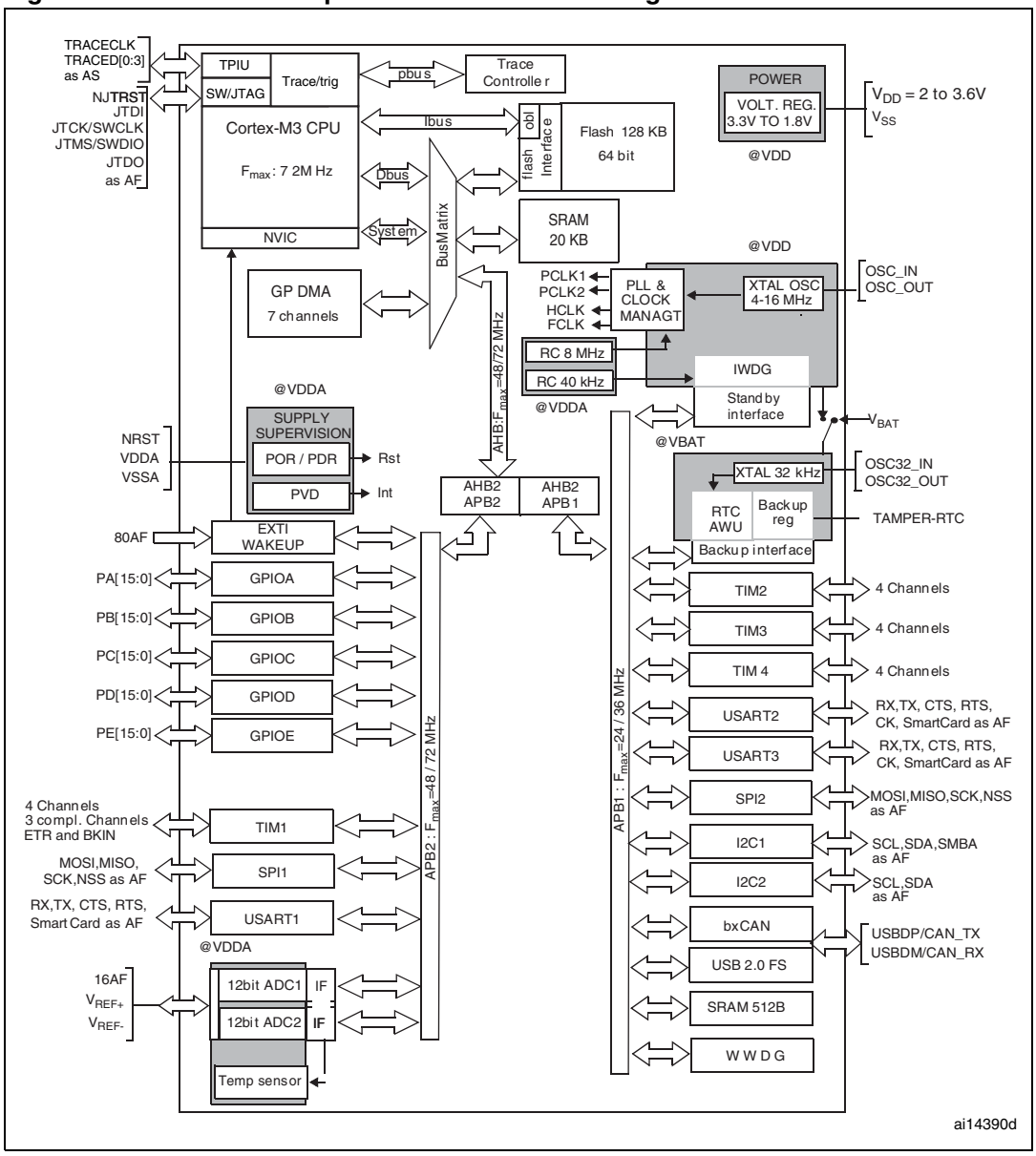
- $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to $V_{DDA}$ is 2.4 V when the ADC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 12: Power supply scheme*.

### 2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains

**Figure 1. STM32F103xx performance line block diagram**




1. $T_A$ = –40 °C to +105 °C (junction temperature up to 125 °C).
2. AF = alternate function on I/O port pin.

**Figure 6. STM32F103xx performance line TFBGA64 ballout**

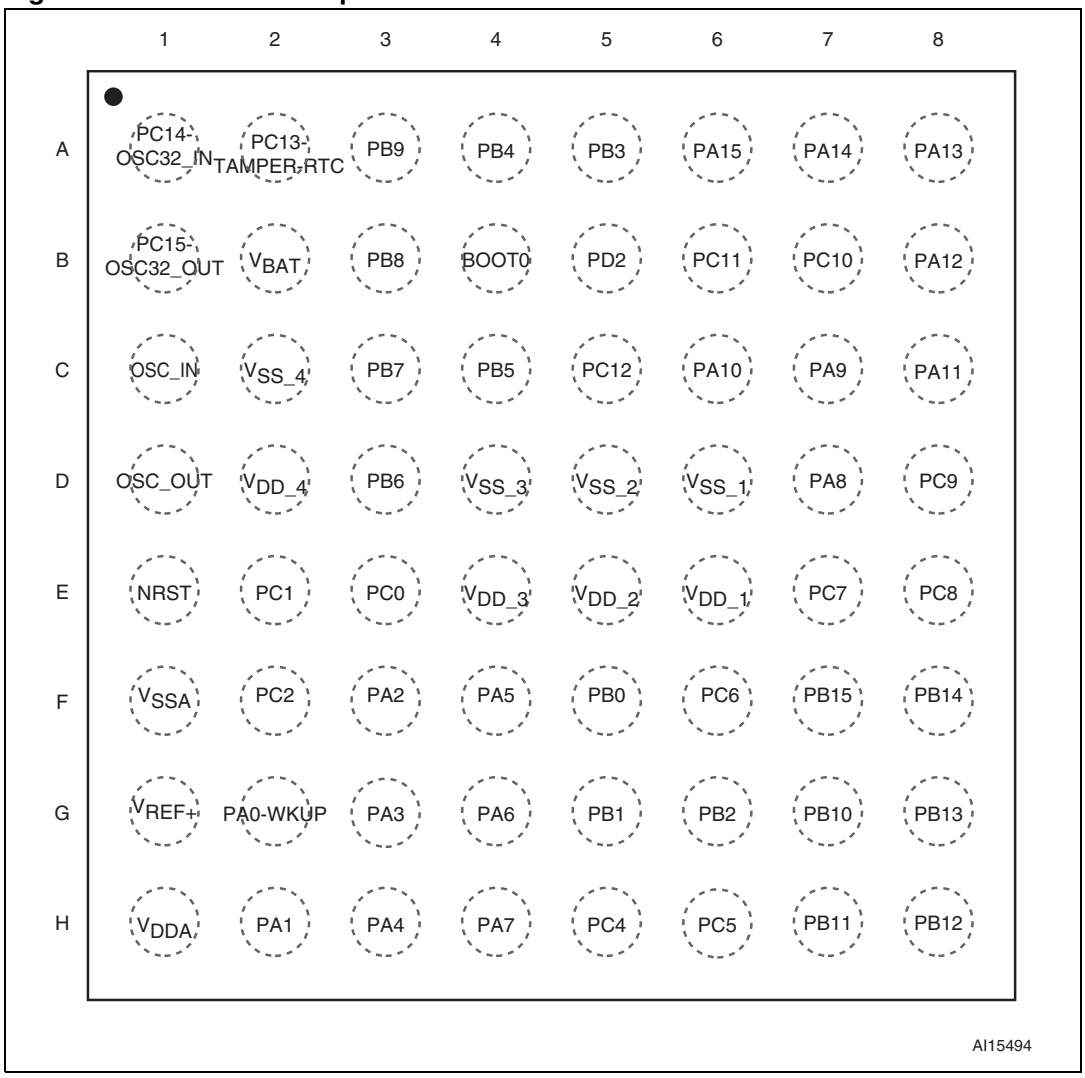


**Table 5. Medium-density STM32F103xx pin definitions**

| Pins | | | | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LFBGA100 | LQFP48 | TFBGA64 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| A3 | - | | - | 1 | - | PE2 | I/O | FT | PE2 | TRACECK | |
| B3 | - | | - | 2 | - | PE3 | I/O | FT | PE3 | TRACED0 | |
| C3 | - | | - | 3 | - | PE4 | I/O | FT | PE4 | TRACED1 | |
| D3 | - | | - | 4 | - | PE5 | I/O | FT | PE5 | TRACED2 | |
| E3 | - | | - | 5 | - | PE6 | I/O | FT | PE6 | TRACED3 | |
| B2 | 1 | B2 | 1 | 6 | - | $V_{BAT}$ | S | | $V_{BAT}$ | | |
| A2 | 2 | A2 | 2 | 7 | - | PC13-TAMPER-RTC(4) | I/O | | PC13(5) | TAMPER-RTC | |
| A1 | 3 | A1 | 3 | 8 | - | PC14-OSC32_IN(4) | I/O | | PC14(5) | OSC32_IN | |
| B1 | 4 | B1 | 4 | 9 | - | PC15-OSC32_OUT(4) | I/O | | PC15(5) | OSC32_OUT | |
| C2 | - | - | - | 10 | - | $V_{SS\_5}$ | S | | $V_{SS\_5}$ | | |
| D2 | - | - | - | 11 | - | $V_{DD\_5}$ | S | | $V_{DD\_5}$ | | |
| C1 | 5 | C1 | 5 | 12 | 2 | OSC_IN | I | | OSC_IN | | |
| D1 | 6 | D1 | 6 | 13 | 3 | OSC_OUT | O | | OSC_OUT | | |
| E1 | 7 | E1 | 7 | 14 | 4 | NRST | I/O | | NRST | | |
| F1 | - | E3 | 8 | 15 | - | PC0 | I/O | | PC0 | ADC12_IN10 | |
| F2 | - | E2 | 9 | 16 | - | PC1 | I/O | | PC1 | ADC12_IN11 | |
| E2 | - | F2 | 10 | 17 | - | PC2 | I/O | | PC2 | ADC12_IN12 | |
| F3 | - | -(6) | 11 | 18 | - | PC3 | I/O | | PC3 | ADC12_IN13 | |
| G1 | 8 | F1 | 12 | 19 | 5 | $V_{SSA}$ | S | | $V_{SSA}$ | | |
| H1 | - | - | - | 20 | - | $V_{REF-}$ | S | | $V_{REF-}$ | | |
| J1 | - | G1(6) | - | 21 | - | $V_{REF+}$ | S | | $V_{REF+}$ | | |
| K1 | 9 | H1 | 13 | 22 | 6 | $V_{DDA}$ | S | | $V_{DDA}$ | | |
| G2 | 10 | G2 | 14 | 23 | 7 | PA0-WKUP | I/O | | PA0 | WKUP/ USART2_CTS(7)/ ADC12_IN0/ TIM2_CH1_ETR(7) | |
| H2 | 11 | H2 | 15 | 24 | 8 | PA1 | I/O | | PA1 | USART2_RTS(7)/ ADC12_IN1/ TIM2_CH2(7) | |
| J2 | 12 | F3 | 16 | 25 | 9 | PA2 | I/O | | PA2 | USART2_TX(7)/ ADC12_IN2/ TIM2_CH3(7) | |

Table 5. Medium-density STM32F103xx pin definitions (continued)

| Pins | | | | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LFBGA100 | LQFP48 | TFBGA64 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| F7 | 24 | E6 | 32 | 50 | 19 | $V_{DD\_1}$ | S | | $V_{DD\_1}$ | | |
| K8 | 25 | H8 | 33 | 51 | - | PB12 | I/O | FT | PB12 | SPI2_NSS/ I2C2_SMBAI/ USART3_CK(7)/ TIM1_BKIN(7) | |
| J8 | 26 | G8 | 34 | 52 | - | PB13 | I/O | FT | PB13 | SPI2_SCK/ USART3_CTS(7)/ TIM1_CH1N (7) | |
| H8 | 27 | F8 | 35 | 53 | - | PB14 | I/O | FT | PB14 | SPI2_MISO/ USART3_RTS(7) TIM1_CH2N (7) | |
| G8 | 28 | F7 | 36 | 54 | - | PB15 | I/O | FT | PB15 | SPI2_MOSI/ TIM1_CH3N(7) | |
| K9 | - | - | - | 55 | - | PD8 | I/O | FT | PD8 | | USART3_TX |
| J9 | - | - | - | 56 | - | PD9 | I/O | FT | PD9 | | USART3_RX |
| H9 | - | - | - | 57 | - | PD10 | I/O | FT | PD10 | | USART3_CK |
| G9 | - | - | - | 58 | - | PD11 | I/O | FT | PD11 | | USART3_CTS |
| K10 | - | - | - | 59 | - | PD12 | I/O | FT | PD12 | | TIM4_CH1 / USART3_RTS |
| J10 | - | - | - | 60 | - | PD13 | I/O | FT | PD13 | | TIM4_CH2 |
| H10 | - | - | - | 61 | - | PD14 | I/O | FT | PD14 | | TIM4_CH3 |
| G10 | - | - | - | 62 | - | PD15 | I/O | FT | PD15 | | TIM4_CH4 |
| F10 | - | F6 | 37 | 63 | - | PC6 | I/O | FT | PC6 | | TIM3_CH1 |
| E10 | | E7 | 38 | 64 | - | PC7 | I/O | FT | PC7 | | TIM3_CH2 |
| F9 | | E8 | 39 | 65 | - | PC8 | I/O | FT | PC8 | | TIM3_CH3 |
| E9 | - | D8 | 40 | 66 | - | PC9 | I/O | FT | PC9 | | TIM3_CH4 |
| D9 | 29 | D7 | 41 | 67 | 20 | PA8 | I/O | FT | PA8 | USART1_CK/ TIM1_CH1(7)/MCO | |
| C9 | 30 | C7 | 42 | 68 | 21 | PA9 | I/O | FT | PA9 | USART1_TX(7)/ TIM1_CH2(7) | |
| D10 | 31 | C6 | 43 | 69 | 22 | PA10 | I/O | FT | PA10 | USART1_RX(7)/ TIM1_CH3(7) | |
| C10 | 32 | C8 | 44 | 70 | 23 | PA11 | I/O | FT | PA11 | USART1_CTS/ CANRX(7)/ USBDM TIM1_CH4(7) | |
| B10 | 33 | B8 | 45 | 71 | 24 | PA12 | I/O | FT | PA12 | USART1_RTS/ CANTX(7) //USBDP TIM1_ETR(7) | |

**Table 9. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $P_D$ | Power dissipation at $T_A$ = 85 °C for suffix 6 or $T_A$ = 105 °C for suffix 7(3) | LFBGA100 | | 454 | mW |
| | | LQFP100 | | 434 | |
| | | TFBGA64 | | 308 | |
| | | LQFP64 | | 444 | |
| | | LQFP48 | | 363 | |
| | | VFQFPN36 | | 1110 | |
| $T_A$ | Ambient temperature for 6 suffix version | Maximum power dissipation | –40 | 85 | °C |
| | | Low power dissipation(4) | –40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | 105 | °C |
| | | Low power dissipation(4) | –40 | 125 | |
| $T_J$ | Junction temperature range | 6 suffix version | –40 | 105 | °C |
| | | 7 suffix version | –40 | 125 | |

1. When the ADC is used, refer to *Table 45: ADC characteristics*.
2. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and operation.
3. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 81*).
4. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 81*).

### 5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for $T_A$.

**Table 10. Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

### 5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 12. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.16 | 1.20 | 1.26 | V |
| | | –40 °C < $T_A$ < +85 °C | 1.16 | 1.20 | 1.24 | V |
| $T_{S\_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | | | 5.1 | 17.1(2) | µs |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

### 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Figure 14. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled**

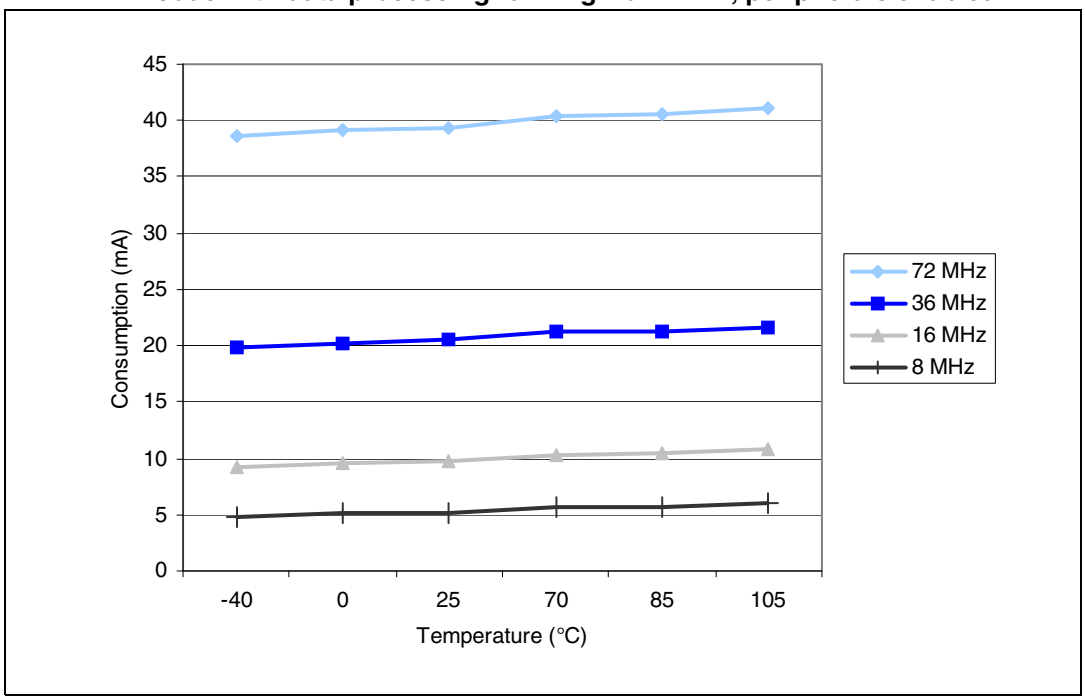



**Figure 15. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled**

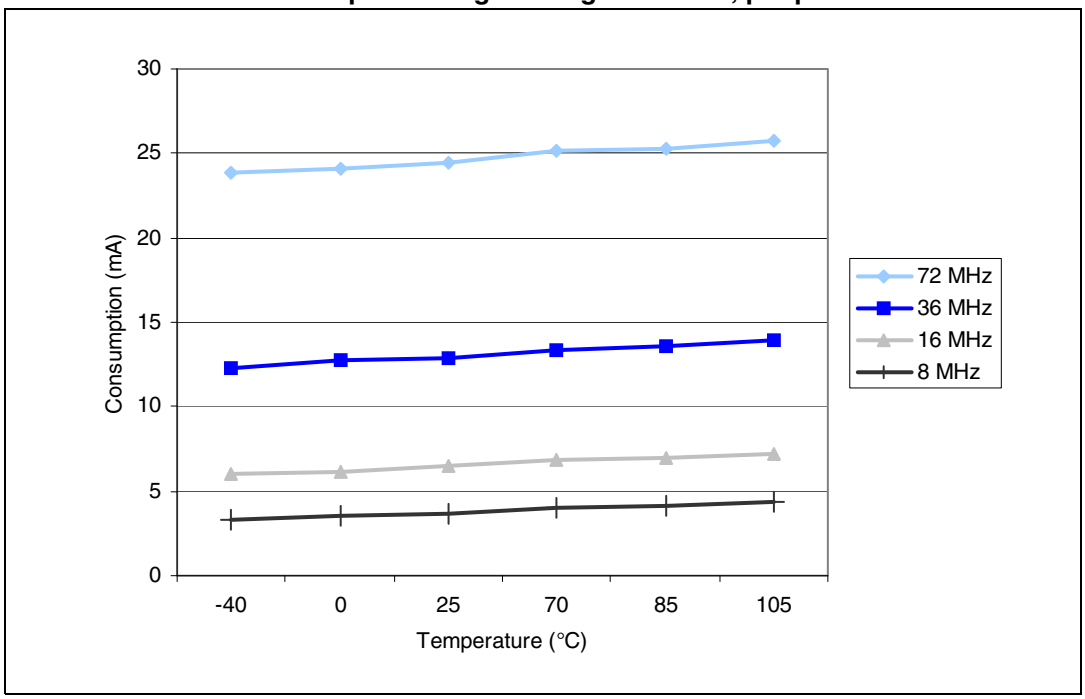


**Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2), all peripherals enabled | 72 MHz | 30 | 32 | mA |
| | | | 48 MHz | 20 | 20.5 | |
| | | | 36 MHz | 15.5 | 16 | |
| | | | 24 MHz | 11.5 | 12 | |
| | | | 16 MHz | 8.5 | 9 | |
| | | | 8 MHz | 5.5 | 6 | |
| | | External clock(2), all peripherals disabled | 72 MHz | 7.5 | 8 | |
| | | | 48 MHz | 6 | 6.5 | |
| | | | 36 MHz | 5 | 5.5 | |
| | | | 24 MHz | 4.5 | 5 | |
| | | | 16 MHz | 4 | 4.5 | |
| | | | 8 MHz | 3 | 4 | |

1. based on characterization, tested in production at $V_{DD\ max}$, $f_{HCLK}$ max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 6*

**Table 19. Peripheral current consumption(1)**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| APB1 | TIM2 | 1.2 | mA |
| | TIM3 | 1.2 | |
| | TIM4 | 0.9 | |
| | SPI2 | 0.2 | |
| | USART2 | 0.35 | |
| | USART3 | 0.35 | |
| | I2C1 | 0.39 | |
| | I2C2 | 0.39 | |
| | USB | 0.65 | |
| | CAN | 0.72 | |
| APB2 | GPIO A | 0.47 | mA |
| | GPIO B | 0.47 | |
| | GPIO C | 0.47 | |
| | GPIO D | 0.47 | |
| | GPIO E | 0.47 | |
| | ADC1(2) | 1.81 | |
| | ADC2 | 1.78 | |
| | TIM1 | 1.6 | |
| | SPI1 | 0.43 | |
| | USART1 | 0.85 | |

1. $f_{HCLK}$ = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. Specific conditions for ADC: $f_{HCLK}$ = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2/4}$, ADON bit in the ADC_CR2 register is set to 1.

## 5.3.6 External clock source characteristics

### High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

**Table 20. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency(1) | | 0 | 8 | 25 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 16 | | | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | | | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 45 | | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | | | ±1 | µA |

1. Guaranteed by design, not tested in production.

### Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

**Table 21. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User External clock source frequency(1) | | | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time(1) | | 450 | | | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | | | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | | | 5 | | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | 30 | | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | | | ±1 | µA |

**Table 26. Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $t_{WUSLEEP}$(1) | Wakeup from Sleep mode | Wakeup on HSI RC clock | 1.8 | µs |
| $t_{WUSTOP}$(1) | Wakeup from Stop mode (regulator in run mode) | HSI RC wakeup time = 2 µs | 3.6 | µs |
| | Wakeup from Stop mode (regulator in low power mode) | HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs | 5.4 | |
| $t_{WUSTDBY}$(1) | Wakeup from Standby mode | HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs | 50 | µs |

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

## 5.3.8 PLL characteristics

The parameters given in *Table 27* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 27. PLL characteristics**

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min(1) | Typ | Max(1) | |
| $f_{PLL\_IN}$ | PLL input clock(2) | | 1 | 8.0 | 25 | MHz |
| | PLL input clock duty cycle | | 40 | | 60 | % |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | | 16 | | 72 | MHz |
| $t_{LOCK}$ | PLL lock time | | | | 200 | µs |

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

## 5.3.9 Memory characteristics

### Flash memory

The characteristics are given at $T_A$ = –40 to 105 °C unless otherwise specified.

**Table 28. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming time | $T_A$ = –40 to +105 °C | 40 | 52.5 | 70 | µs |
| $t_{ERASE}$ | Page (1 KB) erase time | $T_A$ = –40 to +105 °C | 20 | | 40 | ms |
| $t_{ME}$ | Mass erase time | $T_A$ = –40 to +105 °C | 20 | | 40 | ms |

**Table 30. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 1000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 1000-4-4 | 4A |

## Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

## Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

**Table 31. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | | Unit |
|---|---|---|---|---|---|---|
| | | | | 8/48 MHz | 8/72 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, LQFP100 package compliant with SAE J 1752/3 | 0.1 to 30 MHz | 12 | 12 | dBµV |
| | | | 30 to 130 MHz | 22 | 19 | |
| | | | 130 MHz to 1GHz | 23 | 29 | |
| | | | SAE EMI Level | 4 | 4 | - |

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed $V_{OL}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 7*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 7*).

### Output voltage levels

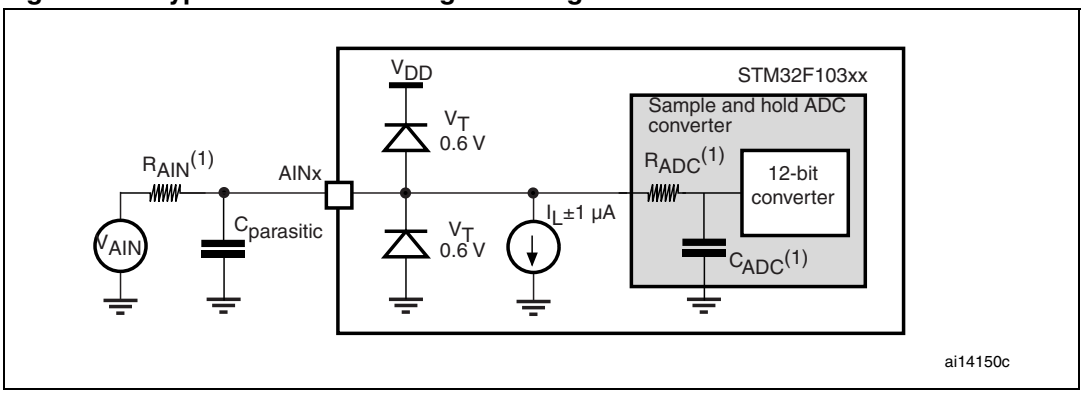
Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

**Table 35. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | TTL port<br>$I_{IO}$ = +8 mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$(2) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–0.4 | | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | CMOS port<br>$I_{IO}$ =+ 8mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$ (2) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | 2.4 | | |
| $V_{OL}$(1)(3) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO}$ = +20 mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 1.3 | V |
| $V_{OH}$(2)(3) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–1.3 | | |
| $V_{OL}$(1)(3) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO}$ = +6 mA<br>2 V < $V_{DD}$ < 2.7 V | | 0.4 | V |
| $V_{OH}$(2)(3) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–0.4 | | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
3. Based on characterization data, not tested in production.

**Figure 31. Typical connection diagram using the ADC**

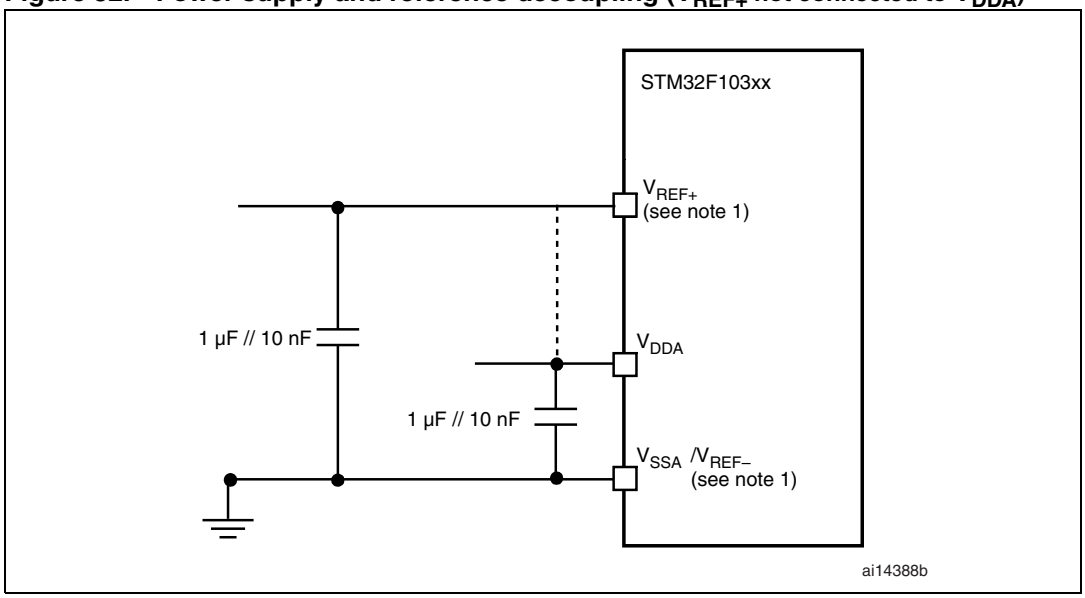



1. Refer to *Table 45* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 32* or *Figure 33*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 32. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**




1. $V_{REF+}$ and $V_{REF-}$ inputs are available only on 100-pin packages.

# 6 Package characteristics

## 6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 34. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package outline(1)**

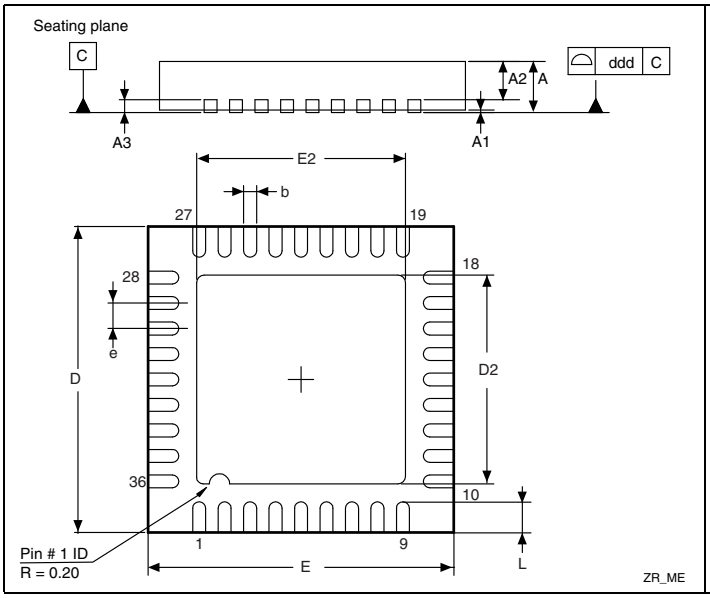
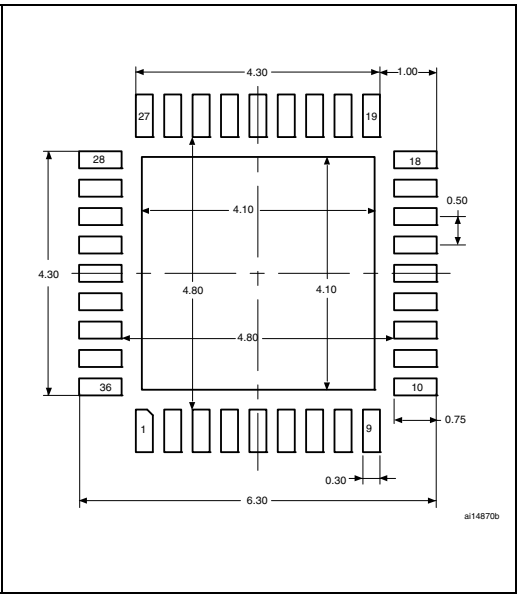



**Figure 35. Recommended footprint (dimensions in mm)(1)(2)(3)**




1. Drawing is not to scale.
2. The back-side pad is not internally connected to the $V_{SS}$ or $V_{DD}$ power pads.
3. There is an exposed die pad on the underside of the VFQFPN package. It should be soldered to the PCB. All leads should also be soldered to the PCB.

**Table 50. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | | 0.020 | 0.050 | | 0.0008 | 0.0020 |
| A2 | | 0.650 | 1.000 | | 0.0256 | 0.0394 |
| A3 | | 0.250 | | | 0.0098 | |
| b | 0.180 | 0.230 | 0.300 | 0.0071 | 0.0091 | 0.0118 |
| D | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| D2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| E | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| E2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| e | 0.450 | 0.500 | 0.550 | 0.0177 | 0.0197 | 0.0217 |
| L | 0.350 | 0.550 | 0.750 | 0.0138 | 0.0217 | 0.0295 |
| ddd | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 44. LQFP48, 48-pin low-profile quad flat package outline(1)**

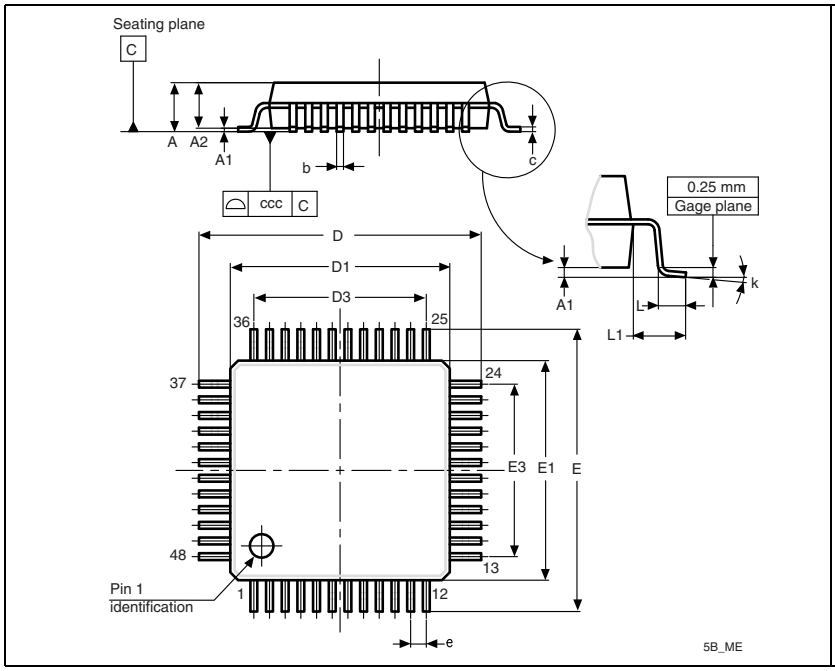
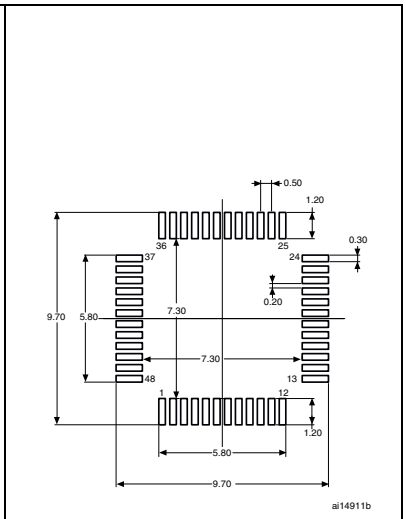



**Figure 45. Recommended footprint(1)(2)**




1. Drawing is not to scale.
2. Dimensions are in millimeters.

**Table 55. LQFP48, 48-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | | 0.050 | 0.150 | | 0.0020 | 0.0059 |
| A2 | 1.400 | 1.350 | 1.450 | 0.0551 | 0.0531 | 0.0571 |
| b | 0.220 | 0.170 | 0.270 | 0.0087 | 0.0067 | 0.0106 |
| c | | 0.090 | 0.200 | | 0.0035 | 0.0079 |
| D | 9.000 | 8.800 | 9.200 | 0.3543 | 0.3465 | 0.3622 |
| D1 | 7.000 | 6.800 | 7.200 | 0.2756 | 0.2677 | 0.2835 |
| D3 | 5.500 | | | 0.2165 | | |
| E | 9.000 | 8.800 | 9.200 | 0.3543 | 0.3465 | 0.3622 |
| E1 | 7.000 | 6.800 | 7.200 | 0.2756 | 0.2677 | 0.2835 |
| E3 | 5.500 | | | 0.2165 | | |
| e | 0.500 | | | 0.0197 | | |
| L | 0.600 | 0.450 | 0.750 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.000 | | | 0.0394 | | |
| k | 3.5° | 0° | 7° | 3.5° | 0° | 7° |
| ccc | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.