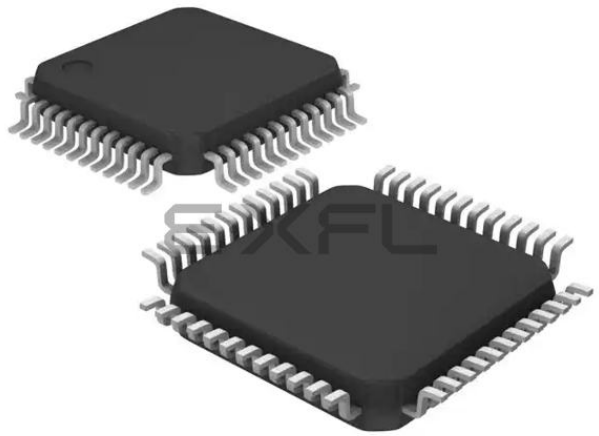

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103c8t7tr

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x8 and STM32F103xB medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F103x8 and STM32F103xB performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx medium-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.

2.2 Full compatibility throughout the family

The STM32F103xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x4 and STM32F103x6 are identified as low-density devices, the STM32F103x8 and STM32F103xB are referred to as medium-density devices, and the STM32F103xC, STM32F103xD and STM32F103xE are referred to as high-density devices.

Low- and high-density devices are an extension of the STM32F103x8/B devices, they are specified in the STM32F103x4/6 and STM32F103xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I^2S and DAC, while remaining fully compatible with the other members of the STM32F103xx family.

The STM32F103x4, STM32F103x6, STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for STM32F103x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F103xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

Table 3. STM32F103xx family

<table>
<tr><th rowspan="3">Pinout</th><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th>6 KB RAM</th><th>10 KB RAM</th><th>20 KB RAM</th><th>20 KB RAM</th><th>48 KB RAM</th><th>64 KB RAM</th><th>64 KB RAM</th></tr>
<tr><td>144</td><td></td><td></td><td></td><td></td><td colspan="3" rowspan="3">5 × USARTs
4 × 16-bit timers, 2 × basic timers
3 × SPIs, 2 × I^2Ss, 2 × I2Cs
USB, CAN, 2 × PWM timers
3 × ADCs, 1 × DAC, 1 × SDIO
FSMC (100 and 144 pins)</td></tr>
<tr><td>100</td><td></td><td></td><td colspan="2" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I^2Cs, USB, CAN, 1 × PWM timer
2 × ADC</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I^2C, USB, CAN, 1 × PWM timer
2 × ADCs</td><td colspan="3"></td></tr>
<tr><td>48</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>36</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6 or 7), the reference datasheet for electrical characteristics is that of the STM32F103x8/B medium-density devices.

2.3 Overview

2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Twenty Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F103xx performance line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.3.9 Power supply schemes

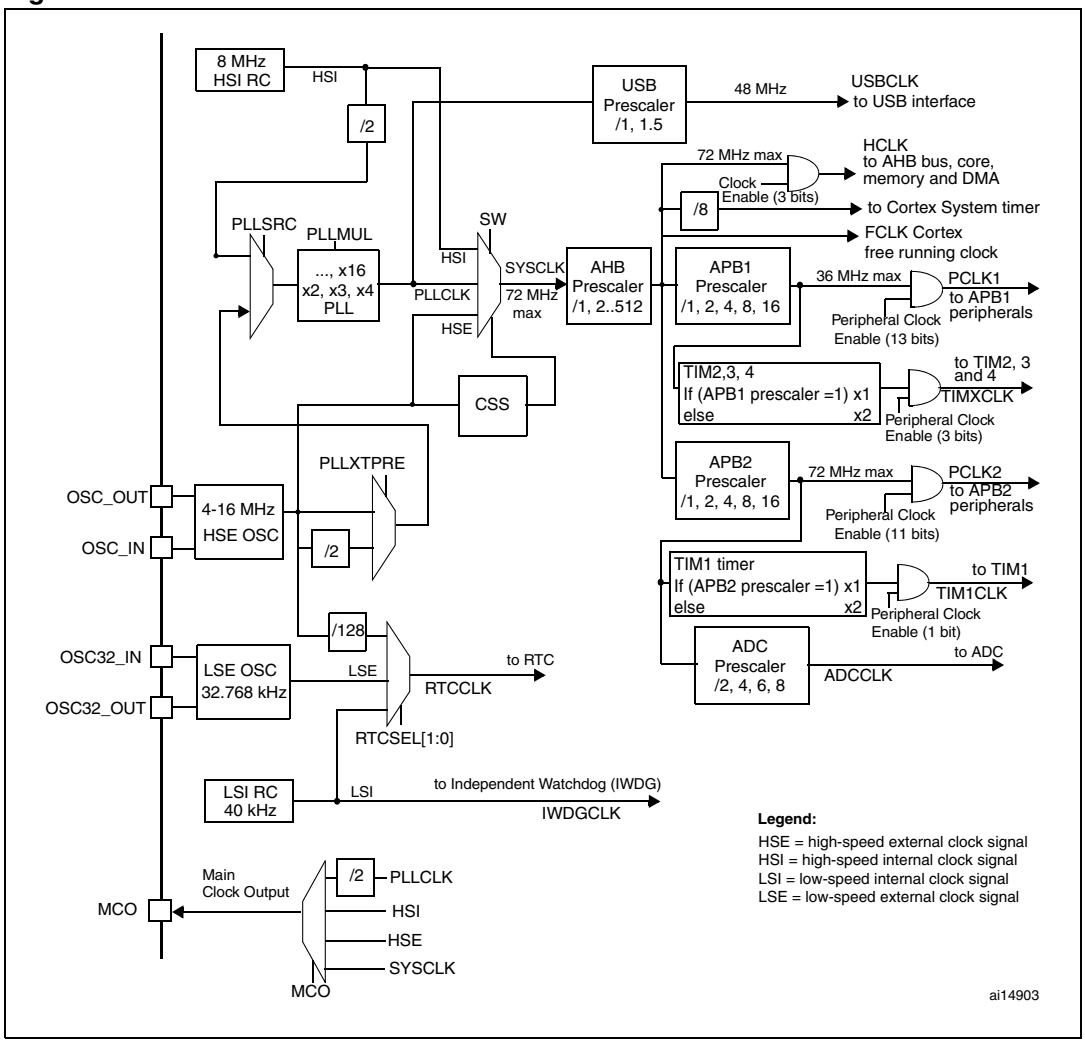
- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 12: Power supply scheme*.

2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 48 MHz or 72 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

Figure 4. STM32F103xx performance line LQFP100 pinout

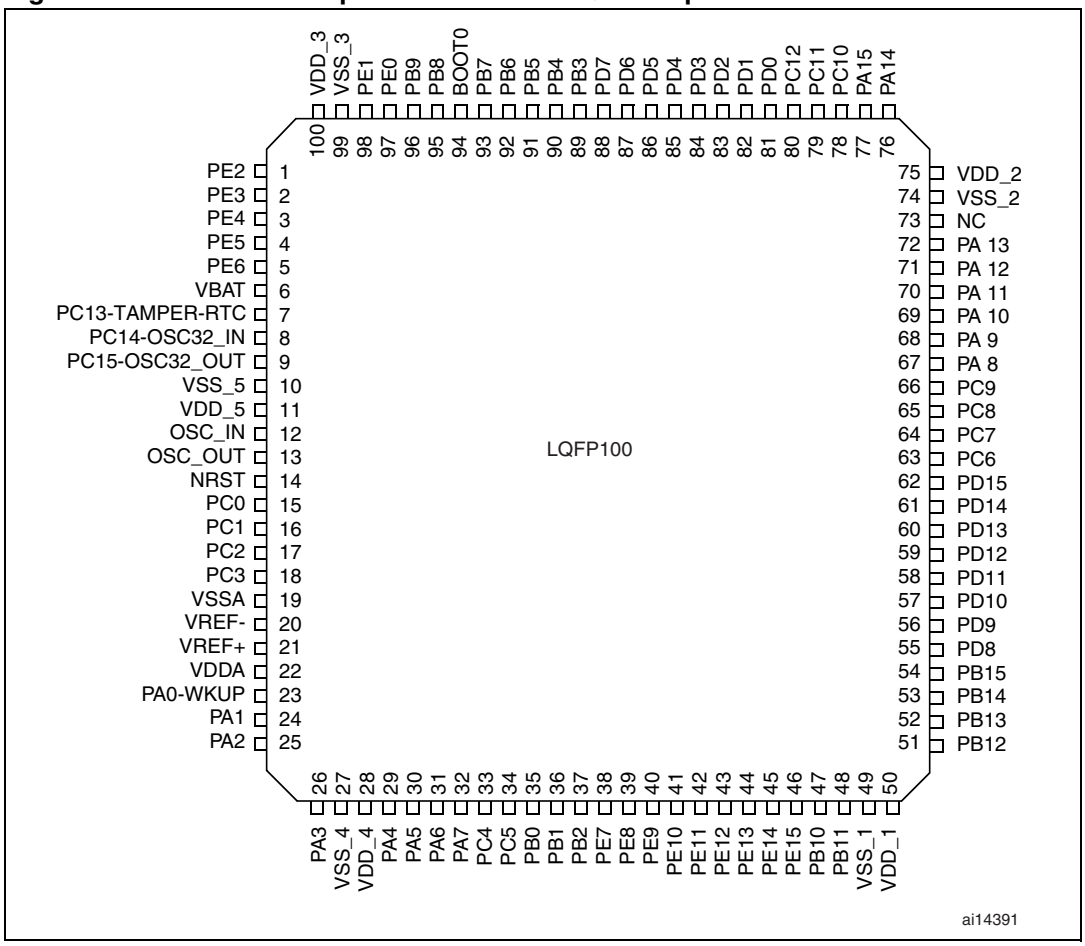


Figure 7. STM32F103xx performance line LQFP48 pinout

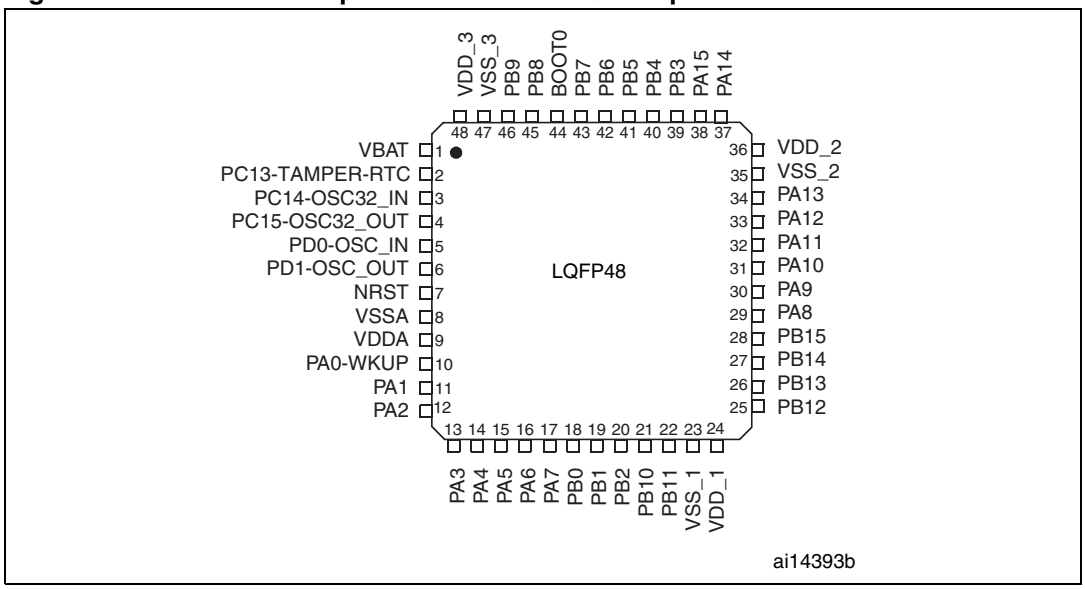


Figure 8. STM32F103xx Performance Line VFQFPN36 pinout

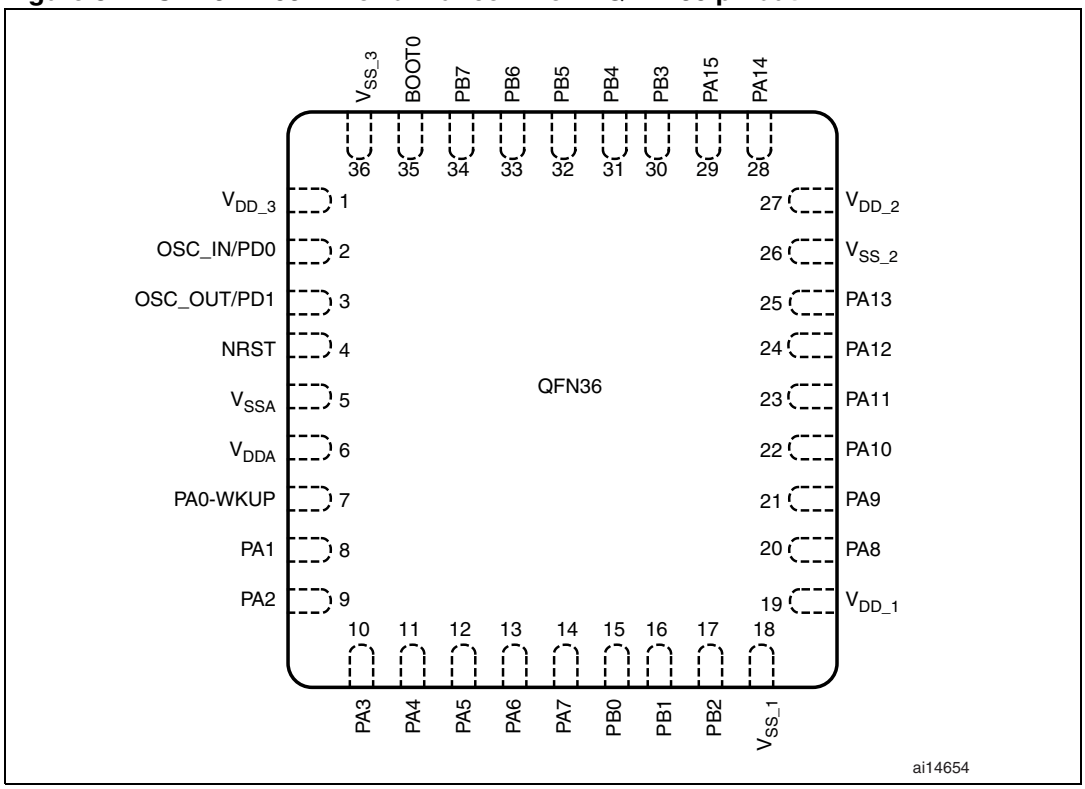


Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A10	34	A8	46	72	25	PA13	I/O	FT	JTMS/SWDIO		PA13
F8	-	-	-	73	-	Not connected					
E6	35	D5	47	74	26	V_{SS_2}	S		V_{SS_2}		
F6	36	E5	48	75	27	V_{DD_2}	S		V_{DD_2}		
A9	37	A7	49	76	28	PA14	I/O	FT	JTCK/SWCLK		PA14
A8	38	A6	50	77	29	PA15	I/O	FT	JTDI		TIM2_CH1_ETR/ PA15 /SPI1_NSS
B9	-	B7	51	78		PC10	I/O	FT	PC10		USART3_TX
B8	-	B6	52	79		PC11	I/O	FT	PC11		USART3_RX
C8	-	C5	53	80		PC12	I/O	FT	PC12		USART3_CK
D8	5	C1	5	81	2	PD0	I/O	FT	OSC_IN(8)		CANRX
E8	6	D1	6	82	3	PD1	I/O	FT	OSC_OUT(8)		CANTX
B7		B5	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	
C7	-	-	-	84	-	PD3	I/O	FT	PD3		USART2_CTS
D7	-	-	-	85	-	PD4	I/O	FT	PD4		USART2_RTS
B6	-	-	-	86	-	PD5	I/O	FT	PD5		USART2_TX
C6	-	-	-	87	-	PD6	I/O	FT	PD6		USART2_RX
D6	-	-	-	88	-	PD7	I/O	FT	PD7		USART2_CK
A7	39	A5	55	89	30	PB3	I/O	FT	JTDO		TIM2_CH2 / PB3 TRACESWO SPI1_SCK
A6	40	A4	56	90	31	PB4	I/O	FT	JNTRST		TIM3_CH1/ PB4/ SPI1_MISO
C5	41	C4	57	91	32	PB5	I/O		PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
B5	42	D3	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL(7)/ TIM4_CH1(7)	USART1_TX
A5	43	C3	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA(7)/ TIM4_CH2(7)	USART1_RX
D5	44	B4	60	94	35	BOOT0	I		BOOT0		
B4	45	B3	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3(7)	I2C1_SCL / CANRX
A4	46	A3	62	96	-	PB9	I/O	FT	PB9	TIM4_CH4(7)	I2C1_SDA/ CANTX

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
D4	-	-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR	
C4	-	-	-	98	-	PE1	I/O	FT	PE1		
E5	47	D4	63	99	36	V_{SS_3}	S		V_{SS_3}		
F5	48	E4	64	100	1	V_{DD_3}	S		V_{DD_3}		

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 10*.
4. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 is restricted: only one I/O at a time can be used as an output, the speed has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
8. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages, and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
   The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 6*

Table 19. Peripheral current consumption(1)

Peripheral		Typical consumption at 25 °C	Unit
APB1	TIM2	1.2	mA
	TIM3	1.2	
	TIM4	0.9	
	SPI2	0.2	
	USART2	0.35	
	USART3	0.35	
	I2C1	0.39	
	I2C2	0.39	
	USB	0.65	
	CAN	0.72	
APB2	GPIO A	0.47	mA
	GPIO B	0.47	
	GPIO C	0.47	
	GPIO D	0.47	
	GPIO E	0.47	
	ADC1(2)	1.81	
	ADC2	1.78	
	TIM1	1.6	
	SPI1	0.43	
	USART1	0.85	

1. f_{HCLK} = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. Specific conditions for ADC: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2/4}$, ADON bit in the ADC_CR2 register is set to 1.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C	–2	±1	2.5	%
		T_A = –10 to 85 °C	–1.5	±1	2.2	%
		T_A = 0 to 70 °C	–1.3	±1	2	%
		T_A = 25 °C	–1.1	±1	1.8	%
$t_{su(HSI)}$	HSI oscillator startup time		1		2	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	µA

1. Guaranteed by design, not tested in production.
2. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption		0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

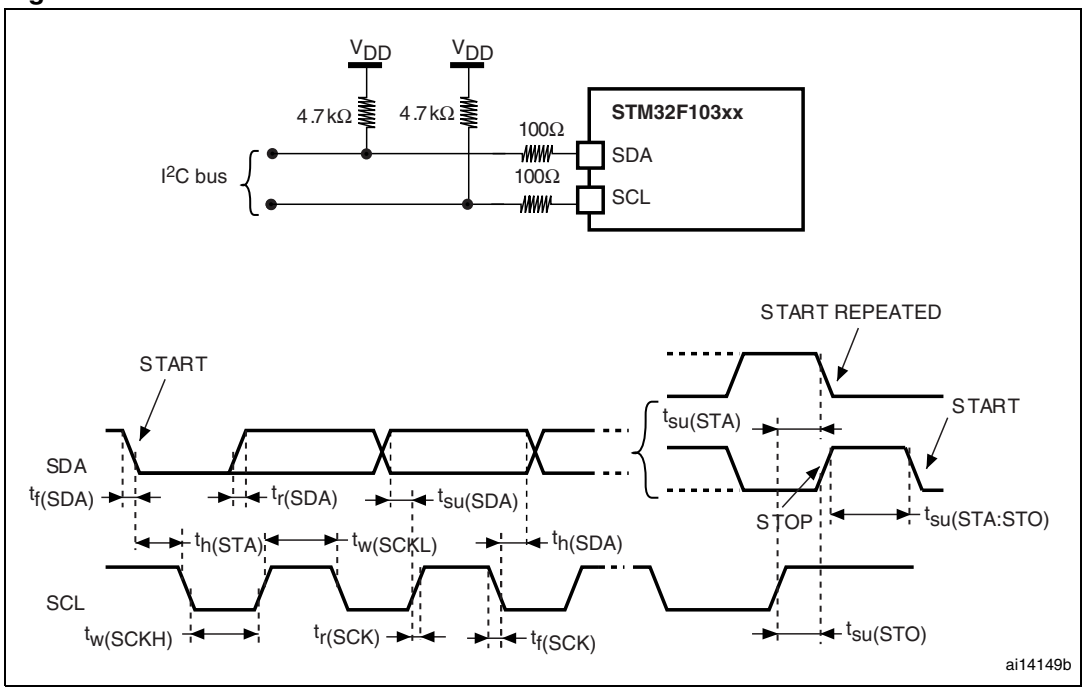
Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Figure 25. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

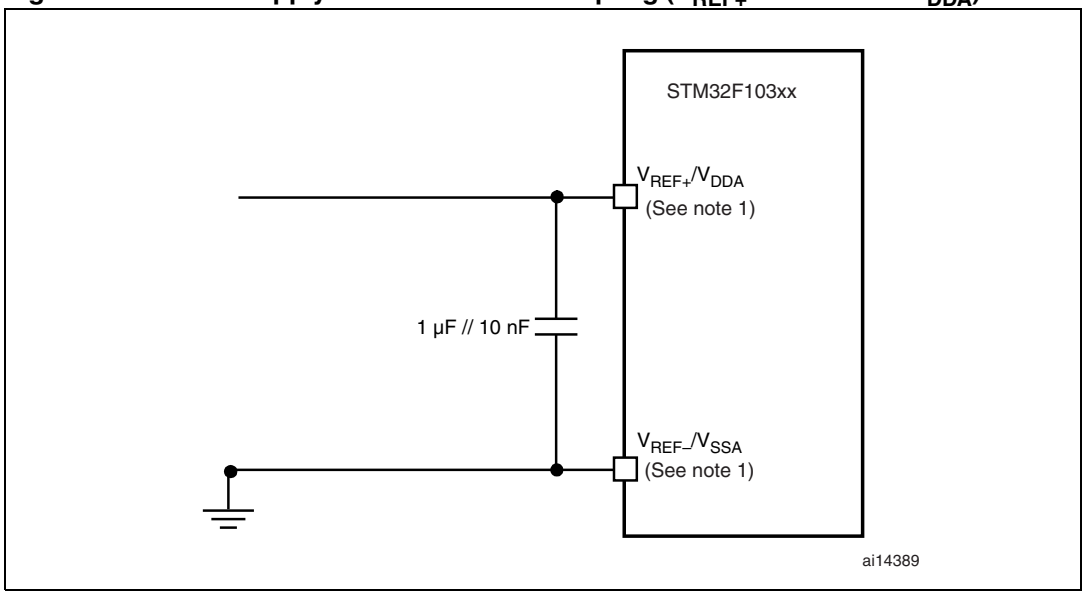
Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 t_{PCLK}		
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	73		
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (2)	Data input setup time Master mode	SPI1	1		
		SPI2	5		
$t_{su(SI)}$(2)	Data input setup time Slave mode		1		
$t_{h(MI)}$ (2)	Data input hold time Master mode	SPI1	1		
		SPI2	5		
$t_{h(SI)}$(2)	Data input hold time Slave mode		3		
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 24 MHz	0	4 t_{PCLK}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$(2)		Master mode (after enable edge)	4		

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 33. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

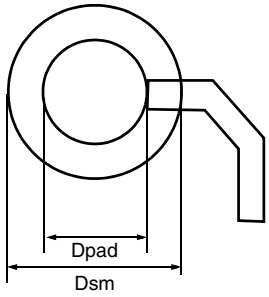
5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{25}[1]	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}[2]	Startup time	4		10	µs
T_{S_temp}[3][2]	ADC sampling time when reading the temperature			17.1	µs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Figure 37. Recommended PCB design rules (0.80/0.75 mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

Table 58. Document revision history (continued)

Date	Revision	Changes
22-Nov-2007	4	Document status promoted from preliminary data to datasheet. The STM32F103xx is USB certified. Small text changes. *Power supply schemes on page 13* modified. Number of communication peripherals corrected for STM32F103Tx and number of GPIOs corrected for LQFP package in *Table 2: STM32F103xx medium-density device features and peripheral counts*. Main function and default alternate function modified for PC14 and PC15 in, *Note 5* added and Remap column added in *Table 5: Medium-density STM32F103xx pin definitions*. V_{DD}–V_{SS} ratings and *Note 1* modified in *Table 6: Voltage characteristics*, *Note 1* modified in *Table 7: Current characteristics*. *Note 1* and *Note 2* added in *Table 11: Embedded reset and power control block characteristics*. I_{DD} value at 72 MHz with peripherals enabled modified in *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM*. I_{DD} value at 72 MHz with peripherals enabled modified in *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 41*. I_{DD_VBAT} typical value at 2.4 V modified and I_{DD_VBAT} maximum values added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. Note added in *Table 17 on page 44* and *Table 18 on page 45*. ADC1 and ADC2 consumption and notes modified in *Table 19: Peripheral current consumption*. $t_{SU(HSE)}$ and $t_{SU(LSE)}$ conditions modified in *Table 22* and *Table 23*, respectively. Maximum values removed from *Table 26: Low-power mode wakeup timings*. t_{RET} conditions modified in *Table 29: Flash memory endurance and data retention*. *Figure 12: Power supply scheme* corrected. *Figure 17: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at V_{DD} = 3.3 V and 3.6 V* added. Note removed below *Figure 26: SPI timing diagram - slave mode and CPHA = 0*. Note added below *Figure 27: SPI timing diagram - slave mode and CPHA = 1(1)*. Details on unused pins removed from *General input/output characteristics on page 56*. *Table 41: SPI characteristics* updated. *Table 42: USB startup time* added. V_{AIN}, $t_{lat\ and}$ t_{latr} modified, note added and I_{lkg} removed in *Table 45: ADC characteristics*. Test conditions modified and note added in *Table 48: ADC accuracy*. Note added below *Table 46* and *Table 49*. Inch values corrected in *Table 52: LQPF100, 100-pin low-profile quad flat package mechanical data*, *Table 53: LQFP64, 64-pin low-profile quad flat package mechanical data* and *Table 55: LQFP48, 48-pin low-profile quad flat package mechanical data*. Θ_{JA}value for VFQFPN36 package added in *Table 56: Package thermal characteristics*. Order codes replaced by *Section 7: Ordering information scheme*. MCU ‘s operating conditions modified in *Typical current consumption on page 44*. Avg_Slope and V_{25} modified in *Table 49: TS characteristics*. *I2C interface characteristics on page 61* modified. Impedance size specified in *A.4: Voltage glitch on ADC input 0 on page 81*.

Table 58. Document revision history (continued)

Date	Revision	Changes
14-Mar-2008	5	*Figure 2: Clock tree on page 20* added. Maximum T_J value given in *Table 8: Thermal characteristics on page 35*. CRC feature added (see *CRC (cyclic redundancy check) calculation unit on page 9* and *Figure 9: Memory map on page 31* for address). I_{DD} modified in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. ACC_{HSI} modified in *Table 24: HSI oscillator characteristics on page 51*, note 2 removed. P_D, T_A and T_J added, t_{prog} values modified and t_{prog} description clarified in *Table 28: Flash memory characteristics on page 52*. t_{RET} modified in *Table 29: Flash memory endurance and data retention*. $V_{NF(NRST)}$ unit corrected in *Table 37: NRST pin characteristics on page 59*. *Table 41: SPI characteristics on page 63* modified. I_{VREF} added to *Table 45: ADC characteristics on page 67*. *Table 47: ADC accuracy - limited test conditions* added. *Table 48: ADC accuracy* modified. LQFP100 package specifications updated (see *Section 6: Package characteristics on page 72*). Recommended LQFP100, LQFP 64, LQFP48 and VFQFPN36 footprints added (see *Figure 39*, *Figure 41*, *Figure 45* and *Figure 35*). *Section 6.2: Thermal characteristics on page 81* modified, *Section 6.2.1* and *Section 6.2.2* added. *Appendix A: Important notes on page 81* removed.
21-Mar-2008	6	Small text changes. *Figure 9: Memory map* clarified. In *Table 29: Flash memory endurance and data retention*: – N_{END} tested over the whole temperature range – cycling conditions specified for t_{RET} – t_{RET} min modified at T_A = 55 °C V_{25}, Avg_Slope and T_L modified in *Table 49: TS characteristics*. CRC feature removed.
22-May-2008	7	CRC feature added back. Small text changes. *Section 1: Introduction* modified. *Section 2.2: Full compatibility throughout the family* added. I_{DD} at T_A max = 105 °C added to *Table 16: Typical and maximum current consumptions in Stop and Standby modes on page 42*. I_{DD_VBAT} removed from *Table 21: Typical current consumption in Standby mode on page 47*. Values added to *Table 40: SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V) on page 62*. *Figure 26: SPI timing diagram - slave mode and CPHA = 0 on page 64* modified. *Equation 1* corrected. t_{RET} at T_A = 105 °C modified in *Table 29: Flash memory endurance and data retention on page 53*. V_{USB} added to *Table 43: USB DC electrical characteristics on page 66*. *Figure 46: LQFP100 P_D max vs. T_A on page 83* modified. Axx option added to *Table 57: Ordering information scheme on page 84*.

Table 58. Document revision history (continued)

Date	Revision	Changes
23-Apr-2009	10	I/O information clarified *on page 1*. *Figure 3: STM32F103xx performance line LFBGA100 ballout* modified. *Figure 9: Memory map* modified. *Table 4: Timer feature comparison* added. PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column in *Table 5: Medium-density STM32F103xx pin definitions*. P_D for LFBGA100 corrected in *Table 9: General operating conditions*. Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified. *Figure 17* shows a typical curve (title modified). ACC_{HSI} max values modified in *Table 24: HSI oscillator characteristics*. TFBGA64 package added (see *Table 54* and *Table 42*). Small text changes.