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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103cbt7

2.3 Overview

2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Twenty Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F103xx performance line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

Figure 4. STM32F103xx performance line LQFP100 pinout

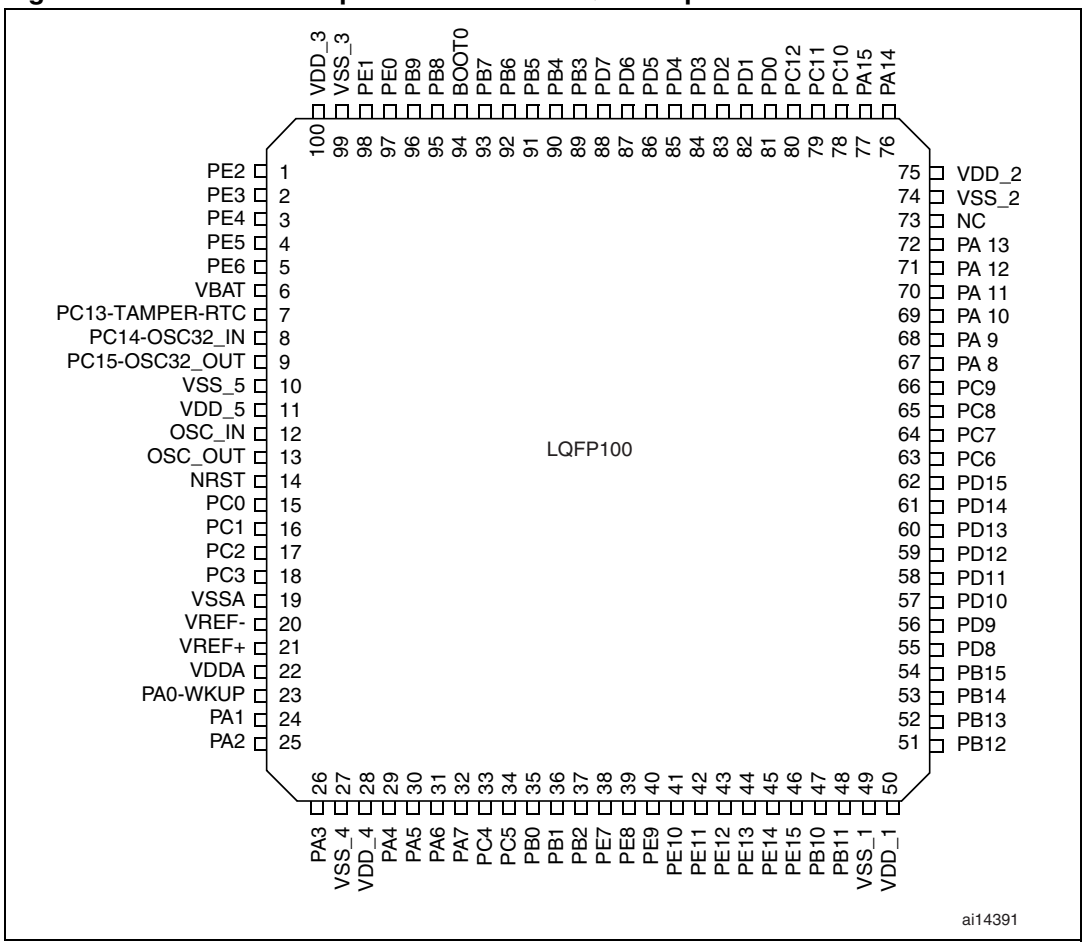


Table 5. Medium-density STM32F103xx pin definitions

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A3	-		-	1	-	PE2	I/O	FT	PE2	TRACECK	
B3	-		-	2	-	PE3	I/O	FT	PE3	TRACED0	
C3	-		-	3	-	PE4	I/O	FT	PE4	TRACED1	
D3	-		-	4	-	PE5	I/O	FT	PE5	TRACED2	
E3	-		-	5	-	PE6	I/O	FT	PE6	TRACED3	
B2	1	B2	1	6	-	V_{BAT}	S		V_{BAT}		
A2	2	A2	2	7	-	PC13-TAMPER-RTC(4)	I/O		PC13(5)	TAMPER-RTC	
A1	3	A1	3	8	-	PC14-OSC32_IN(4)	I/O		PC14(5)	OSC32_IN	
B1	4	B1	4	9	-	PC15-OSC32_OUT(4)	I/O		PC15(5)	OSC32_OUT	
C2	-	-	-	10	-	V_{SS_5}	S		V_{SS_5}		
D2	-	-	-	11	-	V_{DD_5}	S		V_{DD_5}		
C1	5	C1	5	12	2	OSC_IN	I		OSC_IN		
D1	6	D1	6	13	3	OSC_OUT	O		OSC_OUT		
E1	7	E1	7	14	4	NRST	I/O		NRST		
F1	-	E3	8	15	-	PC0	I/O		PC0	ADC12_IN10	
F2	-	E2	9	16	-	PC1	I/O		PC1	ADC12_IN11	
E2	-	F2	10	17	-	PC2	I/O		PC2	ADC12_IN12	
F3	-	-(6)	11	18	-	PC3	I/O		PC3	ADC12_IN13	
G1	8	F1	12	19	5	V_{SSA}	S		V_{SSA}		
H1	-	-	-	20	-	V_{REF-}	S		V_{REF-}		
J1	-	G1(6)	-	21	-	V_{REF+}	S		V_{REF+}		
K1	9	H1	13	22	6	V_{DDA}	S		V_{DDA}		
G2	10	G2	14	23	7	PA0-WKUP	I/O		PA0	WKUP/ USART2_CTS(7)/ ADC12_IN0/ TIM2_CH1_ETR(7)	
H2	11	H2	15	24	8	PA1	I/O		PA1	USART2_RTS(7)/ ADC12_IN1/ TIM2_CH2(7)	
J2	12	F3	16	25	9	PA2	I/O		PA2	USART2_TX(7)/ ADC12_IN2/ TIM2_CH3(7)	

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
K2	13	G3	17	26	10	PA3	I/O		PA3	USART2_RX(7)/ ADC12_IN3/ TIM2_CH4(7)	
E4	-	C2	18	27	-	V_{SS_4}	S		V_{SS_4}		
F4	-	D2	19	28	-	V_{DD_4}	S		V_{DD_4}		
G3	14	H3	20	29	11	PA4	I/O		PA4	SPI1_NSS(7)/ USART2_CK(7)/ ADC12_IN4	
H3	15	F4	21	30	12	PA5	I/O		PA5	SPI1_SCK(7)/ ADC12_IN5	
J3	16	G4	22	31	13	PA6	I/O		PA6	SPI1_MISO(7)/ ADC12_IN6/ TIM3_CH1(7)	TIM1_BKIN
K3	17	H4	23	32	14	PA7	I/O		PA7	SPI1_MOSI(7)/ ADC12_IN7/ TIM3_CH2(7)	TIM1_CH1N
G4	-	H5	24	33		PC4	I/O		PC4	ADC12_IN14	
H4	-	H6	25	34		PC5	I/O		PC5	ADC12_IN15	
J4	18	F5	26	35	15	PB0	I/O		PB0	ADC12_IN8/ TIM3_CH3(7)	TIM1_CH2N
K4	19	G5	27	36	16	PB1	I/O		PB1	ADC12_IN9/ TIM3_CH4(7)	TIM1_CH3N
G5	20	G6	28	37	17	PB2	I/O	FT	PB2/BOOT1		
H5	-	-	-	38	-	PE7	I/O	FT	PE7		TIM1_ETR
J5	-	-	-	39	-	PE8	I/O	FT	PE8		TIM1_CH1N
K5	-	-	-	40	-	PE9	I/O	FT	PE9		TIM1_CH1
G6	-	-	-	41	-	PE10	I/O	FT	PE10		TIM1_CH2N
H6	-	-	-	42	-	PE11	I/O	FT	PE11		TIM1_CH2
J6	-	-	-	43	-	PE12	I/O	FT	PE12		TIM1_CH3N
K6	-	-	-	44	-	PE13	I/O	FT	PE13		TIM1_CH3
G7	-	-	-	45	-	PE14	I/O	FT	PE14		TIM1_CH4
H7	-	-	-	46	-	PE15	I/O	FT	PE15		TIM1_BKIN
J7	21	G7	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(7)	TIM2_CH3
K7	22	H7	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(7)	TIM2_CH4
E7	23	D6	31	49	18	V_{SS_1}	S		V_{SS_1}		

5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage			5.1	17.1(2)	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	36	27	mA
			48 MHz	24.2	18.6	
			36 MHz	19	14.8	
			24 MHz	12.9	10.1	
			16 MHz	9.3	7.4	
			8 MHz	5.5	4.6	
			4 MHz	3.3	2.8	
			2 MHz	2.2	1.9	
			1 MHz	1.6	1.45	
			500 kHz	1.3	1.25	
			125 kHz	1.08	1.06	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	31.4	23.9	mA
			48 MHz	23.5	17.9	
			36 MHz	18.3	14.1	
			24 MHz	12.2	9.5	
			16 MHz	8.5	6.8	
			8 MHz	4.9	4	
			4 MHz	2.7	2.2	
			2 MHz	1.6	1.4	
			1 MHz	1.02	0.9	
			500 kHz	0.73	0.67	
			125 kHz	0.5	0.48	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	Wakeup on HSI RC clock	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 µs	3.6	µs
	Wakeup from Stop mode (regulator in low power mode)	HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs	50	µs

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 27. PLL characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)		1	8.0	25	MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock		16		72	MHz
t_{LOCK}	PLL lock time				200	µs

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 28. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20		40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20		40	ms

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 32. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 33. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

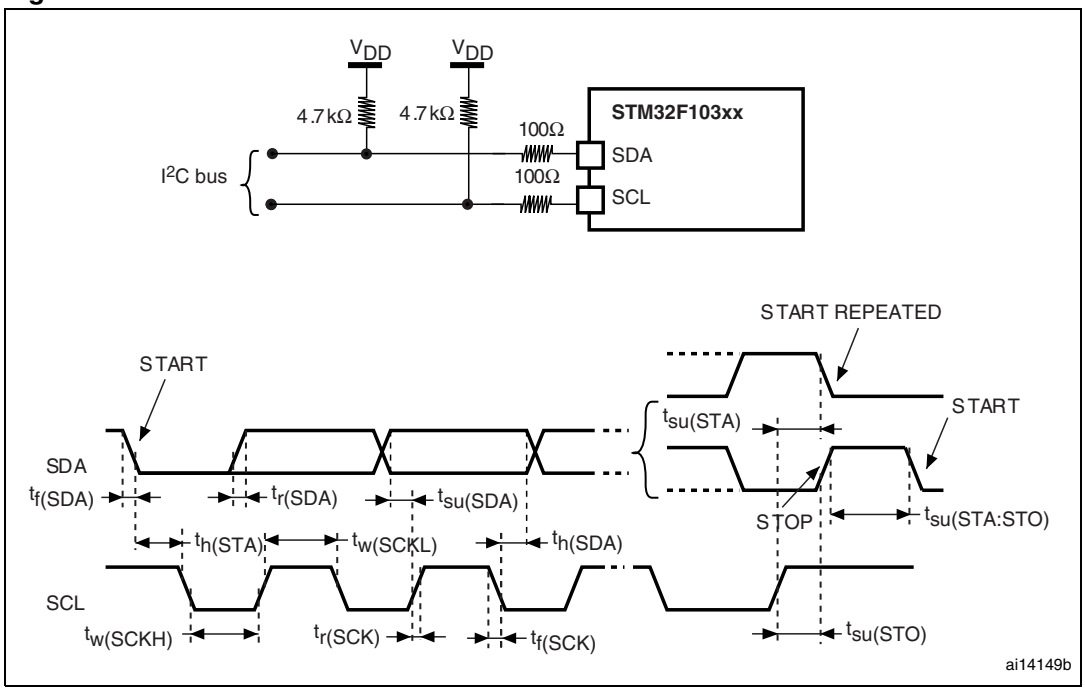
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL ports	–0.5		0.8	V
V_{IH}	Standard IO input high level voltage		2		V_{DD}+0.5	
	IO FT(1) input high level voltage		2		5.5V	
V_{IL}	Input low level voltage	CMOS ports	–0.5		0.35 V_{DD}	V
V_{IH}	Input high level voltage		0.65 V_{DD}		V_{DD}+0.5	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)		200			mV
	IO FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)			mV
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os			±1	µA
		V_{IN}= 5 V I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = Five-volt tolerant.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required), their characteristics consider the most strict CMOS-technology or TTL parameters:

- For V_{IH}:
  - if V_{DD} is in the [2.00 V - 3.08 V] range: CMOS characteristics but TTL included
  - if V_{DD} is in the [3.08 V - 3.60 V] range: TTL characteristics but CMOS included
- For V_{IL}:
  - if V_{DD} is in the [2.00 V - 2.28 V] range: TTL characteristics but CMOS included
  - if V_{DD} is in the [2.28 V - 3.60 V] range: CMOS characteristics but TTL included

Figure 25. I²C bus AC waveforms and measurement circuit



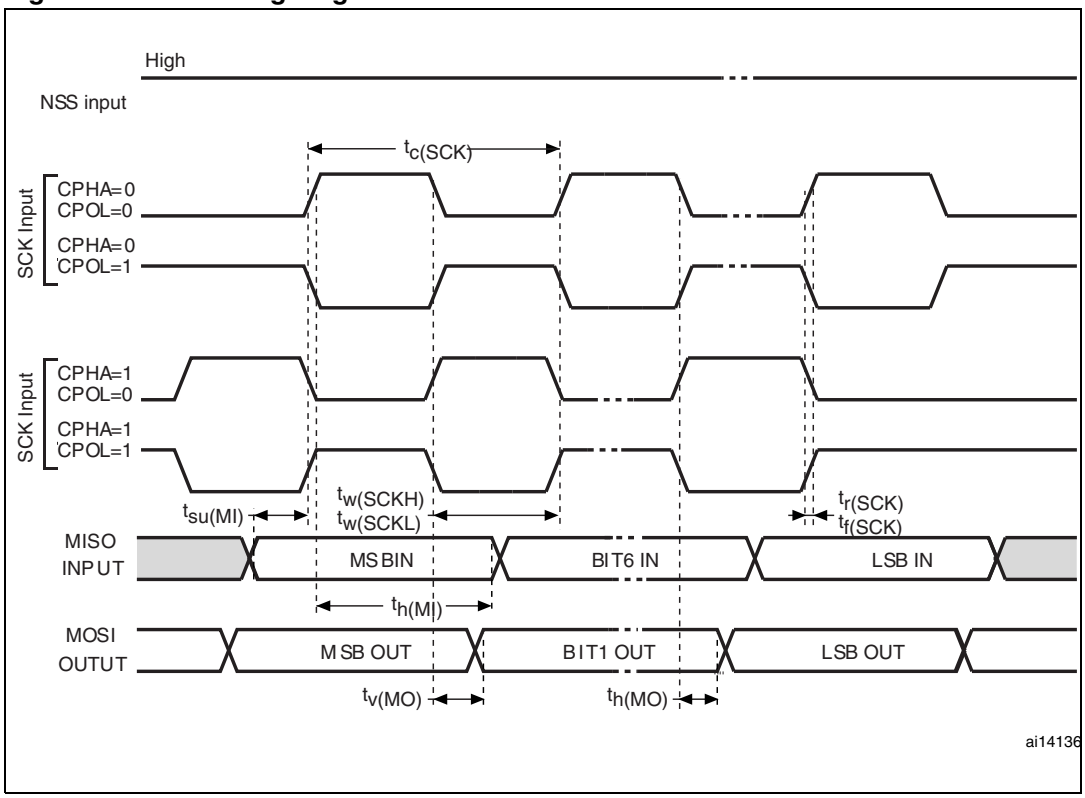
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 28. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Note: It is recommended to perform a calibration after each power-up.

Table 45. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
R_{AIN}(2)	External input impedance		See *Equation 1* and *Table 46*			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				12	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz			0.214	µs
					3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. In devices delivered in VFQFPN and LQFP packages, V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}. Devices that come in the TFBGA64 package have a V_{REF+} pin but no V_{REF-} pin (V_{REF-} is internally connected to V_{SSA}), see *Table 5* and *Figure 6*.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 45*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 46. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	1.2
7.5	0.54	10
13.5	0.96	19
28.5	2.04	41
41.5	2.96	60
55.5	3.96	80
71.5	5.11	104
239.5	17.1	350

1. Based on characterization, not tested in production.

Table 47. ADC accuracy - limited test conditions(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 34. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package outline(1)

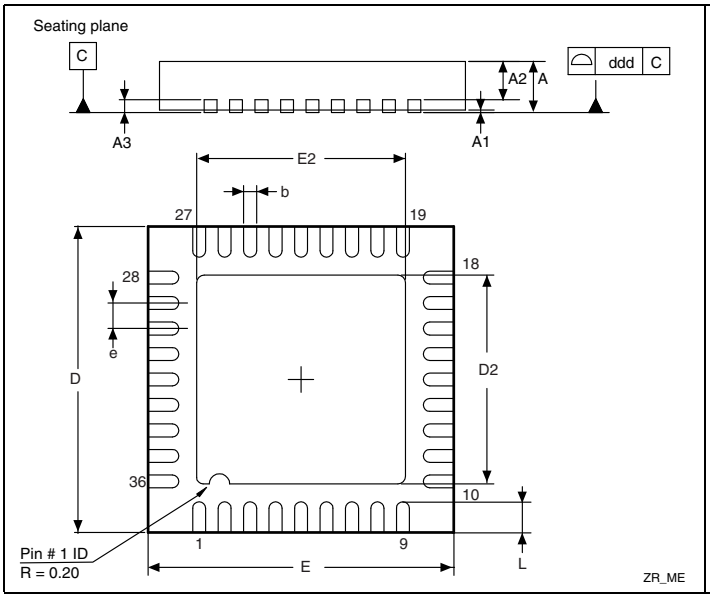
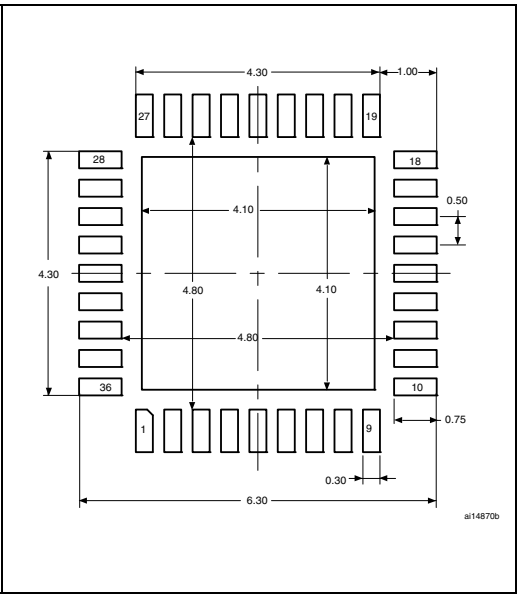


Figure 35. Recommended footprint (dimensions in mm)(1)(2)(3)



1. Drawing is not to scale.
2. The back-side pad is not internally connected to the V_{SS} or V_{DD} power pads.
3. There is an exposed die pad on the underside of the VFQFPN package. It should be soldered to the PCB. All leads should also be soldered to the PCB.

Table 50. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1		0.020	0.050		0.0008	0.0020
A2		0.650	1.000		0.0256	0.0394
A3		0.250			0.0098	
b	0.180	0.230	0.300	0.0071	0.0091	0.0118
D	5.875	6.000	6.125	0.2313	0.2362	0.2411
D2	1.750	3.700	4.250	0.0689	0.1457	0.1673
E	5.875	6.000	6.125	0.2313	0.2362	0.2411
E2	1.750	3.700	4.250	0.0689	0.1457	0.1673
e	0.450	0.500	0.550	0.0177	0.0197	0.0217
L	0.350	0.550	0.750	0.0138	0.0217	0.0295
ddd		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. LQFP100, 100-pin low-profile quad flat package outline(1)

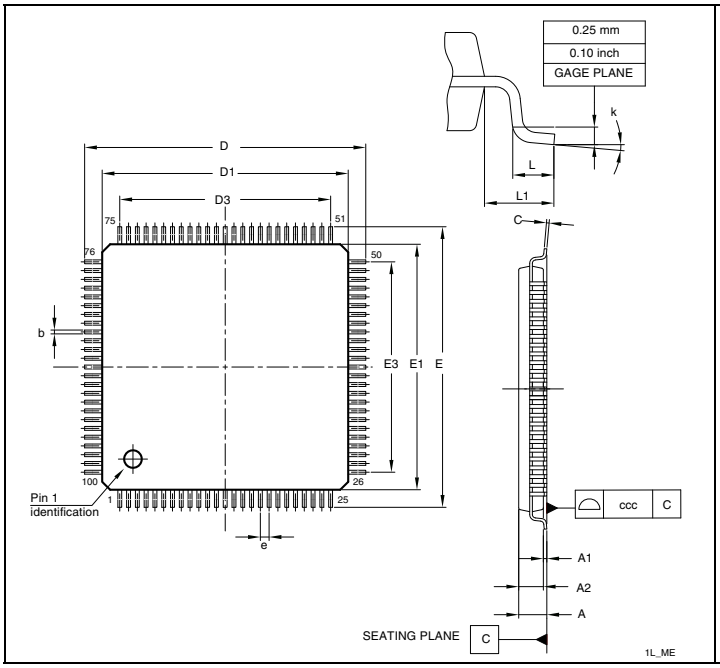
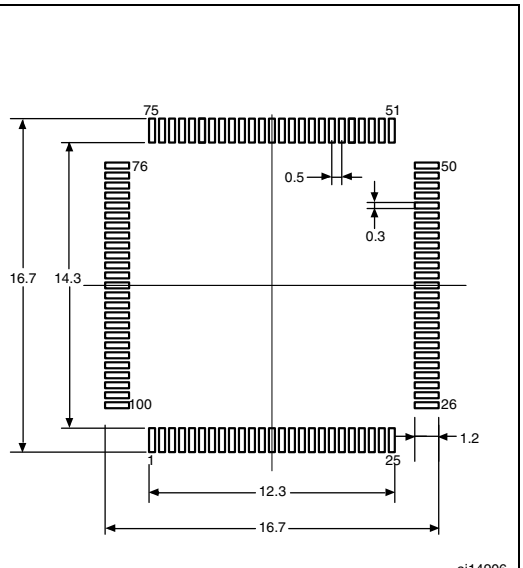


Figure 39. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 52. LQPF100, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	16	15.8	16.2	0.6299	0.622	0.6378
D1	14	13.8	14.2	0.5512	0.5433	0.5591
D3	12			0.4724		
E	16	15.8	16.2	0.6299	0.622	0.6378
E1	14	13.8	14.2	0.5512	0.5433	0.5591
E3	12			0.4724		
e	0.5			0.0197		
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
k	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP48, 48-pin low-profile quad flat package outline(1)

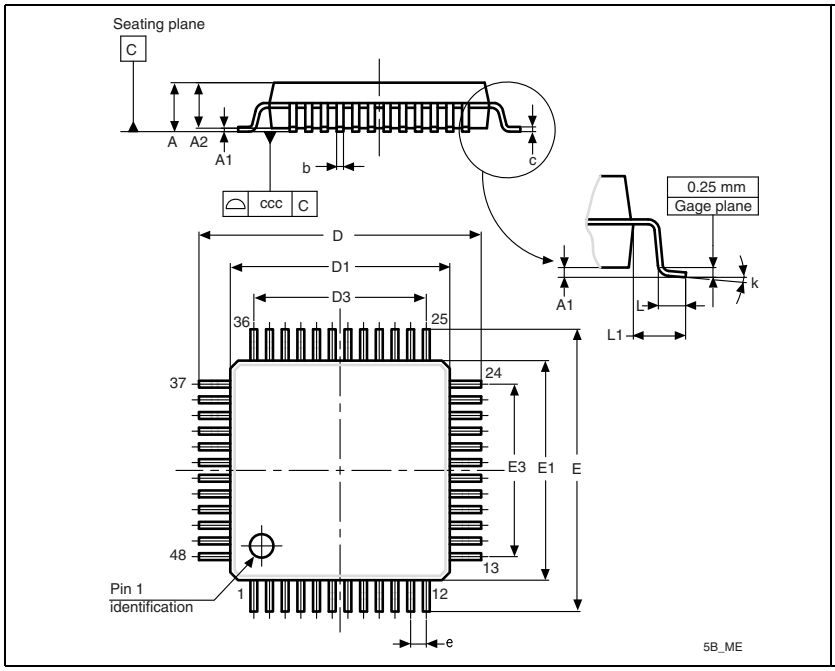
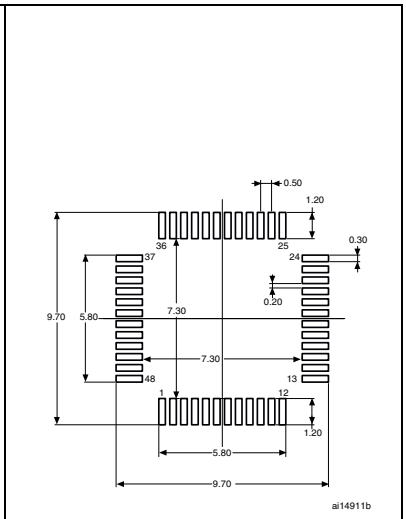


Figure 45. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 55. LQFP48, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
c		0.090	0.200		0.0035	0.0079
D	9.000	8.800	9.200	0.3543	0.3465	0.3622
D1	7.000	6.800	7.200	0.2756	0.2677	0.2835
D3	5.500			0.2165		
E	9.000	8.800	9.200	0.3543	0.3465	0.3622
E1	7.000	6.800	7.200	0.2756	0.2677	0.2835
E3	5.500			0.2165		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Using the values obtained in *Table 56* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 57: Ordering information scheme*).

Figure 46. LQFP100 P_D max vs. T_A