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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103cbt7tr

2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and advanced-control timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Timers and watchdogs

The medium-density STM32F103xx performance line devices include an advanced-control timer, three general-purpose timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the advanced-control and general-purpose timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It

can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.3.16 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.17 Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

2.3.18 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.19 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.20 Universal serial bus (USB)

The STM32F103xx performance line embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

Figure 4. STM32F103xx performance line LQFP100 pinout

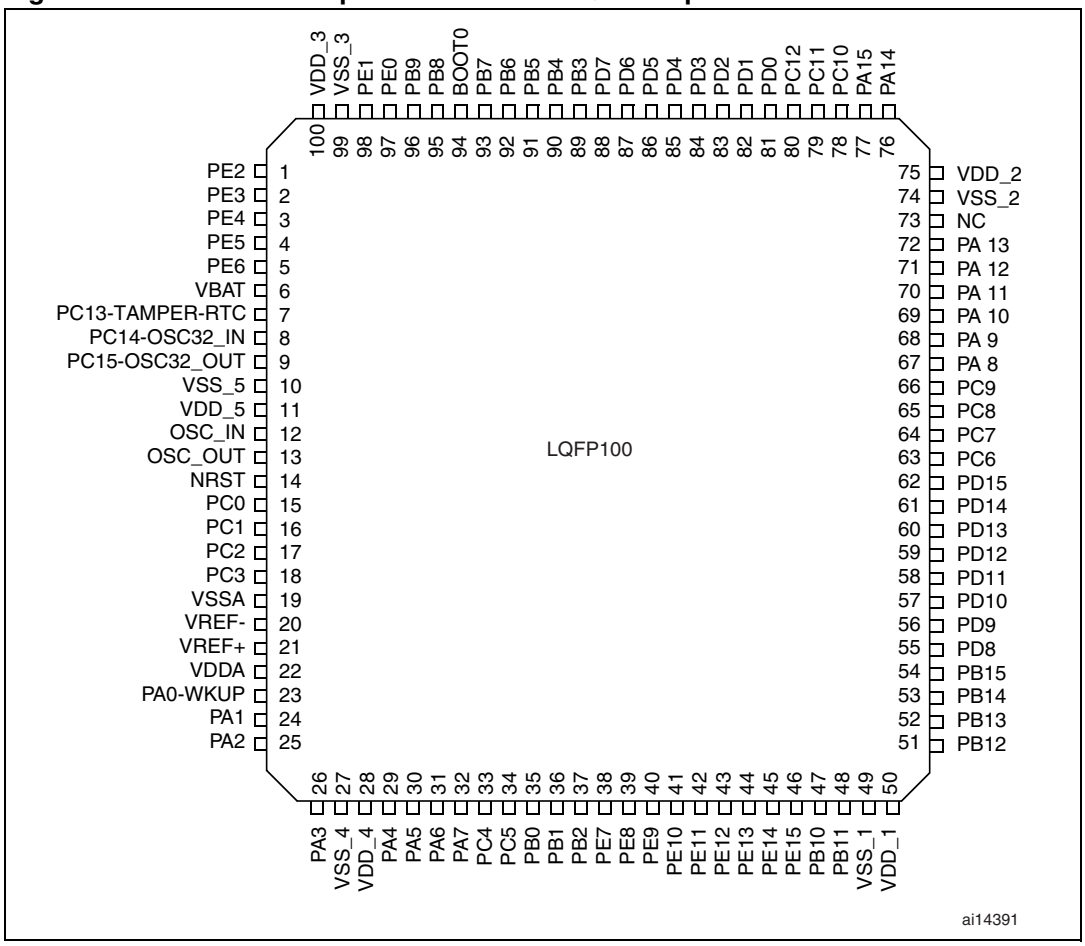
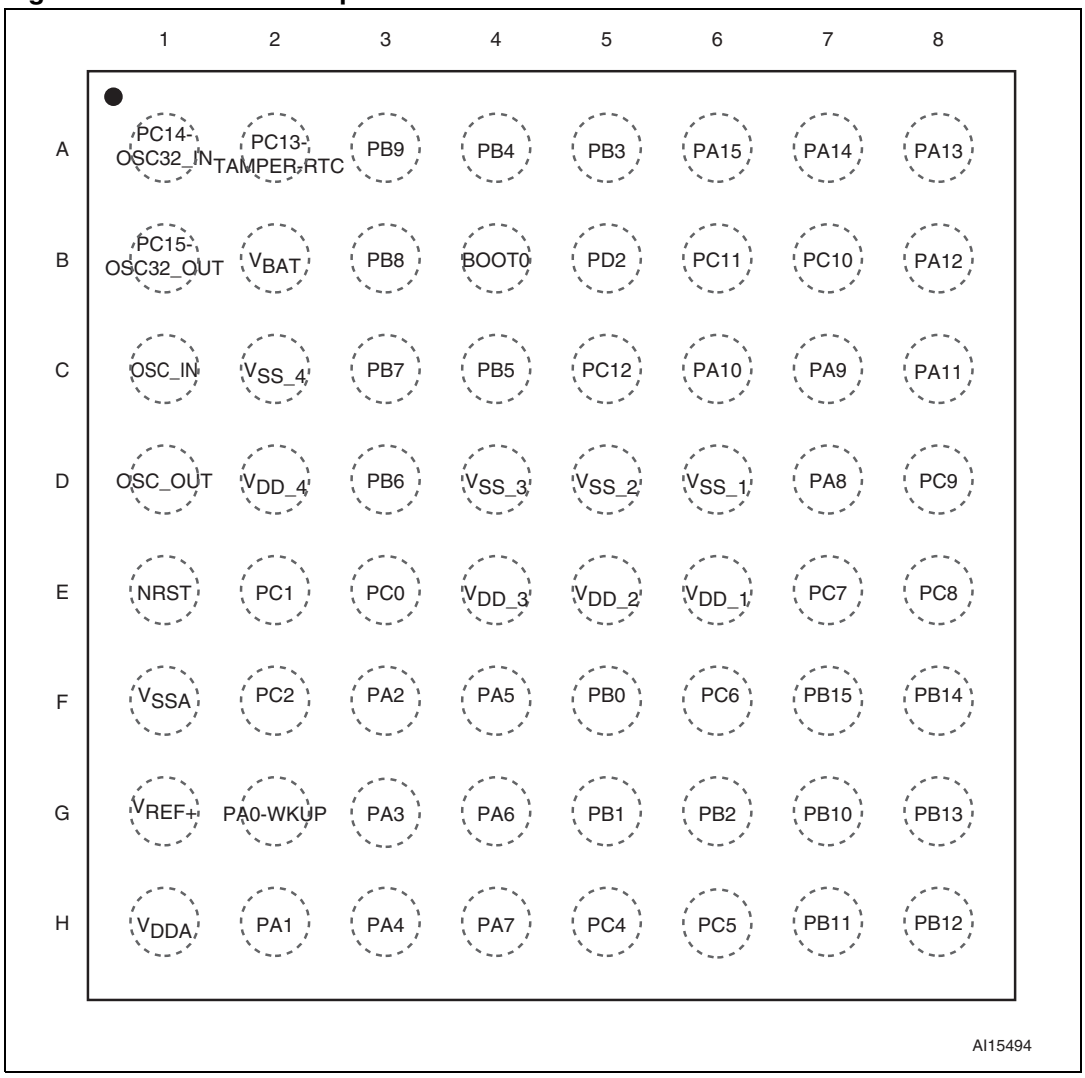


Figure 6. STM32F103xx performance line TFBGA64 ballout



4 Memory mapping

The memory map is shown in *Figure 9*.

Figure 9. Memory map

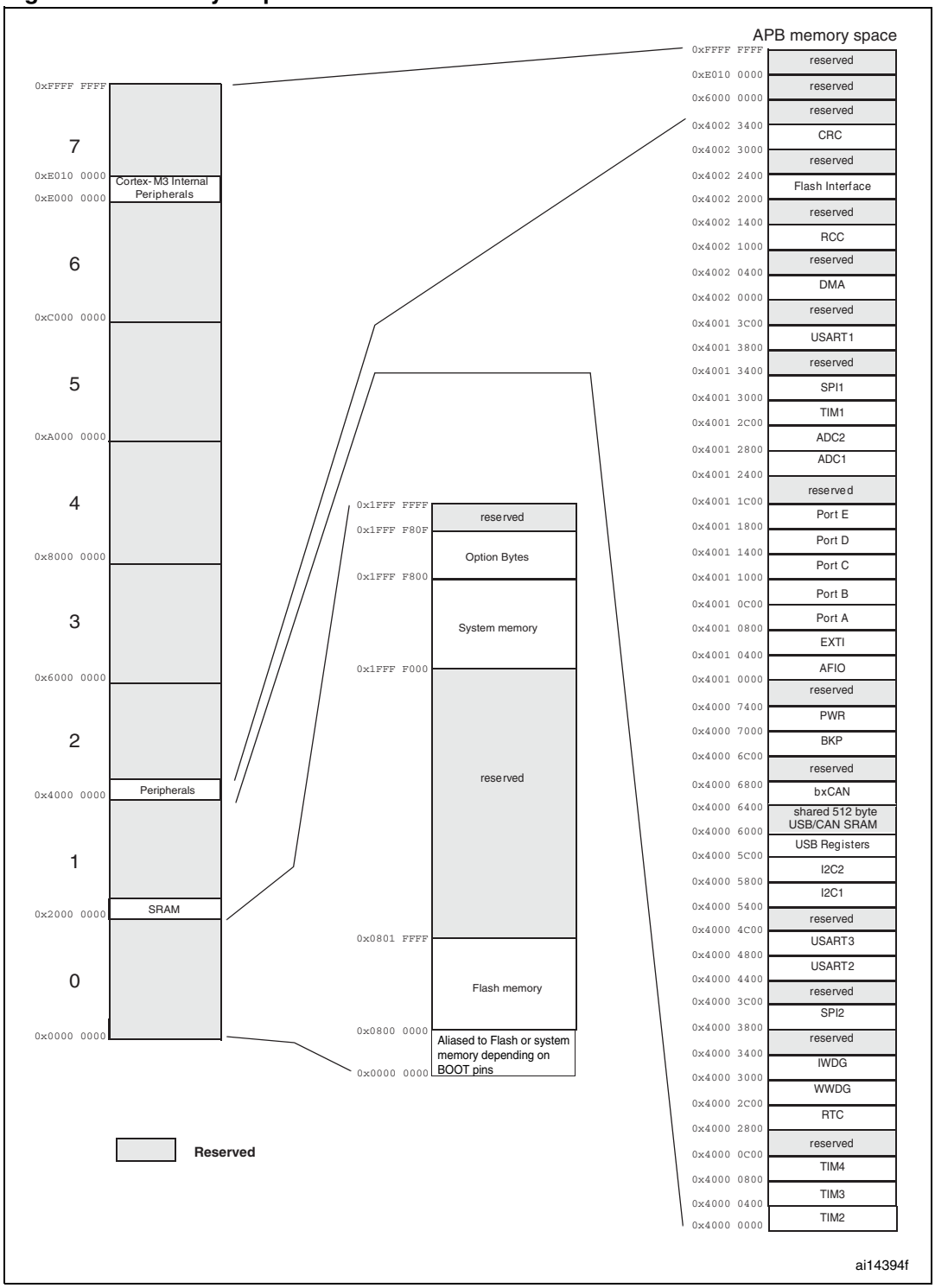


Table 13. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	50	50.3	mA
			48 MHz	36.1	36.2	
			36 MHz	28.6	28.7	
			24 MHz	19.9	20.1	
			16 MHz	14.7	14.9	
			8 MHz	8.6	8.9	
		External clock(2), all peripherals disabled	72 MHz	32.8	32.9	
			48 MHz	24.4	24.5	
			36 MHz	19.8	19.9	
			24 MHz	13.9	14.2	
			16 MHz	10.7	11	
			8 MHz	6.8	7.1	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 14. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	48	50	mA
			48 MHz	31.5	32	
			36 MHz	24	25.5	
			24 MHz	17.5	18	
			16 MHz	12.5	13	
			8 MHz	7.5	8	
		External clock(2), all peripherals disabled	72 MHz	29	29.5	
			48 MHz	20.5	21	
			36 MHz	16	16.5	
			24 MHz	11.5	12	
			16 MHz	8.5	9	
			8 MHz	5.5	6	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	14.4	5.5	mA
			48 MHz	9.9	3.9	
			36 MHz	7.6	3.1	
			24 MHz	5.3	2.3	
			16 MHz	3.8	1.8	
			8 MHz	2.1	1.2	
			4 MHz	1.6	1.1	
			2 MHz	1.3	1	
			1 MHz	1.11	0.98	
			500 kHz	1.04	0.96	
			125 kHz	0.98	0.95	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	12.3	4.4	
			48 MHz	9.3	3.3	
			36 MHz	7	2.5	
			24 MHz	4.8	1.8	
			16 MHz	3.2	1.2	
			8 MHz	1.6	0.6	
			4 MHz	1	0.5	
			2 MHz	0.72	0.47	
			1 MHz	0.56	0.44	
			500 kHz	0.49	0.42	
			125 kHz	0.43	0.41	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		0	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)			5		pF
$DuCy_{(LSE)}$	Duty cycle		30		70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 23* and *Table 36*, respectively.

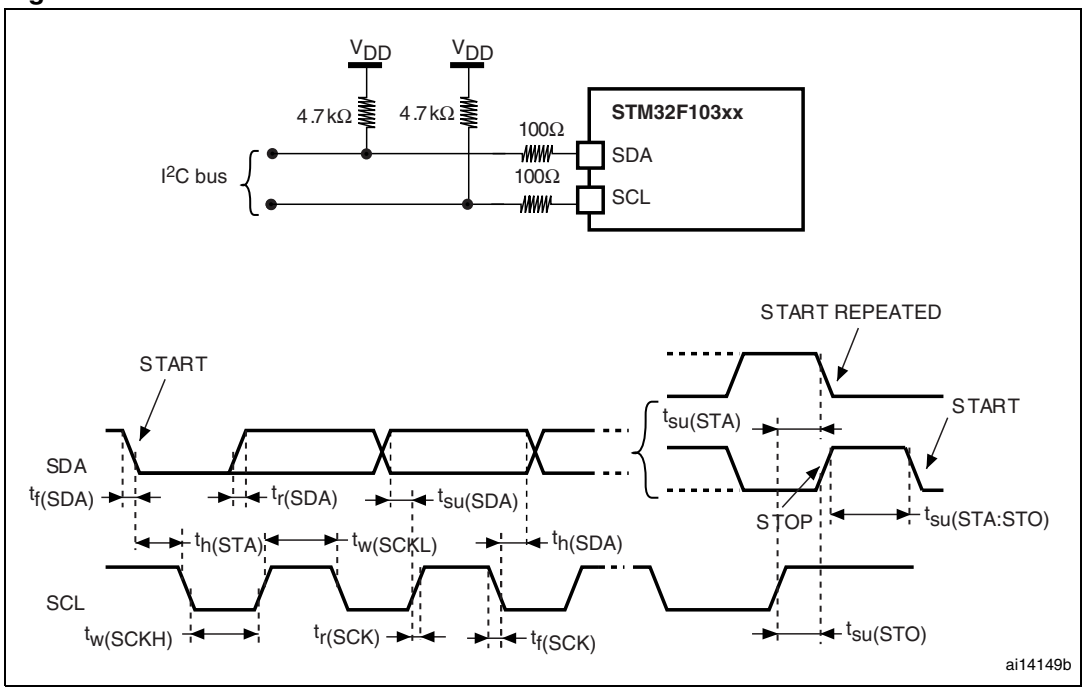
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 36. I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 23*.
3. Guaranteed by design, not tested in production.

Figure 25. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Table 48. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

Figure 30. ADC accuracy characteristics

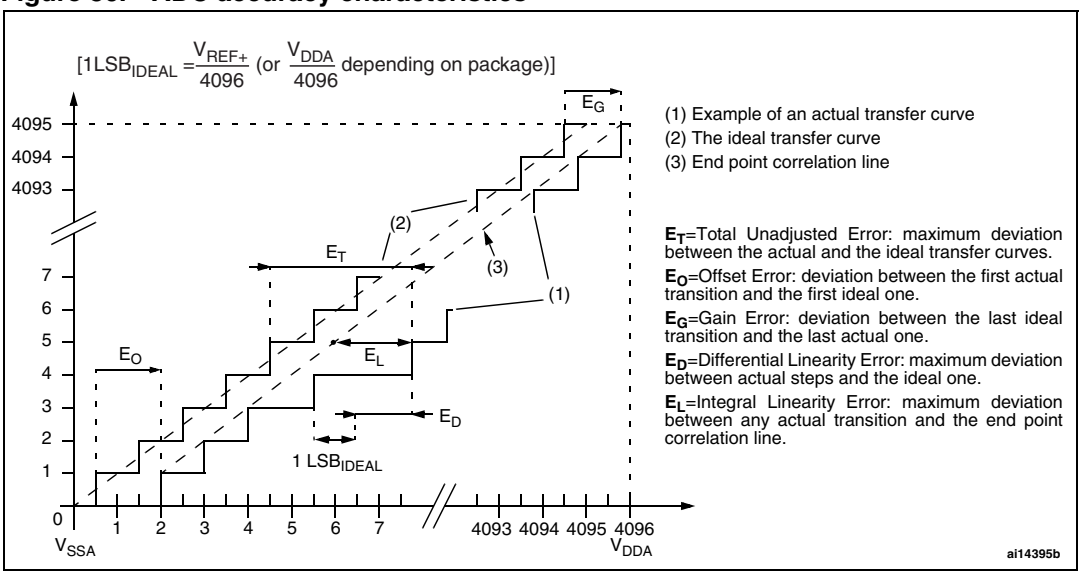
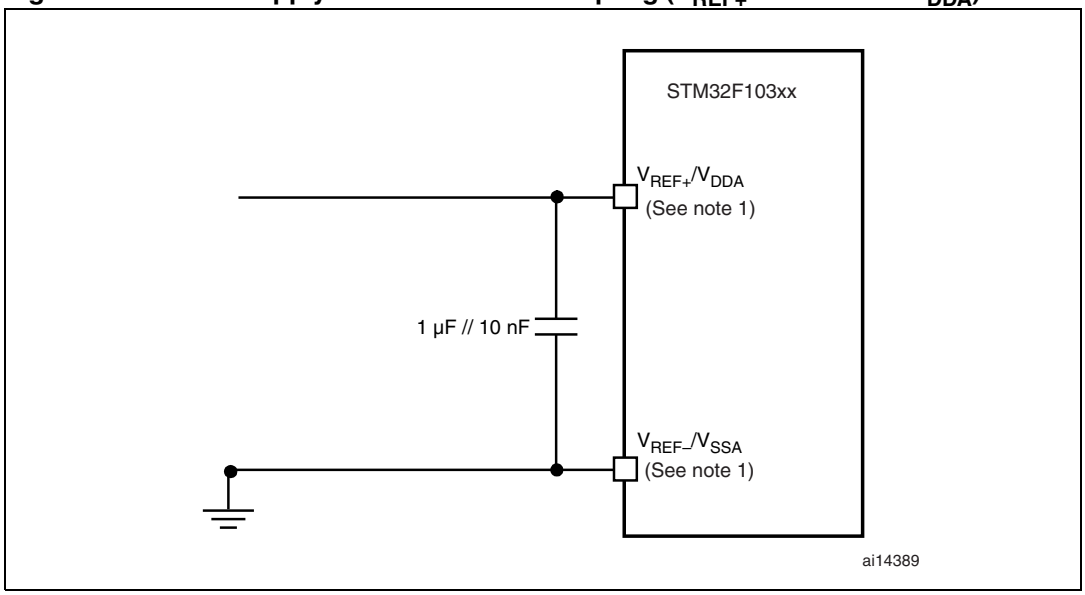


Figure 33. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{25}[1]	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}[2]	Startup time	4		10	µs
T_{S_temp}[3][2]	ADC sampling time when reading the temperature			17.1	µs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Figure 34. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package outline(1)

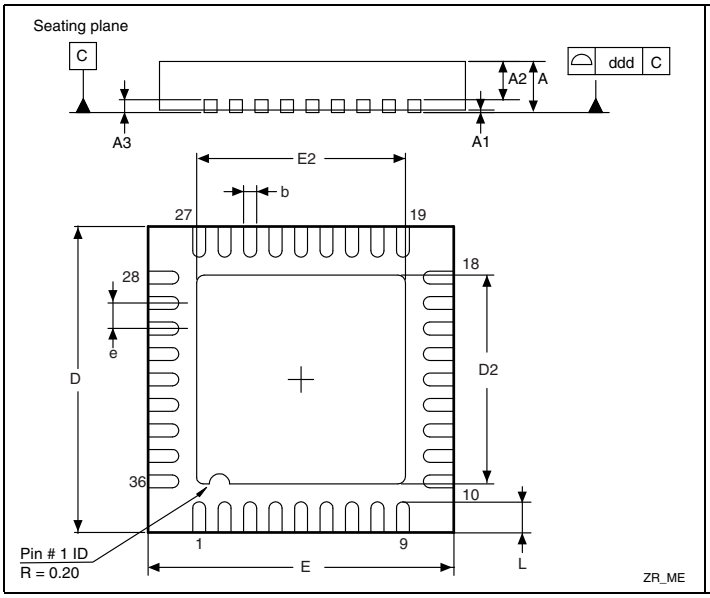
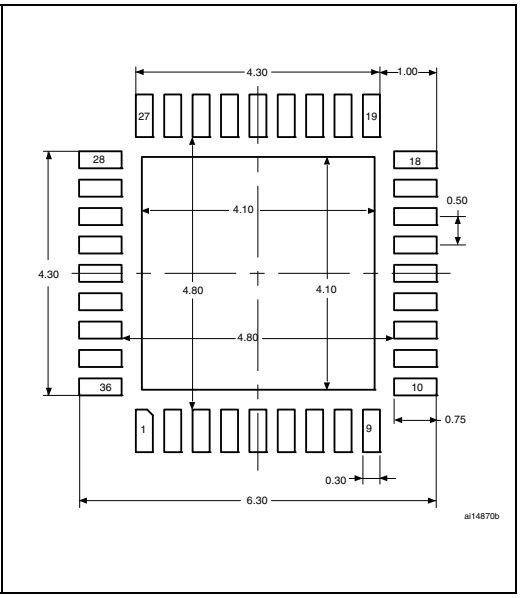


Figure 35. Recommended footprint (dimensions in mm)(1)(2)(3)



1. Drawing is not to scale.
2. The back-side pad is not internally connected to the V_{SS} or V_{DD} power pads.
3. There is an exposed die pad on the underside of the VFQFPN package. It should be soldered to the PCB. All leads should also be soldered to the PCB.

Table 50. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1		0.020	0.050		0.0008	0.0020
A2		0.650	1.000		0.0256	0.0394
A3		0.250			0.0098	
b	0.180	0.230	0.300	0.0071	0.0091	0.0118
D	5.875	6.000	6.125	0.2313	0.2362	0.2411
D2	1.750	3.700	4.250	0.0689	0.1457	0.1673
E	5.875	6.000	6.125	0.2313	0.2362	0.2411
E2	1.750	3.700	4.250	0.0689	0.1457	0.1673
e	0.450	0.500	0.550	0.0177	0.0197	0.0217
L	0.350	0.550	0.750	0.0138	0.0217	0.0295
ddd		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP48, 48-pin low-profile quad flat package outline(1)

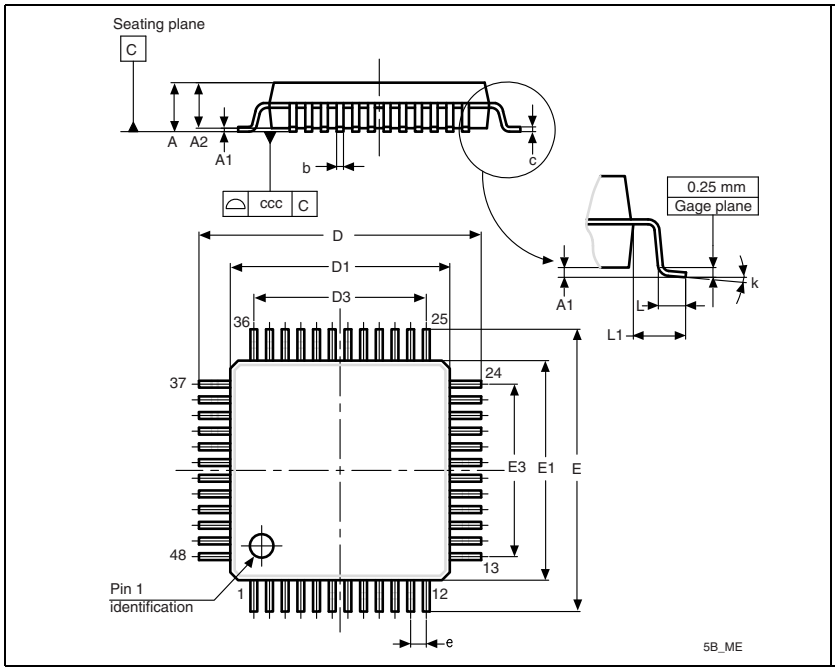
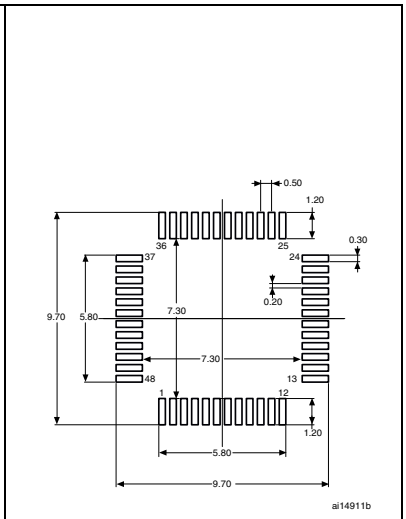


Figure 45. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 55. LQFP48, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
c		0.090	0.200		0.0035	0.0079
D	9.000	8.800	9.200	0.3543	0.3465	0.3622
D1	7.000	6.800	7.200	0.2756	0.2677	0.2835
D3	5.500			0.2165		
E	9.000	8.800	9.200	0.3543	0.3465	0.3622
E1	7.000	6.800	7.200	0.2756	0.2677	0.2835
E3	5.500			0.2165		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Using the values obtained in *Table 56* T_{Jmax} is calculated as follows:

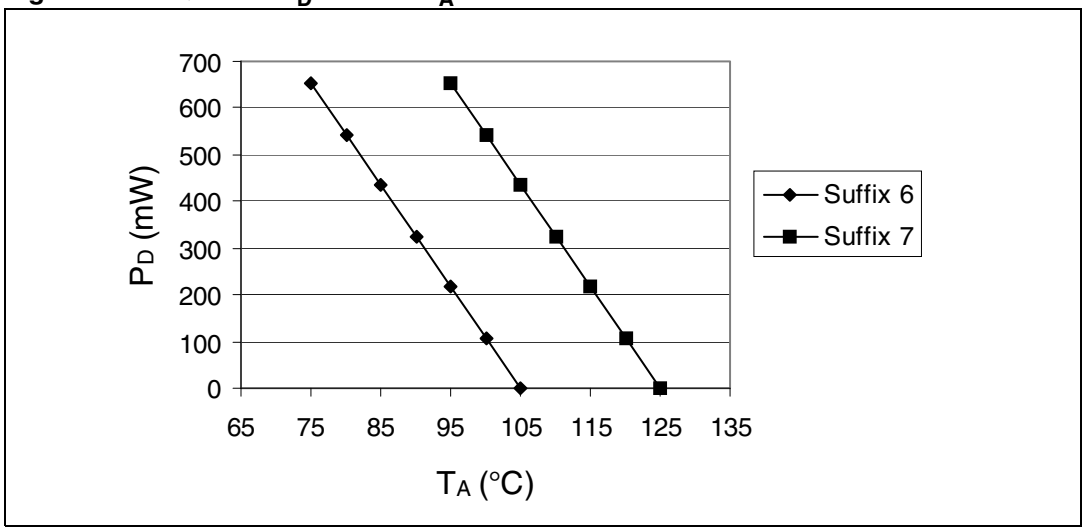
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 57: Ordering information scheme*).

Figure 46. LQFP100 P_D max vs. T_A



8 Revision history

Table 58. Document revision history

Date	Revision	Changes
01-jun-2007	1	Initial release.
20-Jul-2007	2	Flash memory size modified in *Note 7*, *Note 4*, *Note 7*, *Note 8* and BGA100 pins added to *Table 5: Medium-density STM32F103xx pin definitions*. *Figure 3: STM32F103xx performance line LFBGA100 ballout* added. T_{HSE} changed to T_{LSE} in *Figure 20: Low-speed external clock source AC timing diagram*. V_{BAT} ranged modified in *Power supply schemes*. $t_{SU(LSE)}$ changed to $t_{SU(HSE)}$ in *Table 22: HSE 4-16 MHz oscillator characteristics*. $I_{DD(HSI)}$ max value added to *Table 24: HSI oscillator characteristics*. Sample size modified and machine model removed in *Electrostatic discharge (ESD)*. Number of parts modified and standard reference updated in *Static latch-up*. 25 °C and 85 °C conditions removed and class name modified in *Table 33: Electrical sensitivities*. R_{PU} and R_{PD} min and max values added to *Table 34: I/O static characteristics*. R_{PU} min and max values added to *Table 37: NRST pin characteristics*. *Figure 25: I^2C bus AC waveforms and measurement circuit* and *Figure 24: Recommended NRST pin protection* corrected. Notes removed below *Table 9*, *Table 37*, *Table 43*. I_{DD} typical values changed in *Table 11: Maximum current consumption in Run and Sleep modes*. *Table 38: TIMx characteristics* modified. t_{STAB}, V_{REF+} value, t_{lat} and f_{TRIG} added to *Table 45: ADC characteristics*. In *Table 29: Flash memory endurance and data retention*, typical endurance and data retention for T_A = 85 °C added, data retention for T_A = 25 °C removed. V_{BG} changed to V_{REFINT} in *Table 12: Embedded internal reference voltage*. Document title changed. *Controller area network (CAN)* section modified. *Figure 12: Power supply scheme* modified. *Features on page 1* list optimized. Small text changes.

Table 58. Document revision history (continued)

Date	Revision	Changes
14-Mar-2008	5	*Figure 2: Clock tree on page 20* added. Maximum T_J value given in *Table 8: Thermal characteristics on page 35*. CRC feature added (see *CRC (cyclic redundancy check) calculation unit on page 9* and *Figure 9: Memory map on page 31* for address). I_{DD} modified in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. ACC_{HSI} modified in *Table 24: HSI oscillator characteristics on page 51*, note 2 removed. P_D, T_A and T_J added, t_{prog} values modified and t_{prog} description clarified in *Table 28: Flash memory characteristics on page 52*. t_{RET} modified in *Table 29: Flash memory endurance and data retention*. $V_{NF(NRST)}$ unit corrected in *Table 37: NRST pin characteristics on page 59*. *Table 41: SPI characteristics on page 63* modified. I_{VREF} added to *Table 45: ADC characteristics on page 67*. *Table 47: ADC accuracy - limited test conditions* added. *Table 48: ADC accuracy* modified. LQFP100 package specifications updated (see *Section 6: Package characteristics on page 72*). Recommended LQFP100, LQFP 64, LQFP48 and VFQFPN36 footprints added (see *Figure 39*, *Figure 41*, *Figure 45* and *Figure 35*). *Section 6.2: Thermal characteristics on page 81* modified, *Section 6.2.1* and *Section 6.2.2* added. *Appendix A: Important notes on page 81* removed.
21-Mar-2008	6	Small text changes. *Figure 9: Memory map* clarified. In *Table 29: Flash memory endurance and data retention*: – N_{END} tested over the whole temperature range – cycling conditions specified for t_{RET} – t_{RET} min modified at T_A = 55 °C V_{25}, Avg_Slope and T_L modified in *Table 49: TS characteristics*. CRC feature removed.
22-May-2008	7	CRC feature added back. Small text changes. *Section 1: Introduction* modified. *Section 2.2: Full compatibility throughout the family* added. I_{DD} at T_A max = 105 °C added to *Table 16: Typical and maximum current consumptions in Stop and Standby modes on page 42*. I_{DD_VBAT} removed from *Table 21: Typical current consumption in Standby mode on page 47*. Values added to *Table 40: SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V) on page 62*. *Figure 26: SPI timing diagram - slave mode and CPHA = 0 on page 64* modified. *Equation 1* corrected. t_{RET} at T_A = 105 °C modified in *Table 29: Flash memory endurance and data retention on page 53*. V_{USB} added to *Table 43: USB DC electrical characteristics on page 66*. *Figure 46: LQFP100 P_D max vs. T_A on page 83* modified. Axx option added to *Table 57: Ordering information scheme on page 84*.