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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103cbu6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

5	Elect	rical ch	aracteristics	32
	5.1	Parame	eter conditions	32
		5.1.1	Minimum and maximum values	32
		5.1.2	Typical values	32
		5.1.3	Typical curves	32
		5.1.4	Loading capacitor	32
		5.1.5	Pin input voltage	32
		5.1.6	Power supply scheme	33
		5.1.7	Current consumption measurement	34
	5.2	Absolut	e maximum ratings	34
	5.3	Operati	ng conditions	35
		5.3.1	General operating conditions	35
		5.3.2	Operating conditions at power-up / power-down	36
		5.3.3	Embedded reset and power control block characteristics	36
		5.3.4	Embedded reference voltage	38
		5.3.5	Supply current characteristics	38
		5.3.6	External clock source characteristics	47
		5.3.7	Internal clock source characteristics	50
		5.3.8	PLL characteristics	52
		5.3.9	Memory characteristics	52
		5.3.10	EMC characteristics	53
		5.3.11	Absolute maximum ratings (electrical sensitivity)	55
		5.3.12	I/O port characteristics	56
		5.3.13	NRST pin characteristics	59
		5.3.14	TIM timer characteristics	60
		5.3.15	Communications interfaces	61
		5.3.16	CAN (controller area network) interface	66
		5.3.17	12-bit ADC characteristics	67
		5.3.18	Temperature sensor characteristics	71
6	Pack	age cha	racteristics	72
	6.1	Packag	e mechanical data	72
	6.2	Therma	Il characteristics	81
		6.2.1	Reference document	81
		6.2.2	Selecting the product temperature range	
7	Orde	ring info	ormation scheme	84
57			Doc ID 13587 Rev 10	3/91

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x8 and STM32F103xB medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual. The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex[™]-M3 core please refer to the Cortex[™]-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F103x8 and STM32F103xB performance line family incorporates the highperformance ARM Cortex[™]-M3 32-bit RISC core operating at a 72 MHz frequency, highspeed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx medium-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the -40 to +85 °C temperature range and the -40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.



This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.3.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 12: Power supply scheme*.

2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains







1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.

- For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 48 MHz or 72 MHz.
- 3. To have an ADC conversion time of 1 $\mu s,$ APB2 must be at 14 MHz, 28 MHz or 56 MHz.



		Pir	IS					(2)		Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36	Pin name	Type ⁽¹⁾	I / O Level	Main function ⁽³⁾ (after reset)	Default	Remap
К2	13	G3	17	26	10	PA3	I/O		PA3	USART2_RX ⁽⁷⁾ / ADC12_IN3/ TIM2_CH4 ⁽⁷⁾	
E4	-	C2	18	27	-	V_{SS_4}	S		V _{SS_4}		
F4	-	D2	19	28	-	V_{DD_4}	S		V _{DD_4}		
G3	14	HЗ	20	29	11	PA4	I/O		PA4	SPI1_NSS ⁽⁷⁾ / USART2_CK ⁽⁷⁾ / ADC12_IN4	
НЗ	15	F4	21	30	12	PA5	I/O		PA5	SPI1_SCK ⁽⁷⁾ / ADC12_IN5	
JЗ	16	G4	22	31	13	PA6	I/O		PA6	SPI1_MISO ⁽⁷⁾ / ADC12_IN6/ TIM3_CH1 ⁽⁷⁾	TIM1_BKIN
КЗ	17	H4	23	32	14	PA7	I/O		PA7	SPI1_MOSI ⁽⁷⁾ / ADC12_IN7/ TIM3_CH2 ⁽⁷⁾	TIM1_CH1N
G4	-	H5	24	33		PC4	I/O		PC4	ADC12_IN14	
H4	-	H6	25	34		PC5	I/O		PC5	ADC12_IN15	
J4	18	F5	26	35	15	PB0	I/O		PB0	ADC12_IN8/ TIM3_CH3 ⁽⁷⁾	TIM1_CH2N
K4	19	G5	27	36	16	PB1	I/O		PB1	ADC12_IN9/ TIM3_CH4 ⁽⁷⁾	TIM1_CH3N
G5	20	G6	28	37	17	PB2	I/O	FT	PB2/BOOT1		
H5	-	-	-	38	-	PE7	I/O	FT	PE7		TIM1_ETR
J5	-	•	-	39	-	PE8	I/O	FT	PE8		TIM1_CH1N
K5	-	-	-	40	-	PE9	I/O	FT	PE9		TIM1_CH1
G6	-	-	-	41	-	PE10	I/O	FT	PE10		TIM1_CH2N
H6	-	-	-	42	-	PE11	I/O	FT	PE11		TIM1_CH2
J6	-	-	-	43	-	PE12	I/O	FT	PE12		TIM1_CH3N
K6	-	-	-	44	-	PE13	I/O	FT	PE13		TIM1_CH3
G7	-	-	-	45	-	PE14	I/O	FT	PE14		TIM1_CH4
H7	-	-	-	46	-	PE15	I/O	FT	PE15		TIM1_BKIN
J7	21	G7	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX ⁽⁷⁾	TIM2_CH3
K7	22	H7	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX ⁽⁷⁾	TIM2_CH4
E7	23	D6	31	49	18	V _{SS_1}	S		V _{SS_1}		

Table 5. Medium-density STM32F103xx pin definit	ions (continued)
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		Pin	IS					(2)		Alternate functions		
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36	Pin name	Type ⁽¹⁾	I / O Level	Main function ⁽³⁾ (after reset)	Default	Remap	
F7	24	E6	32	50	19	V _{DD_1}	S		V_{DD_1}			
K8	25	H8	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK ⁽⁷⁾ / TIM1_BKIN ⁽⁷⁾		
J8	26	G8	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS ⁽⁷⁾ / TIM1_CH1N ⁽⁷⁾		
H8	27	F8	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS ⁽⁷⁾ TIM1_CH2N ⁽⁷⁾		
G8	28	F7	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N ⁽⁷⁾		
K9	-	-	-	55	-	PD8	I/O	FT	PD8		USART3_TX	
J9	-	-	-	56	-	PD9	I/O	FT	PD9		USART3_RX	
H9	-	I	•	57	-	PD10	I/O	FT	PD10		USART3_CK	
G9	-	•	-	58	-	PD11	I/O	FT	PD11		USART3_CTS	
K10	-	-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1 / USART3_RTS	
J10	-	-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2	
H10	-	I	•	61	-	PD14	I/O	FT	PD14		TIM4_CH3	
G10	-	-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4	
F10	-	F6	37	63	-	PC6	I/O	FT	PC6		TIM3_CH1	
E10		E7	38	64	-	PC7	I/O	FT	PC7		TIM3_CH2	
F9		E8	39	65	-	PC8	I/O	FT	PC8		TIM3_CH3	
E9	-	D8	40	66	-	PC9	I/O	FT	PC9		TIM3_CH4	
D9	29	D7	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1 ⁽⁷⁾ /MCO		
C9	30	C7	42	68	21	PA9	I/O	FT	PA9	USART1_TX ⁽⁷⁾ / TIM1_CH2 ⁽⁷⁾		
D10	31	C6	43	69	22	PA10	I/O	FT	PA10	USART1_RX ⁽⁷⁾ / TIM1_CH3 ⁽⁷⁾		
C10	32	C8	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ CANRX ⁽⁷⁾ / USBDM TIM1_CH4 ⁽⁷⁾		
B10	33	B8	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/ CANTX ⁽⁷⁾ //USBDP TIM1_ETR ⁽⁷⁾		

Table 5. Medium-density STM32F103xx pin definitions (continued)



STM32F103x8, STM32F103xB

57

		Pir	IS					(2)		Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36	Pin name	Type ⁽¹⁾	I / O Leve	Main function ⁽³⁾ (after reset)	Default	Remap
A10	34	A8	46	72	25	PA13	I/O	FT	JTMS/SWDIO		PA13
F8	-	-	-	73	-			Not	connected		
E6	35	D5	47	74	26	V _{SS_2}	S		V _{SS_2}		
F6	36	E5	48	75	27	V _{DD_2}	S		V_{DD_2}		
A9	37	A7	49	76	28	PA14	I/O	FT	JTCK/SWCLK		PA14
A8	38	A6	50	77	29	PA15	I/O	FT	JTDI		TIM2_CH1_ETR/ PA15 /SPI1_NSS
B9	-	B7	51	78		PC10	I/O	FT	PC10		USART3_TX
B8	-	B6	52	79		PC11	I/O	FT	PC11		USART3_RX
C8	-	C5	53	80		PC12	I/O	FT	PC12		USART3_CK
D8	5	C1	5	81	2	PD0	I/O	FT	OSC_IN ⁽⁸⁾		CANRX
E8	6	D1	6	82	3	PD1	I/O	FT	OSC_OUT ⁽⁸⁾		CANTX
B7		B5	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	
C7	-	-	-	84	-	PD3	I/O	FT	PD3		USART2_CTS
D7	-	-	-	85	-	PD4	I/O	FT	PD4		USART2_RTS
B6	-	-	-	86	-	PD5	I/O	FT	PD5		USART2_TX
C6	-	-	-	87	-	PD6	I/O	FT	PD6		USART2_RX
D6	-	-	-	88	-	PD7	I/O	FT	PD7		USART2_CK
A7	39	A5	55	89	30	PB3	I/O	FT	JTDO		TIM2_CH2/PB3 TRACESWO SPI1_SCK
A6	40	A4	56	90	31	PB4	I/O	FT	JNTRST		TIM3_CH1/PB4/ SPI1_MISO
C5	41	C4	57	91	32	PB5	I/O		PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
B5	42	D3	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL ⁽⁷⁾ / TIM4_CH1 ⁽⁷⁾	USART1_TX
A5	43	C3	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA ⁽⁷⁾ / TIM4_CH2 ⁽⁷⁾	USART1_RX
D5	44	B4	60	94	35	BOOT0	Ι		BOOT0		
B4	45	B3	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3 ⁽⁷⁾	I2C1_SCL / CANRX
A4	46	A3	62	96	-	PB9	I/O	FT	PB9	TIM4_CH4 ⁽⁷⁾	I2C1_SDA/ CANTX

Table 5. Medium-density STM32F103xx pin definitions (continued)



5.1.7 Current consumption measurement



Figure 13. Current consumption measurement scheme

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Min	Max	Unit	
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and $V_{DD})^{(1)}$	-0.3	4.0		
V _{IN}	Input voltage on five volt tolerant pin ⁽²⁾	$V_{SS} - 0.3$	+5.5	V	
	Input voltage on any other pin ⁽²⁾	$V_{SS} - 0.3$	V _{DD} +0.3		
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins		50	m\/	
$ V_{SSX} - V_{SS} $	Variations between all the different ground pins		50	IIIV	
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	see Section 5.3.11: Absolute maximum ratings (electrical sensitivity)			

 Table 6.
 Voltage characteristics

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. $I_{INJ(PIN)}$ must never be exceeded (see *Table 7: Current characteristics*). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by V_{IN} > V_{IN} max while a negative injection is induced by V_{IN} < V_{SS} .



Symbol Ratings		Max.	Unit
I _{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) ⁽¹⁾	150	
I _{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
1	Output current sunk by any I/O and control pin	25	
١O	Output current source by any I/Os and control pin	- 25	m 1
	Injected current on NRST pin	± 5	
I _{INJ(PIN)} ⁽²⁾⁽³⁾	Injected current on HSE OSC_IN and LSE OSC_IN pins	± 5	
	Injected current on any other pin ⁽⁴⁾	± 5	
$\Sigma I_{\rm INJ(PIN)}^{(2)}$	Total injected current (sum of all I/O and control pins) ⁽⁴⁾	± 25	

Table 7.Current characteristics

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

I_{INJ(PIN)} must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the I_{INJ(PIN)} value. A positive injection is induced by V_{IN} > V_{DD} while a negative injection is induced by V_{IN} < V_{SS}.

3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.

4. When several inputs are submitted to a current injection, the maximum Σl_{INJ(PIN)} is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with Σl_{INJ(PIN)} maximum current injection on four I/O port pins of the device.

Table 8.Thermal characteristics

Symbol	Ratings	Value	Unit
T _{STG}	Storage temperature range	-65 to +150	°C
Т _Ј	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9.General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f _{HCLK}	Internal AHB clock frequency		0	72	
f _{PCLK1}	Internal APB1 clock frequency		0	36	MHz
f _{PCLK2}	Internal APB2 clock frequency		0	72	
V _{DD}	Standard operating voltage		2	3.6	V
V (1)	Analog operating voltage (ADC not used)	Must be the same potential	2	3.6	М
V DDA`´´	Analog operating voltage (ADC used)	as V _{DD} ⁽²⁾	2.4	3.6	v
V _{BAT}	Backup operating voltage		1.8	3.6	V



5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{REFINT}	Internal reference voltage	$-40 \ ^{\circ}\text{C} < \text{T}_{\text{A}} < +105 \ ^{\circ}\text{C}$	1.16	1.20	1.26	V
		−40 °C < T _A < +85 °C	1.16	1.20	1.24	V
T _{S_vrefint} (1)	ADC sampling time when reading the internal reference voltage			5.1	17.1 ⁽²⁾	μs

Table 12. Embedded internal reference voltage

1. Shortest sampling time can be determined in the application by multiple iterations.

2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.













High-speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI}	Frequency			8		MHz
ACC _{HSI}		$T_A = -40$ to 105 °C	-2	±1	2.5	%
	Accuracy of HSI oscillator	$T_A = -10$ to 85 °C	-1.5	±1	2.2	%
		$T_A = 0$ to 70 °C	-1.3	±1	2	%
		$T_A = 25 \ ^\circ C$	-1.1	±1	1.8	%
t _{su(HSI)}	HSI oscillator startup time		1		2	μs
I _{DD(HSI)}	HSI oscillator power consumption			80	100	μA

Table 24. HSI oscillator characteristics^{(1) (2)}

1. Guaranteed by design, not tested in production.

2. $V_{DD} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min	Тур	Max	Unit
f _{LSI} ⁽²⁾	Frequency	30	40	60	kHz
t _{su(LSI)} ⁽³⁾	LSI oscillator startup time			85	μs
I _{DD(LSI)} ⁽³⁾	LSI oscillator power consumption		0.65	1.2	μA

1. V_{DD} = 3 V, T_A = -40 to 105 °C unless otherwise specified.

2. Based on characterization, not tested in production.

3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.



Symbol	Parameter	Conditions	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
		Read mode $f_{HCLK} = 72 \text{ MHz with 2 wait}$ states, V _{DD} = 3.3 V			20	mA
I _{DD}	Supply current	Write / Erase modes f _{HCLK} = 72 MHz, V _{DD} = 3.3 V			5	mA
		Power-down mode / Halt, $V_{DD} = 3.0$ to 3.6 V			50	μA
V _{prog}	Programming voltage		2		3.6	V

Table 28. Flash memory characteristics (continued)

1. Guaranteed by design, not tested in production.

Table 29. Flash memory endurance and data retention

Symbol	Paramotor	Conditions		Value			
Symbol			Min ⁽¹⁾	Тур	Max	Onit	
N _{END}	Endurance	$T_A = -40$ to +85 °C (6 suffix versions) $T_A = -40$ to +105 °C (7 suffix versions)	10			kcycles	
		1 kcycle ⁽²⁾ at $T_A = 85 \ ^{\circ}C$	30				
t _{RET}	Data retention	1 kcycle ⁽²⁾ at $T_A = 105 \ ^\circ C$	10			Years	
		10 kcycles ⁽²⁾ at T _A = 55 °C	20				

1. Based on characterization, not tested in production.

2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 30*. They are based on the EMS levels and classes defined in application note AN1709.



5.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL}	Input low level voltage		-0.5		0.8	
VIH	Standard IO input high level voltage	TTL ports	2		V _{DD} +0.5	V
	IO FT ⁽¹⁾ input high level voltage		2		5.5V	
V _{IL}	Input low level voltage	CMOS porte	-0.5		0.35 V _{DD}	V
V _{IH}	Input high level voltage	CINCS ports	0.65 V _{DD}		V _{DD} +0.5	v
V	Standard IO Schmitt trigger voltage hysteresis ⁽²⁾		200			mV
V _{hys}	IO FT Schmitt trigger voltage hysteresis ⁽²⁾		5% V _{DD} ⁽³⁾			mV
L.	Input loakage current ⁽⁴⁾	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os			±1	
'lkg	input leakage current V	V _{IN} = 5 V I/O FT			3	μΑ
R _{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$	30	40	50	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	30	40	50	kΩ
C _{IO}	I/O pin capacitance			5		pF

Table 34.I/O static characteristics

1. FT = Five-volt tolerant.

2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.

- 3. With a minimum of 100 mV.
- 4. Leakage could be higher than max. if negative current is injected on adjacent pins.
- 5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required), their characteristics consider the most strict CMOS-technology or TTL parameters:

- For V_{IH}:
 - if V_{DD} is in the [2.00 V 3.08 V] range: CMOS characteristics but TTL included
 - if V_{DD} is in the [3.08 V 3.60 V] range: TTL characteristics but CMOS included
- For V_{IL}:
 - if V_{DD} is in the [2.00 V 2.28 V] range: TTL characteristics but CMOS included
 - if V_{DD} is in the [2.28 V 3.60 V] range: CMOS characteristics but TTL included





Figure 28. SPI timing diagram - master mode⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{\text{DD}}$ and $0.7V_{\text{DD}}.$

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 42.USB startup time

Symbol	Parameter	Max	Unit
t _{STARTUP} ⁽¹⁾	USB transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.



Symbol	Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit			
Input leve	els							
V _{DD}	USB operating voltage ⁽²⁾		3.0 ⁽³⁾	3.6	V			
V _{DI} ⁽⁴⁾	Differential input sensitivity	I(USBDP, USBDM)	0.2					
V _{CM} ⁽⁴⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	V			
$V_{SE}^{(4)}$	Single ended receiver threshold		1.3	2.0				
Output le	Output levels							
V _{OL}	Static output level low	${\sf R}_{\sf L}$ of 1.5 k Ω to 3.6 V $^{(5)}$		0.3	V			
V _{OH}	Static output level high	${\sf R}_{\sf L}$ of 15 k Ω to ${\sf V}_{\sf SS}{}^{(5)}$	2.8	3.6	v			

 Table 43.
 USB DC electrical characteristics

1. All the voltages are measured from the local ground potential.

2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 k Ω resistor to a 3.0-to-3.6 V voltage range.

3. The STM32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.

4. Guaranteed by design, not tested in production.

5. R_L is the load connected on the USB drivers

Figure 29. USB timings: definition of data signal rise and fall time



Table 44	USB: Full-speed	electrical	characteristics ⁽¹⁾
1abic 44.	USD. I ull-speeu	electrical	characteristics.

Symbol	Parameter	Conditions	Min	Max	Unit
Driver cha	racteristics				
t _r	Rise time ⁽²⁾	C _L = 50 pF	4	20	ns
t _f	Fall time ⁽²⁾	C _L = 50 pF	4	20	ns
t _{rfm}	Rise/ fall time matching	t _r /t _f	90	110	%
V _{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

5.3.16 CAN (controller area network) interface

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).





Figure 38. LQFP100, 100-pin low-profile quad flat package outline⁽¹⁾

1. Drawing is not to scale.

2. Dimensions are in millimeters.

Table 52. LQPF100, 100-pin low-profile quad flat package mechanical data

Symbol		millimeters	limeters inches ⁽¹⁾			
Cymbol	Тур	Min	Мах	Тур	Min	Мах
A			1.6			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
С		0.09	0.2		0.0035	0.0079
D	16	15.8	16.2	0.6299	0.622	0.6378
D1	14	13.8	14.2	0.5512	0.5433	0.5591
D3	12			0.4724		
E	16	15.8	16.2	0.6299	0.622	0.6378
E1	14	13.8	14.2	0.5512	0.5433	0.5591
E3	12			0.4724		
е	0.5			0.0197		
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
k	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
CCC		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Figure 39. Recommended footprint $^{(1)(2)}$

Figure 44. LQFP48, 48-pin low-profile quad flat package outline⁽¹⁾





1. Drawing is not to scale.

2. Dimensions are in millimeters.

Table 55.	LQFP48, 48-pin	low-profile q	uad flat packa	ge mechanical data
				U

Symbol	millimeters			eters inches ⁽¹⁾		
Symbol	Тур	Min	Мах	Тур	Min	Мах
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
с		0.090	0.200		0.0035	0.0079
D	9.000	8.800	9.200	0.3543	0.3465	0.3622
D1	7.000	6.800	7.200	0.2756	0.2677	0.2835
D3	5.500			0.2165		
E	9.000	8.800	9.200	0.3543	0.3465	0.3622
E1	7.000	6.800	7.200	0.2756	0.2677	0.2835
E3	5.500			0.2165		
е	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k	3.5°	0°	7 °	3.5°	0°	7 °
CCC		0.080	•		0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Date	Revision	Changes
23-Apr-2009	10	 I/O information clarified on page 1. <i>Figure 3: STM32F103xx performance line LFBGA100 ballout</i> modified. <i>Figure 9: Memory map</i> modified. <i>Table 4: Timer feature comparison</i> added. PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column in <i>Table 5: Medium-density STM32F103xx pin definitions</i>.
		P _D for LFBGA100 corrected in <i>Table 9: General operating conditions</i> .
		Note modified in Table 13: Maximum current consumption in Run mode, code with data processing running from Flash and Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM.
		Table 20: High-speed external user clock characteristics and Table 21:Low-speed external user clock characteristics modified.
		<i>Figure 17</i> shows a typical curve (title modified). ACC _{HSI} max values modified in <i>Table 24: HSI oscillator characteristics</i> .
		TFBGA64 package added (see <i>Table 54</i> and <i>Table 42</i>). Small text changes.

Table 58. Document revision history (continued)



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