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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 51 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103r8t6tr |

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x8 and STM32F103xB medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

# 2 Description

The STM32F103x8 and STM32F103xB performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two $I^2C$s and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx medium-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

*Figure 1* shows the general block diagram of the device family.

## 2.2 Full compatibility throughout the family

The STM32F103xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x4 and STM32F103x6 are identified as low-density devices, the STM32F103x8 and STM32F103xB are referred to as medium-density devices, and the STM32F103xC, STM32F103xD and STM32F103xE are referred to as high-density devices.

Low- and high-density devices are an extension of the STM32F103x8/B devices, they are specified in the STM32F103x4/6 and STM32F103xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, $I^2S$ and DAC, while remaining fully compatible with the other members of the STM32F103xx family.

The STM32F103x4, STM32F103x6, STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for STM32F103x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F103xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

**Table 3. STM32F103xx family**

| Pinout | Low-density devices | | Medium-density devices | | High-density devices | | |
|---|---|---|---|---|---|---|---|
| | 16 KB Flash | 32 KB Flash(1) | 64 KB Flash | 128 KB Flash | 256 KB Flash | 384 KB Flash | 512 KB Flash |
| | 6 KB RAM | 10 KB RAM | 20 KB RAM | 20 KB RAM | 48 KB RAM | 64 KB RAM | 64 KB RAM |
| 144 | | | | | 5 × USARTs<br>4 × 16-bit timers, 2 × basic timers<br>3 × SPIs, 2 × $I^2$Ss, 2 × I2Cs<br>USB, CAN, 2 × PWM timers<br>3 × ADCs, 1 × DAC, 1 × SDIO<br>FSMC (100 and 144 pins) | | |
| 100 | | | 3 × USARTs<br>3 × 16-bit timers<br>2 × SPIs, 2 × $I^2$Cs, USB, CAN, 1 × PWM timer<br>2 × ADC | | | | |
| 64 | 2 × USARTs<br>2 × 16-bit timers<br>1 × SPI, 1 × $I^2$C, USB, CAN, 1 × PWM timer<br>2 × ADCs | | | | | | |
| 48 | | | | | | | |
| 36 | | | | | | | |

1. For orderable part numbers that do not show the A internal code after the temperature range code (6 or 7), the reference datasheet for electrical characteristics is that of the STM32F103x8/B medium-density devices.

## 2.3 Overview

### 2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the device family.

### 2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

### 2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 2.3.4 Embedded SRAM

Twenty Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### 2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F103xx performance line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

### 2.3.22 ADC (analog-to-digital converter)

Two 12-bit analog-to-digital converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

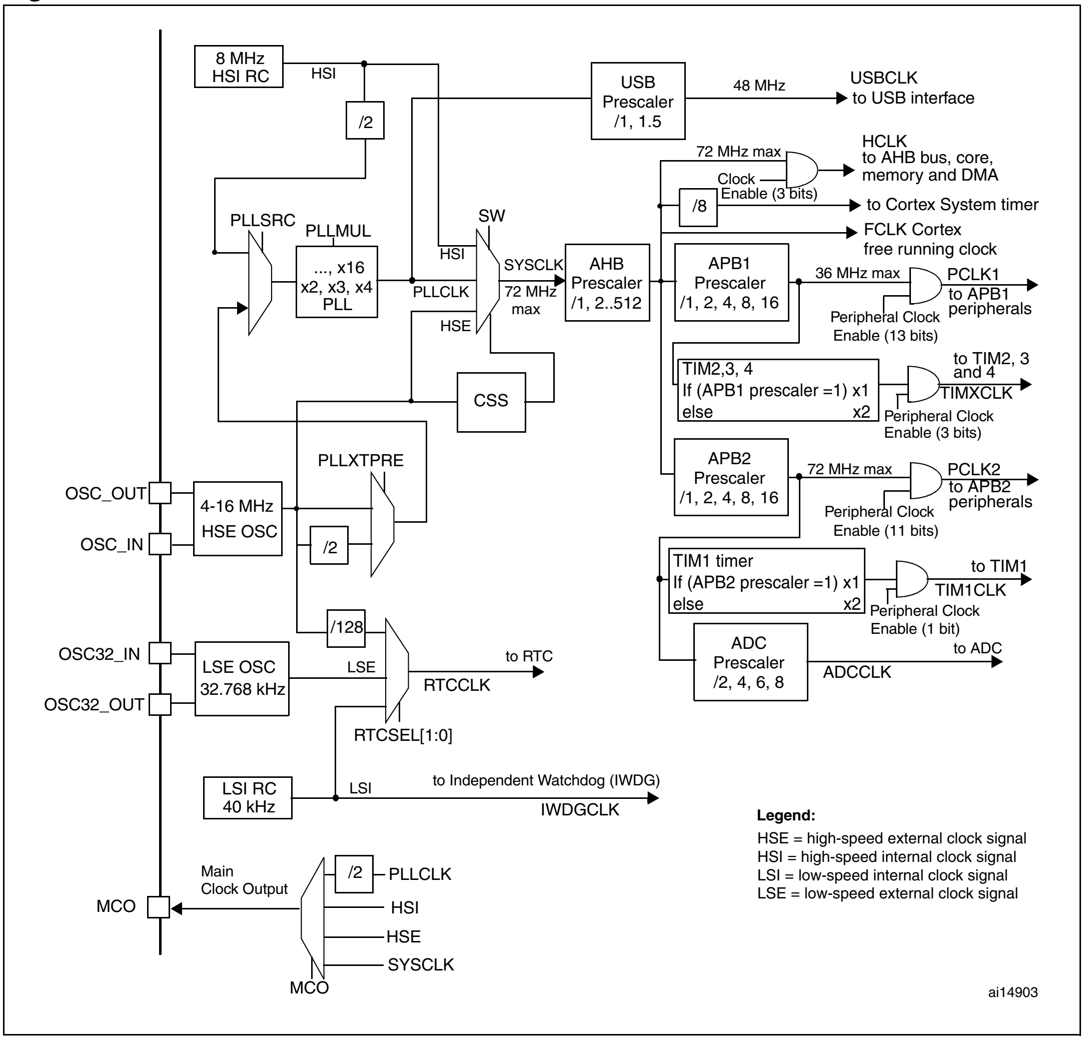
### 2.3.23 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < $V_{DDA}$ < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### 2.3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## Figure 2. Clock tree




1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 48 MHz or 72 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

**Table 5. Medium-density STM32F103xx pin definitions**

| Pins | | | | | | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LFBGA100 | LQFP48 | TFBGA64 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| A3 | - | | - | 1 | - | PE2 | I/O | FT | PE2 | TRACECK | |
| B3 | - | | - | 2 | - | PE3 | I/O | FT | PE3 | TRACED0 | |
| C3 | - | | - | 3 | - | PE4 | I/O | FT | PE4 | TRACED1 | |
| D3 | - | | - | 4 | - | PE5 | I/O | FT | PE5 | TRACED2 | |
| E3 | - | | - | 5 | - | PE6 | I/O | FT | PE6 | TRACED3 | |
| B2 | 1 | B2 | 1 | 6 | - | $V_{BAT}$ | S | | $V_{BAT}$ | | |
| A2 | 2 | A2 | 2 | 7 | - | PC13-TAMPER-RTC[4] | I/O | | PC13[5] | TAMPER-RTC | |
| A1 | 3 | A1 | 3 | 8 | - | PC14-OSC32_IN[4] | I/O | | PC14[5] | OSC32_IN | |
| B1 | 4 | B1 | 4 | 9 | - | PC15-OSC32_OUT[4] | I/O | | PC15[5] | OSC32_OUT | |
| C2 | - | - | - | 10 | - | $V_{SS\_5}$ | S | | $V_{SS\_5}$ | | |
| D2 | - | - | - | 11 | - | $V_{DD\_5}$ | S | | $V_{DD\_5}$ | | |
| C1 | 5 | C1 | 5 | 12 | 2 | OSC_IN | I | | OSC_IN | | |
| D1 | 6 | D1 | 6 | 13 | 3 | OSC_OUT | O | | OSC_OUT | | |
| E1 | 7 | E1 | 7 | 14 | 4 | NRST | I/O | | NRST | | |
| F1 | - | E3 | 8 | 15 | - | PC0 | I/O | | PC0 | ADC12_IN10 | |
| F2 | - | E2 | 9 | 16 | - | PC1 | I/O | | PC1 | ADC12_IN11 | |
| E2 | - | F2 | 10 | 17 | - | PC2 | I/O | | PC2 | ADC12_IN12 | |
| F3 | - | -[6] | 11 | 18 | - | PC3 | I/O | | PC3 | ADC12_IN13 | |
| G1 | 8 | F1 | 12 | 19 | 5 | $V_{SSA}$ | S | | $V_{SSA}$ | | |
| H1 | - | - | - | 20 | - | $V_{REF-}$ | S | | $V_{REF-}$ | | |
| J1 | - | G1[6] | - | 21 | - | $V_{REF+}$ | S | | $V_{REF+}$ | | |
| K1 | 9 | H1 | 13 | 22 | 6 | $V_{DDA}$ | S | | $V_{DDA}$ | | |
| G2 | 10 | G2 | 14 | 23 | 7 | PA0-WKUP | I/O | | PA0 | WKUP/ USART2_CTS[7]/ ADC12_IN0/ TIM2_CH1_ETR[7] | |
| H2 | 11 | H2 | 15 | 24 | 8 | PA1 | I/O | | PA1 | USART2_RTS[7]/ ADC12_IN1/ TIM2_CH2[7] | |
| J2 | 12 | F3 | 16 | 25 | 9 | PA2 | I/O | | PA2 | USART2_TX[7]/ ADC12_IN2/ TIM2_CH3[7] | |

**Figure 10. Pin loading conditions**

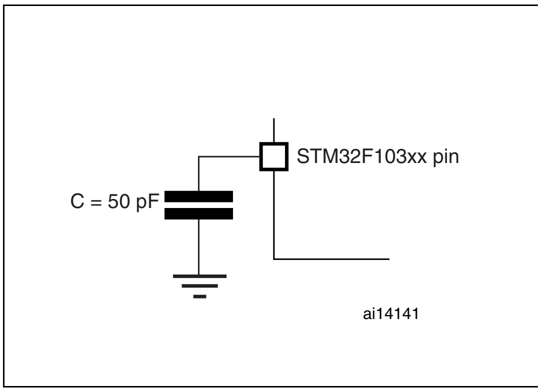
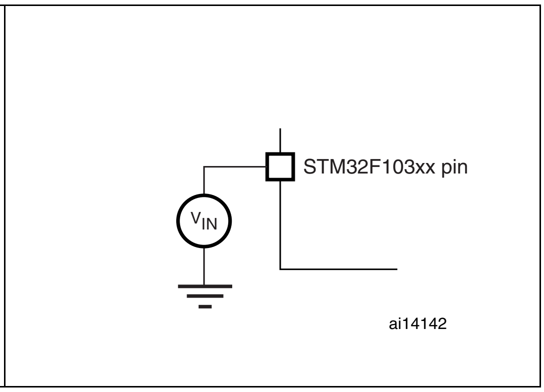
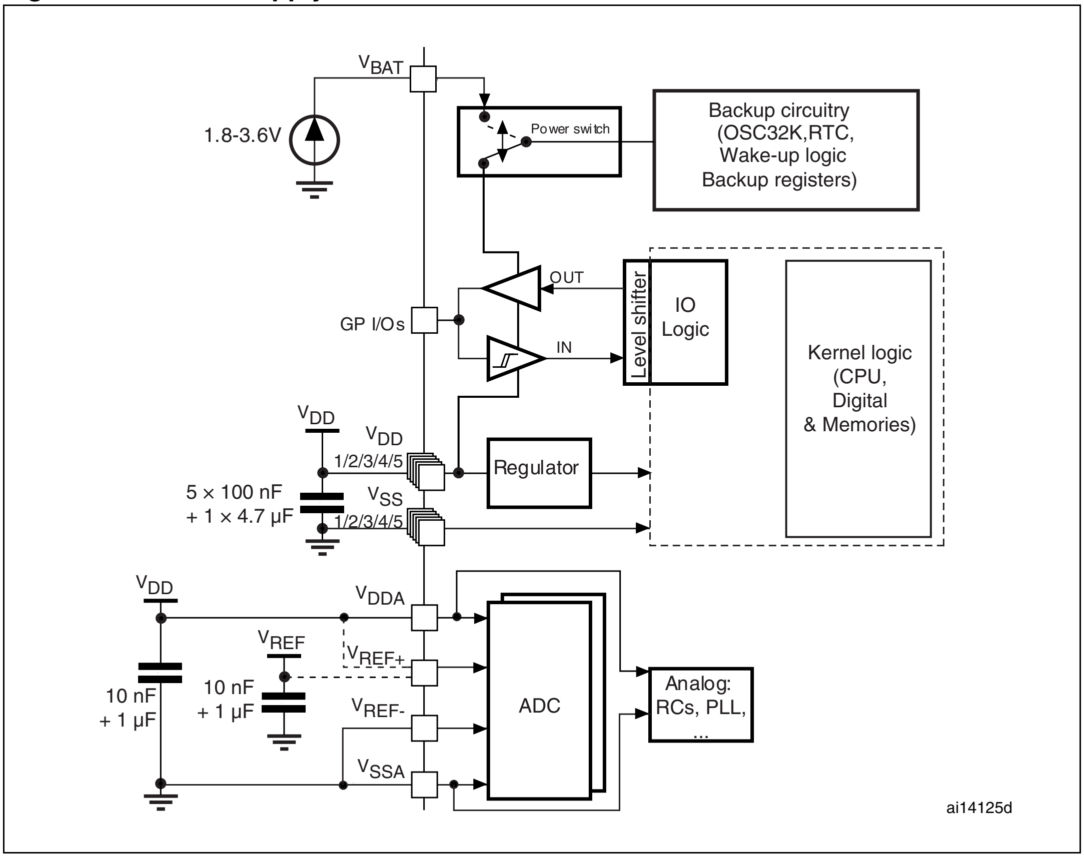



**Figure 11. Pin input voltage**




### 5.1.6 Power supply scheme

**Figure 12. Power supply scheme**




**Caution:** In *Figure 12*, the 4.7 μF capacitor must be connected to $V_{DD3}$.

**Table 7. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}/V_{DDA}$ power lines (source)(1) | 150 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)(1) | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | – 25 | |
| $I_{INJ(PIN)}$ (2)(3) | Injected current on NRST pin | ± 5 | |
| | Injected current on HSE OSC_IN and LSE OSC_IN pins | ± 5 | |
| | Injected current on any other pin(4) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$(2) | Total injected current (sum of all I/O and control pins)(4) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

**Table 8. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

## 5.3 Operating conditions

### 5.3.1 General operating conditions

**Table 9. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | | 0 | 72 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | | 0 | 72 | |
| $V_{DD}$ | Standard operating voltage | | 2 | 3.6 | V |
| $V_{DDA}$(1) | Analog operating voltage (ADC not used) | Must be the same potential as $V_{DD}$(2) | 2 | 3.6 | V |
| | Analog operating voltage (ADC used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | | 1.8 | 3.6 | V |

**Table 13. Maximum current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max[1] $T_A$ = 85 °C | Max[1] $T_A$ = 105 °C | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock[2], all peripherals enabled | 72 MHz | 50 | 50.3 | mA |
| | | | 48 MHz | 36.1 | 36.2 | |
| | | | 36 MHz | 28.6 | 28.7 | |
| | | | 24 MHz | 19.9 | 20.1 | |
| | | | 16 MHz | 14.7 | 14.9 | |
| | | | 8 MHz | 8.6 | 8.9 | |
| | | External clock[2], all peripherals disabled | 72 MHz | 32.8 | 32.9 | |
| | | | 48 MHz | 24.4 | 24.5 | |
| | | | 36 MHz | 19.8 | 19.9 | |
| | | | 24 MHz | 13.9 | 14.2 | |
| | | | 16 MHz | 10.7 | 11 | |
| | | | 8 MHz | 6.8 | 7.1 | |

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 14. Maximum current consumption in Run mode, code with data processing running from RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max[1] $T_A$ = 85 °C | Max[1] $T_A$ = 105 °C | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock[2], all peripherals enabled | 72 MHz | 48 | 50 | mA |
| | | | 48 MHz | 31.5 | 32 | |
| | | | 36 MHz | 24 | 25.5 | |
| | | | 24 MHz | 17.5 | 18 | |
| | | | 16 MHz | 12.5 | 13 | |
| | | | 8 MHz | 7.5 | 8 | |
| | | External clock[2], all peripherals disabled | 72 MHz | 29 | 29.5 | |
| | | | 48 MHz | 20.5 | 21 | |
| | | | 36 MHz | 16 | 16.5 | |
| | | | 24 MHz | 11.5 | 12 | |
| | | | 16 MHz | 8.5 | 9 | |
| | | | 8 MHz | 5.5 | 6 | |

1. Based on characterization, tested in production at $V_{DD}$ max, $f_{HCLK}$ max.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

Table 16. Typical and maximum current consumptions in Stop and Standby modes

| Symbol | Parameter | Conditions | Typ(1) | | Max | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}/V_{BAT}$ = 2.4 V | $V_{DD}/V_{BAT}$ = 3.3 V | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 23.5 | 24 | 200 | 370 | µA |
| | | Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 13.5 | 14 | 180 | 340 | |
| | Supply current in Standby mode | Low-speed internal RC oscillator and independent watchdog ON | 2.6 | 3.4 | - | - | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | 2.4 | 3.2 | - | - | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | 1.7 | 2 | 4 | 5 | |
| $I_{DD\_VBAT}$ | Backup domain supply current | Low-speed oscillator and RTC ON | 1.1 | 1.4 | 1.9(2) | 2.2 | |

1. Typical values are measured at $T_A$ = 25 °C.
2. Based on characterization, not tested in production.

Figure 16. Typical current consumption in Stop mode with regulator in Run mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V

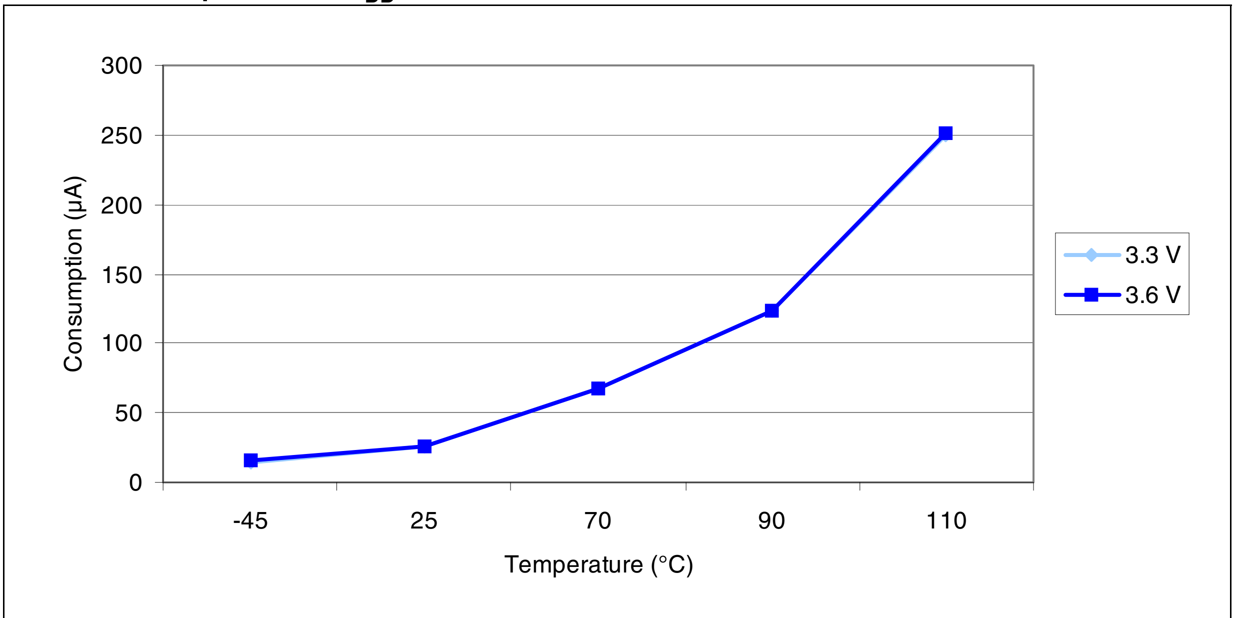


**Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ[1] | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled[2] | All peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode | External clock[3] | 72 MHz | 14.4 | 5.5 | mA |
| | | | 48 MHz | 9.9 | 3.9 | |
| | | | 36 MHz | 7.6 | 3.1 | |
| | | | 24 MHz | 5.3 | 2.3 | |
| | | | 16 MHz | 3.8 | 1.8 | |
| | | | 8 MHz | 2.1 | 1.2 | |
| | | | 4 MHz | 1.6 | 1.1 | |
| | | | 2 MHz | 1.3 | 1 | |
| | | | 1 MHz | 1.11 | 0.98 | |
| | | | 500 kHz | 1.04 | 0.96 | |
| | | | 125 kHz | 0.98 | 0.95 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 64 MHz | 12.3 | 4.4 | |
| | | | 48 MHz | 9.3 | 3.3 | |
| | | | 36 MHz | 7 | 2.5 | |
| | | | 24 MHz | 4.8 | 1.8 | |
| | | | 16 MHz | 3.2 | 1.2 | |
| | | | 8 MHz | 1.6 | 0.6 | |
| | | | 4 MHz | 1 | 0.5 | |
| | | | 2 MHz | 0.72 | 0.47 | |
| | | | 1 MHz | 0.56 | 0.44 | |
| | | | 500 kHz | 0.49 | 0.42 | |
| | | | 125 kHz | 0.43 | 0.41 | |

1. Typical values are measures at $T_A = 25\ °C$, $V_{DD} = 3.3\ V$.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

**Table 30. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 1000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz conforms to IEC 1000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

**Table 31. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | | Unit |
|---|---|---|---|---|---|---|
| | | | | 8/48 MHz | 8/72 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, LQFP100 package compliant with SAE J 1752/3 | 0.1 to 30 MHz | 12 | 12 | dBµV |
| | | | 30 to 130 MHz | 22 | 19 | |
| | | | 130 MHz to 1GHz | 23 | 29 | |
| | | | SAE EMI Level | 4 | 4 | - |

### 5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 32. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A = +25$ °C conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A = +25$ °C conforming to JESD22-C101 | II | 500 | |

1. Based on characterization results, not tested in production.

#### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 33. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A = +105$ °C conforming to JESD78A | II level A |

## 5.3.15 Communications interfaces

### I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature, $f_{PCLK1}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

The STM32F103xx performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 39. I²C characteristics**

| Symbol | Parameter | Standard mode I²C(1) | | Fast mode I²C(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20 + 0.1C_b$ | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | | 0.6 | | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | µs |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

1. Guaranteed by design, not tested in production.
2. $f_{PCLK1}$ must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

**Equation 1: $R_{AIN}$ max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 46. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 1.2 |
| 7.5 | 0.54 | 10 |
| 13.5 | 0.96 | 19 |
| 28.5 | 2.04 | 41 |
| 41.5 | 2.96 | 60 |
| 55.5 | 3.96 | 80 |
| 71.5 | 5.11 | 104 |
| 239.5 | 17.1 | 350 |

1. Based on characterization, not tested in production.

**Table 47. ADC accuracy - limited test conditions(1) (2)**

| Symbol | Parameter | Test conditions | Typ | Max(3) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz,<br>$f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ,<br>$V_{DDA}$ = 3 V to 3.6 V<br>$T_A$ = 25 °C<br>Measurements made after ADC calibration | ±1.3 | ±2 | LSB |
| EO | Offset error | | ±1 | ±1.5 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

### Table 48. ADC accuracy(1) (2) (3)

| Symbol | Parameter | Test conditions | Typ | Max(4) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 2.4 V to 3.6 V Measurements made after ADC calibration | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

### Figure 30. ADC accuracy characteristics

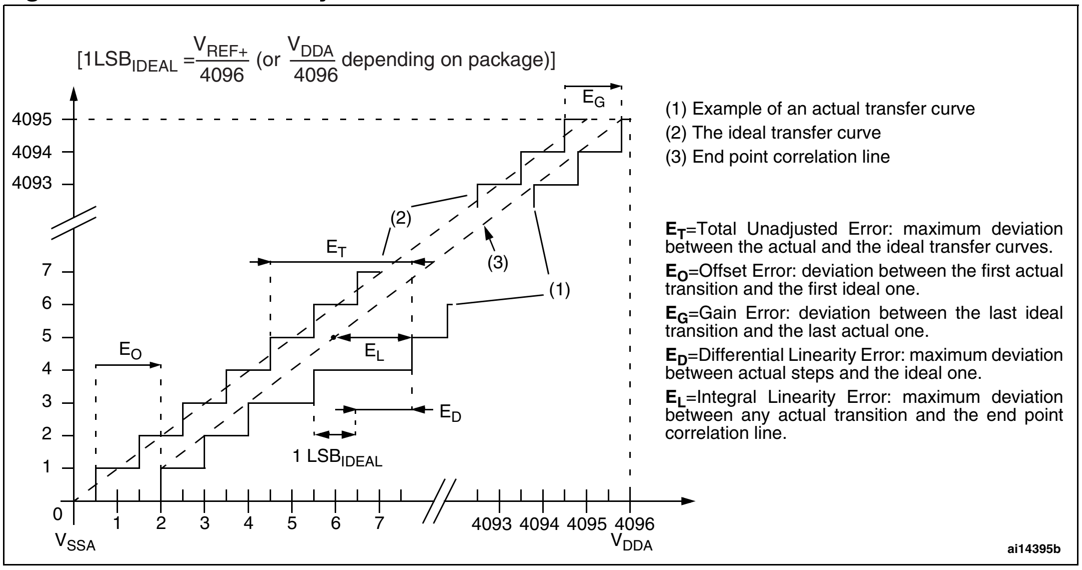


Figure 44. LQFP48, 48-pin low-profile quad flat package outline(1)

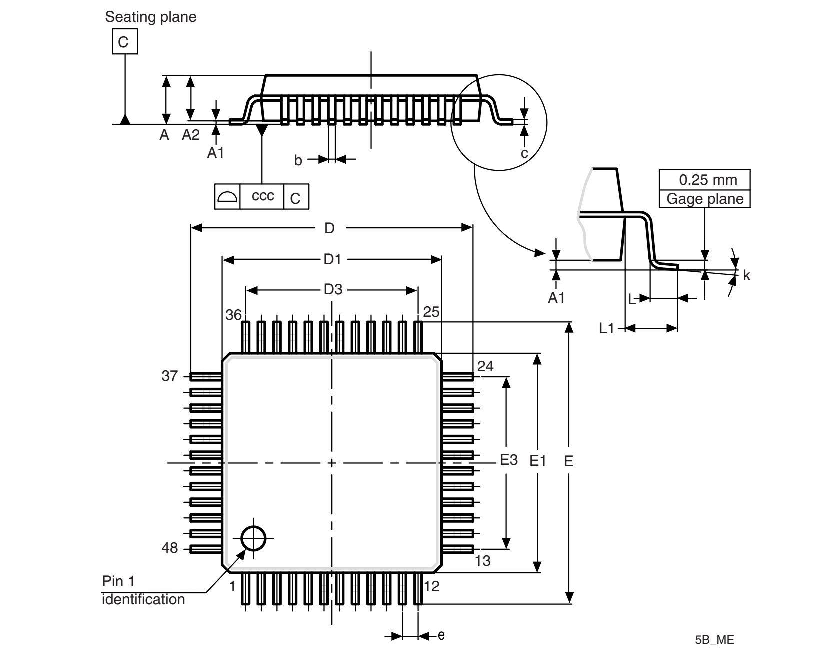
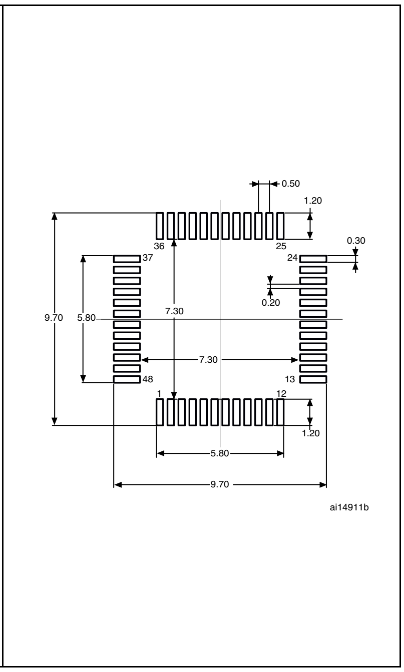



Figure 45. Recommended footprint(1)(2)




1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 55. LQFP48, 48-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | | 0.050 | 0.150 | | 0.0020 | 0.0059 |
| A2 | 1.400 | 1.350 | 1.450 | 0.0551 | 0.0531 | 0.0571 |
| b | 0.220 | 0.170 | 0.270 | 0.0087 | 0.0067 | 0.0106 |
| c | | 0.090 | 0.200 | | 0.0035 | 0.0079 |
| D | 9.000 | 8.800 | 9.200 | 0.3543 | 0.3465 | 0.3622 |
| D1 | 7.000 | 6.800 | 7.200 | 0.2756 | 0.2677 | 0.2835 |
| D3 | 5.500 | | | 0.2165 | | |
| E | 9.000 | 8.800 | 9.200 | 0.3543 | 0.3465 | 0.3622 |
| E1 | 7.000 | 6.800 | 7.200 | 0.2756 | 0.2677 | 0.2835 |
| E3 | 5.500 | | | 0.2165 | | |
| e | 0.500 | | | 0.0197 | | |
| L | 0.600 | 0.450 | 0.750 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.000 | | | 0.0394 | | |
| k | 3.5° | 0° | 7° | 3.5° | 0° | 7° |
| ccc | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

### 6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 57: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

#### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW:

$P_{Dmax}$ = 175 + 272 = 447 mW

Thus: $P_{Dmax}$ = 447 mW

Using the values obtained in *Table 56* $T_{Jmax}$ is calculated as follows:

– For LQFP100, 46 °C/W

$T_{Jmax}$ = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 57: Ordering information scheme*).

#### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 115 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 20 mA × 3.5 V= 70 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW

# 8 Revision history

Table 58. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 01-jun-2007 | 1 | Initial release. |
| 20-Jul-2007 | 2 | Flash memory size modified in *Note 7*, *Note 4*, *Note 7*, *Note 8* and BGA100 pins added to *Table 5: Medium-density STM32F103xx pin definitions*. *Figure 3: STM32F103xx performance line LFBGA100 ballout* added.<br>$T_{HSE}$ changed to $T_{LSE}$ in *Figure 20: Low-speed external clock source AC timing diagram*. $V_{BAT}$ ranged modified in *Power supply schemes*.<br>$t_{SU(LSE)}$ changed to $t_{SU(HSE)}$ in *Table 22: HSE 4-16 MHz oscillator characteristics*. $I_{DD(HSI)}$ max value added to *Table 24: HSI oscillator characteristics*.<br>Sample size modified and machine model removed in *Electrostatic discharge (ESD)*.<br>Number of parts modified and standard reference updated in *Static latch-up*. 25 °C and 85 °C conditions removed and class name modified in *Table 33: Electrical sensitivities*. $R_{PU}$ and $R_{PD}$ min and max values added to *Table 34: I/O static characteristics*. $R_{PU}$ min and max values added to *Table 37: NRST pin characteristics*.<br>*Figure 25: I²C bus AC waveforms and measurement circuit* and *Figure 24: Recommended NRST pin protection* corrected.<br>Notes removed below *Table 9*, *Table 37*, *Table 43*.<br>$I_{DD}$ typical values changed in *Table 11: Maximum current consumption in Run and Sleep modes*. *Table 38: TIMx characteristics* modified.<br>$t_{STAB}$, $V_{REF+}$ value, $t_{lat}$ and $f_{TRIG}$ added to *Table 45: ADC characteristics*.<br>In *Table 29: Flash memory endurance and data retention*, typical endurance and data retention for $T_A$ = 85 °C added, data retention for $T_A$ = 25 °C removed.<br>$V_{BG}$ changed to $V_{REFINT}$ in *Table 12: Embedded internal reference voltage*. Document title changed. *Controller area network (CAN)* section modified.<br>*Figure 12: Power supply scheme* modified.<br>*Features on page 1* list optimized. Small text changes. |