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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rbt7tr |

# List of figures

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x8 and STM32F103xB medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

# 2 Description

The STM32F103x8 and STM32F103xB performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two $I^2C$s and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx medium-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

*Figure 1* shows the general block diagram of the device family.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

### 2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

### 2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

### 2.3.9 Power supply schemes

- $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to $V_{DDA}$ is 2.4 V when the ADC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 12: Power supply scheme*.

### 2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to *Table 11: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

### 2.3.12 Low-power modes

The STM32F103xx performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

**Figure 5. STM32F103xx performance line LQFP64 pinout**

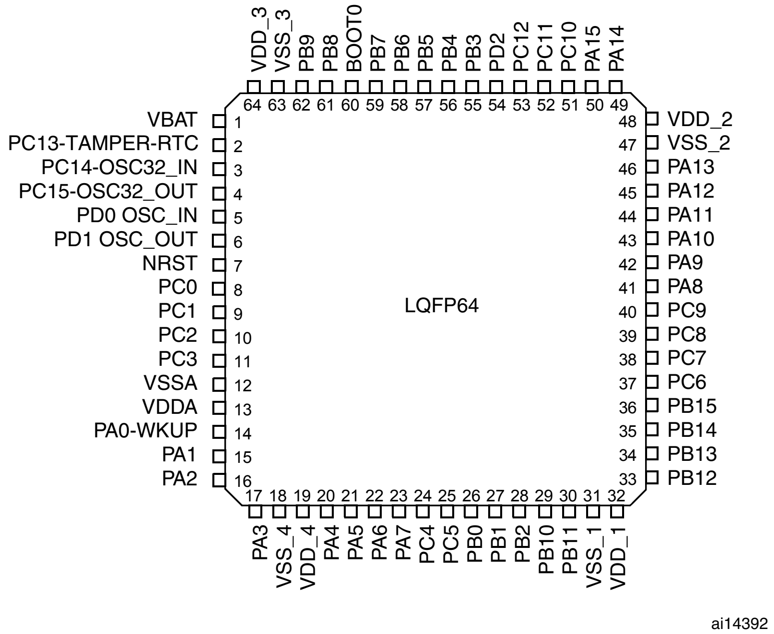


**Table 5. Medium-density STM32F103xx pin definitions (continued)**

| Pins | | | | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **LFBGA100** | **LQFP48** | **TFBGA64** | **LQFP64** | **LQFP100** | **VFQFPN36** | | | | | **Default** | **Remap** |
| K2 | 13 | G3 | 17 | 26 | 10 | PA3 | I/O | | PA3 | USART2_RX(7)/<br>ADC12_IN3/<br>TIM2_CH4(7) | |
| E4 | - | C2 | 18 | 27 | - | $V_{SS\_4}$ | S | | $V_{SS\_4}$ | | |
| F4 | - | D2 | 19 | 28 | - | $V_{DD\_4}$ | S | | $V_{DD\_4}$ | | |
| G3 | 14 | H3 | 20 | 29 | 11 | PA4 | I/O | | PA4 | SPI1_NSS(7)/<br>USART2_CK(7)/<br>ADC12_IN4 | |
| H3 | 15 | F4 | 21 | 30 | 12 | PA5 | I/O | | PA5 | SPI1_SCK(7)/<br>ADC12_IN5 | |
| J3 | 16 | G4 | 22 | 31 | 13 | PA6 | I/O | | PA6 | SPI1_MISO(7)/<br>ADC12_IN6/<br>TIM3_CH1(7) | TIM1_BKIN |
| K3 | 17 | H4 | 23 | 32 | 14 | PA7 | I/O | | PA7 | SPI1_MOSI(7)/<br>ADC12_IN7/<br>TIM3_CH2(7) | TIM1_CH1N |
| G4 | - | H5 | 24 | 33 | | PC4 | I/O | | PC4 | ADC12_IN14 | |
| H4 | - | H6 | 25 | 34 | | PC5 | I/O | | PC5 | ADC12_IN15 | |
| J4 | 18 | F5 | 26 | 35 | 15 | PB0 | I/O | | PB0 | ADC12_IN8/<br>TIM3_CH3(7) | TIM1_CH2N |
| K4 | 19 | G5 | 27 | 36 | 16 | PB1 | I/O | | PB1 | ADC12_IN9/<br>TIM3_CH4(7) | TIM1_CH3N |
| G5 | 20 | G6 | 28 | 37 | 17 | PB2 | I/O | FT | PB2/BOOT1 | | |
| H5 | - | - | - | 38 | - | PE7 | I/O | FT | PE7 | | TIM1_ETR |
| J5 | - | - | - | 39 | - | PE8 | I/O | FT | PE8 | | TIM1_CH1N |
| K5 | - | - | - | 40 | - | PE9 | I/O | FT | PE9 | | TIM1_CH1 |
| G6 | - | - | - | 41 | - | PE10 | I/O | FT | PE10 | | TIM1_CH2N |
| H6 | - | - | - | 42 | - | PE11 | I/O | FT | PE11 | | TIM1_CH2 |
| J6 | - | - | - | 43 | - | PE12 | I/O | FT | PE12 | | TIM1_CH3N |
| K6 | - | - | - | 44 | - | PE13 | I/O | FT | PE13 | | TIM1_CH3 |
| G7 | - | - | - | 45 | - | PE14 | I/O | FT | PE14 | | TIM1_CH4 |
| H7 | - | - | - | 46 | - | PE15 | I/O | FT | PE15 | | TIM1_BKIN |
| J7 | 21 | G7 | 29 | 47 | - | PB10 | I/O | FT | PB10 | I2C2_SCL/<br>USART3_TX(7) | TIM2_CH3 |
| K7 | 22 | H7 | 30 | 48 | - | PB11 | I/O | FT | PB11 | I2C2_SDA/<br>USART3_RX(7) | TIM2_CH4 |
| E7 | 23 | D6 | 31 | 49 | 18 | $V_{SS\_1}$ | S | | $V_{SS\_1}$ | | |

**Table 5. Medium-density STM32F103xx pin definitions (continued)**

| Pins | | | | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LFBGA100 | LQFP48 | TFBGA64 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| D4 | - | - | - | 97 | - | PE0 | I/O | FT | PE0 | TIM4_ETR | |
| C4 | - | - | - | 98 | - | PE1 | I/O | FT | PE1 | | |
| E5 | 47 | D4 | 63 | 99 | 36 | $V_{SS\_3}$ | S | | $V_{SS\_3}$ | | |
| F5 | 48 | E4 | 64 | 100 | 1 | $V_{DD\_3}$ | S | | $V_{DD\_3}$ | | |

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 10*.
4. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 is restricted: only one I/O at a time can be used as an output, the speed has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The $V_{REF+}$ functionality is provided instead.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
8. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages, and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
   The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

**Figure 10. Pin loading conditions**

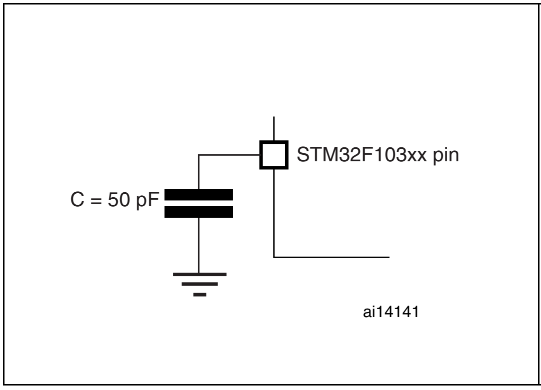
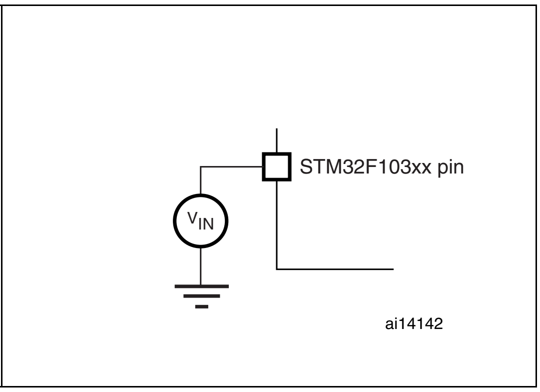
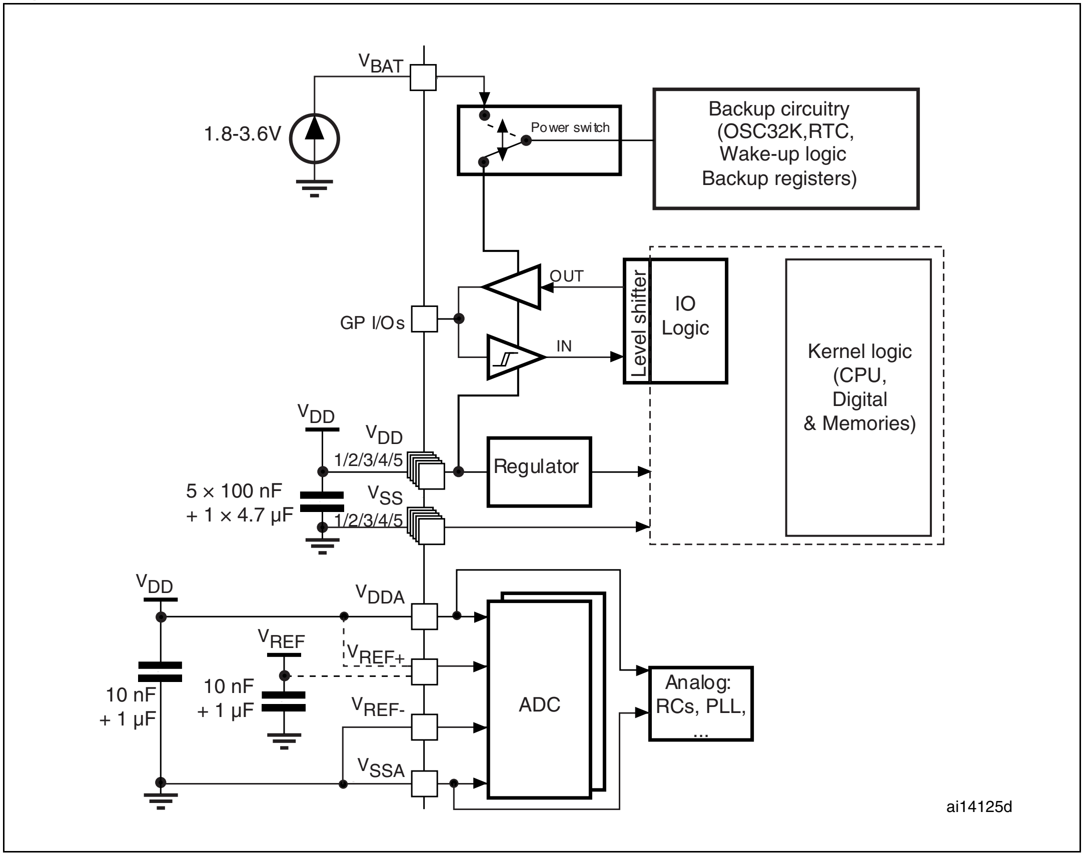


**Figure 11. Pin input voltage**



## 5.1.6 Power supply scheme

**Figure 12. Power supply scheme**



**Caution:** In *Figure 12*, the 4.7 µF capacitor must be connected to $V_{DD3}$.

### Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

**Table 17. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ[1] All peripherals enabled[2] | Typ[1] All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock[3] | 72 MHz | 36 | 27 | mA |
| | | | 48 MHz | 24.2 | 18.6 | |
| | | | 36 MHz | 19 | 14.8 | |
| | | | 24 MHz | 12.9 | 10.1 | |
| | | | 16 MHz | 9.3 | 7.4 | |
| | | | 8 MHz | 5.5 | 4.6 | |
| | | | 4 MHz | 3.3 | 2.8 | |
| | | | 2 MHz | 2.2 | 1.9 | |
| | | | 1 MHz | 1.6 | 1.45 | |
| | | | 500 kHz | 1.3 | 1.25 | |
| | | | 125 kHz | 1.08 | 1.06 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 64 MHz | 31.4 | 23.9 | mA |
| | | | 48 MHz | 23.5 | 17.9 | |
| | | | 36 MHz | 18.3 | 14.1 | |
| | | | 24 MHz | 12.2 | 9.5 | |
| | | | 16 MHz | 8.5 | 6.8 | |
| | | | 8 MHz | 4.9 | 4 | |
| | | | 4 MHz | 2.7 | 2.2 | |
| | | | 2 MHz | 1.6 | 1.4 | |
| | | | 1 MHz | 1.02 | 0.9 | |
| | | | 500 kHz | 0.73 | 0.67 | |
| | | | 125 kHz | 0.5 | 0.48 | |

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

1. Guaranteed by design, not tested in production.

**Figure 19. High-speed external clock source AC timing diagram**

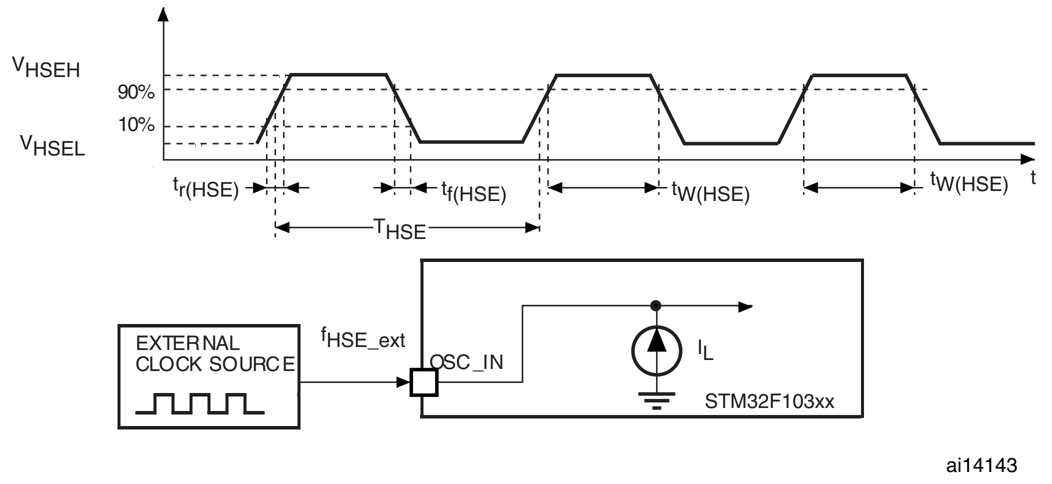
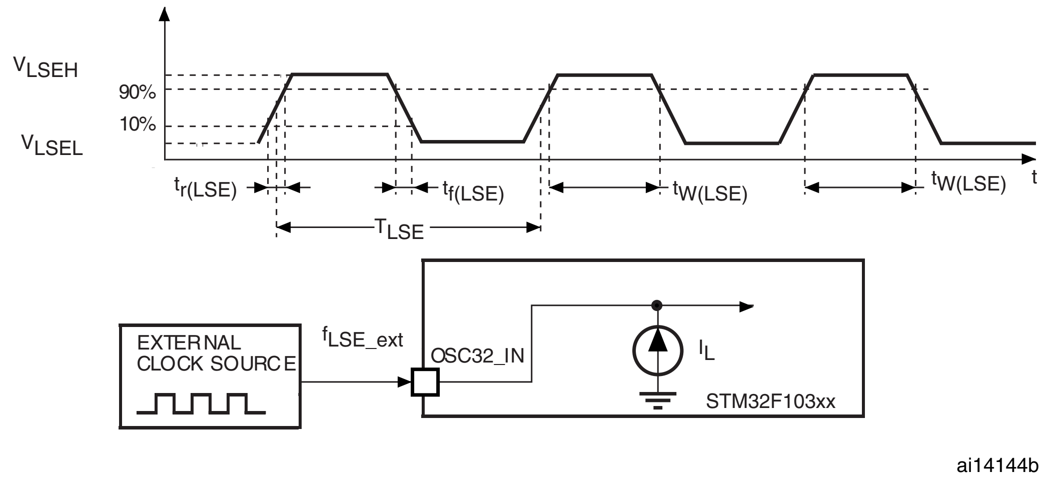


**Figure 20. Low-speed external clock source AC timing diagram**



## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

### High-speed internal (HSI) RC oscillator

**Table 24. HSI oscillator characteristics(1) (2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | | | 8 | | MHz |
| $ACC_{HSI}$ | Accuracy of HSI oscillator | $T_A$ = –40 to 105 °C | –2 | ±1 | 2.5 | % |
| | | $T_A$ = –10 to 85 °C | –1.5 | ±1 | 2.2 | % |
| | | $T_A$ = 0 to 70 °C | –1.3 | ±1 | 2 | % |
| | | $T_A$ = 25 °C | –1.1 | ±1 | 1.8 | % |
| $t_{su(HSI)}$ | HSI oscillator startup time | | 1 | | 2 | µs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 80 | 100 | µA |

1. Guaranteed by design, not tested in production.
2. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.

### Low-speed internal (LSI) RC oscillator

**Table 25. LSI oscillator characteristics (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(2) | Frequency | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | | | 85 | µs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | | 0.65 | 1.2 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

### Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

### 5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 32. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value[1] | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A = +25$ °C conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A = +25$ °C conforming to JESD22-C101 | II | 500 | |

1. Based on characterization results, not tested in production.

#### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 33. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A = +105$ °C conforming to JESD78A | II level A |

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed $V_{OL}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 7*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 7*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

**Table 35. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | TTL port<br>$I_{IO}$ = +8 mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$(2) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–0.4 | | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | CMOS port<br>$I_{IO}$ =+ 8mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$ (2) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | 2.4 | | |
| $V_{OL}$(1)(3) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO}$ = +20 mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 1.3 | V |
| $V_{OH}$(2)(3) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–1.3 | | |
| $V_{OL}$(1)(3) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO}$ = +6 mA<br>2 V < $V_{DD}$ < 2.7 V | | 0.4 | V |
| $V_{OH}$(2)(3) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–0.4 | | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
3. Based on characterization data, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 23* and *Table 36*, respectively.

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 36. I/O AC characteristics(1)**

| MODEx[1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 10 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 125(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 125(3) | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 25(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 25(3) | |
| 11 | $F_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 30 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 20 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5(3) | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12(3) | |
| | $t_{r(IO)out}$ | Output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12(3) | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | | ns |

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 23*.
3. Guaranteed by design, not tested in production.

### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 41. SPI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 18 | MHz |
| | | Slave mode | 0 | 18 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 8 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 $t_{PCLK}$ | | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 73 | | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$ (2) | Data input setup time Master mode | SPI1 | 1 | | |
| | | SPI2 | 5 | | |
| $t_{su(SI)}$(2) | Data input setup time Slave mode | | 1 | | |
| $t_{h(MI)}$ (2) | Data input hold time Master mode | SPI1 | 1 | | |
| | | SPI2 | 5 | | |
| $t_{h(SI)}$(2) | Data input hold time Slave mode | | 3 | | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 0 | 55 | |
| | | Slave mode, $f_{PCLK}$ = 24 MHz | 0 | 4 $t_{PCLK}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 10 | | |
| $t_{v(SO)}$ (2)(1) | Data output valid time | Slave mode (after enable edge) | | 25 | |
| $t_{v(MO)}$(2)(1) | Data output valid time | Master mode (after enable edge) | | 3 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 25 | | |
| $t_{h(MO)}$(2) | | Master mode (after enable edge) | 4 | | |

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

**Figure 26. SPI timing diagram - slave mode and CPHA = 0**

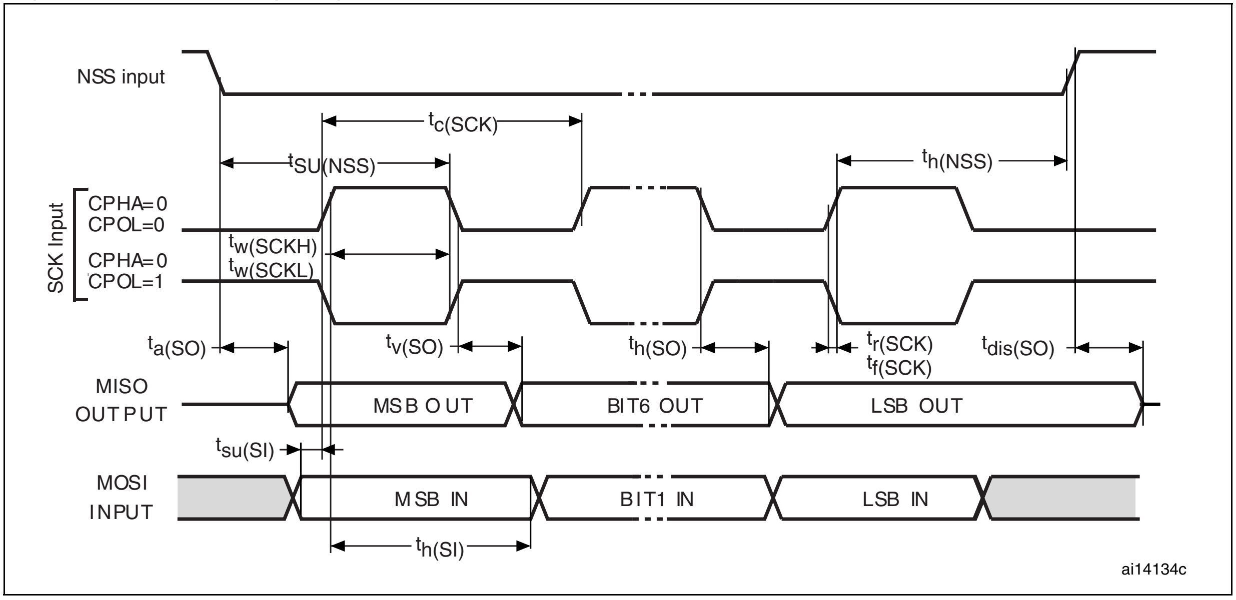
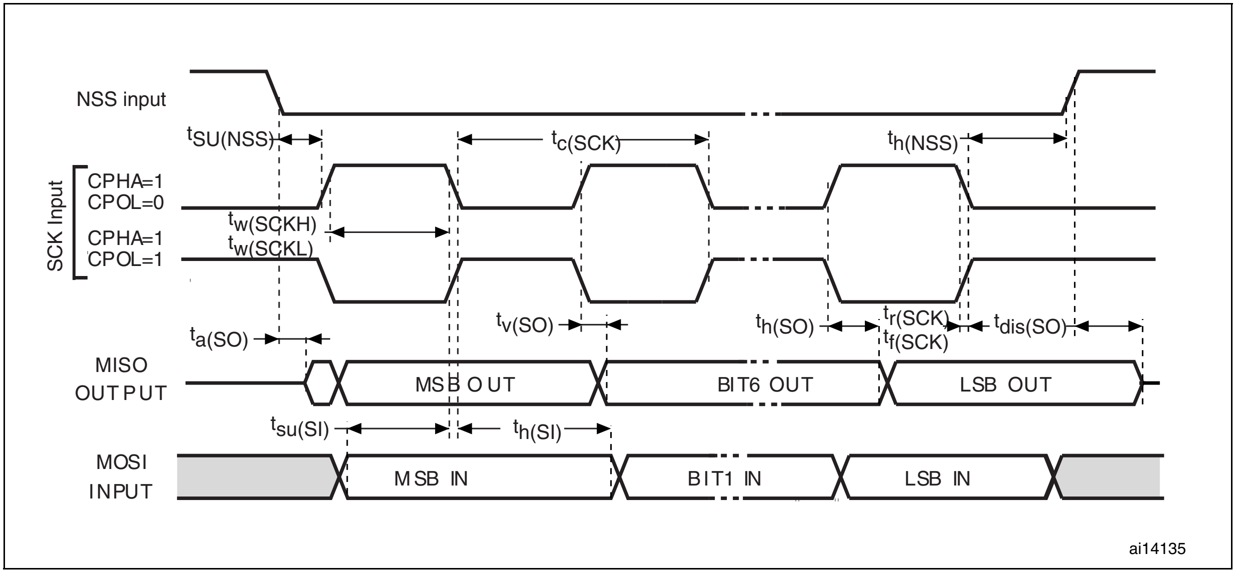
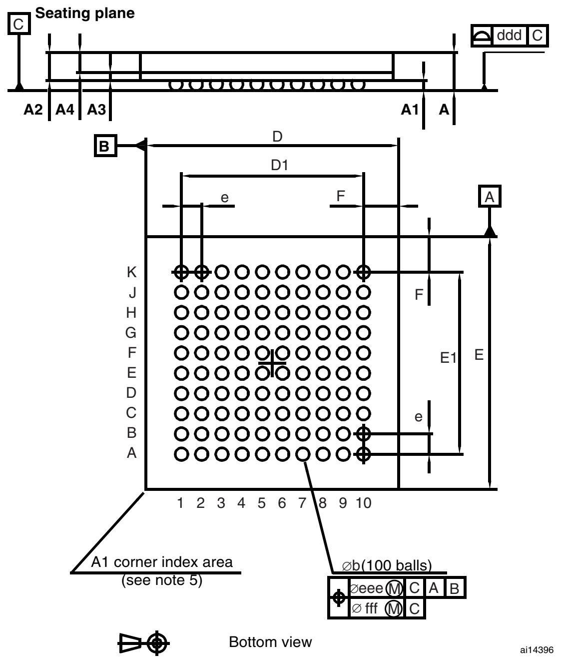


**Figure 27. SPI timing diagram - slave mode and CPHA = 1(1)**



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

### Figure 36. LFBGA100 - low profile fine pitch ball grid array package outline



1. Drawing is not to scale.

### Table 51. LFBGA100 - low profile fine pitch ball grid array package mechanical data

| Dim. | mm | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.700 | | | 0.0669 |
| A1 | 0.270 | | | 0.0106 | | |
| A2 | | 1.085 | | | 0.0427 | |
| A3 | | 0.30 | | | 0.0118 | |
| A4 | | | 0.80 | | | 0.0315 |
| b | 0.45 | 0.50 | 0.55 | 0.0177 | 0.0197 | 0.0217 |
| D | 9.85 | 10.00 | 10.15 | 0.3878 | 0.3937 | 0.3996 |
| D1 | | 7.20 | | | 0.2835 | |
| E | 9.85 | 10.00 | 10.15 | 0.3878 | 0.3937 | 0.3996 |
| E1 | | 7.20 | | | 0.2835 | |
| e | | 0.80 | | | 0.0315 | |
| F | | 1.40 | | | 0.0551 | |
| ddd | | | 0.12 | | | 0.0047 |
| eee | | | 0.15 | | | 0.0059 |
| fff | | | 0.08 | | | 0.0031 |
| N (number of balls) | 100 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

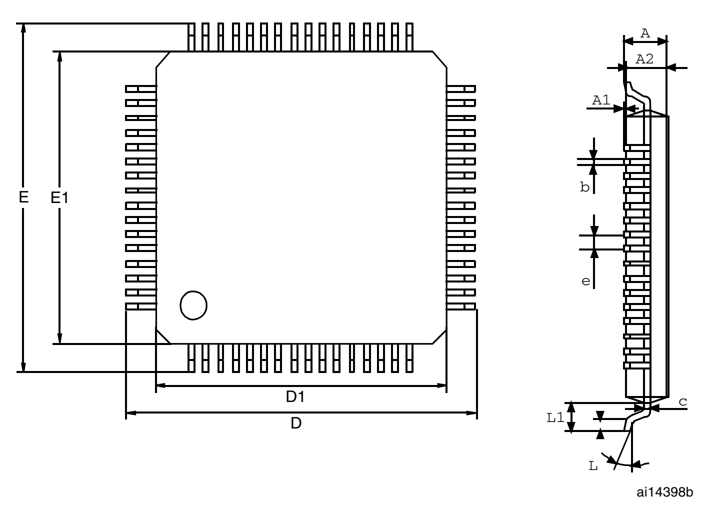


**Figure 40. LQFP64, 64-pin low-profile quad flat package outline**[1]

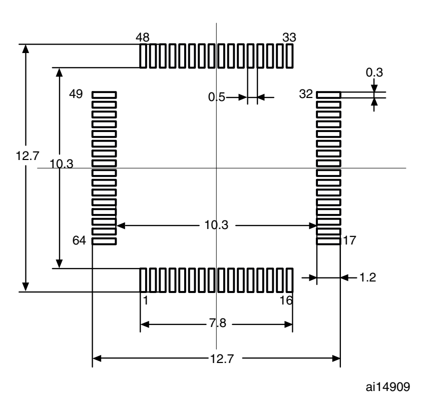


**Figure 41. Recommended footprint**[1][2]

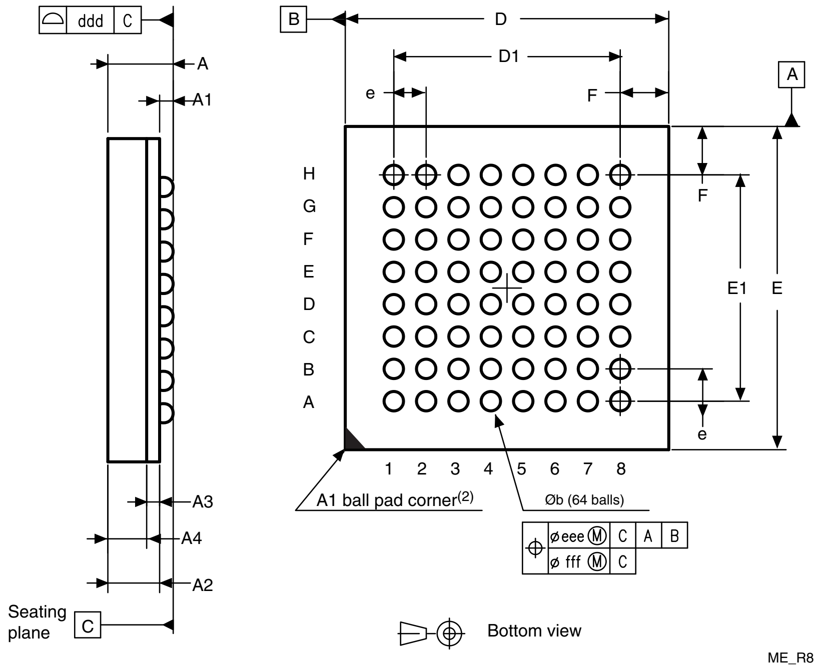
1. Drawing is not to scale.
2. Dimensions are in millimeters.

**Table 53. LQFP64, 64-pin low-profile quad flat package mechanical data**

| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.0630 |
| A1 | 0.05 | | 0.15 | 0.0020 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | | 12.00 | | | 0.4724 | |
| D1 | | 10.00 | | | 0.3937 | |
| E | | 12.00 | | | 0.4724 | |
| E1 | | 10.00 | | | 0.3937 | |
| e | | 0.50 | | | 0.0197 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| N | **Number of pins** | | | | | |
| | 64 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

### Figure 42. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package outline



1. Drawing is not to scale.

### Table 54. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.150 | | | 0.0059 | |
| A2 | 0.785 | | | 0.0309 | | |
| A3 | 0.200 | | | 0.0079 | | |
| A4 | | | 0.600 | | | 0.0236 |
| b | 0.300 | 0.250 | 0.350 | 0.0118 | 0.0098 | 0.0138 |
| D | 5.000 | 4.850 | 5.150 | 0.1969 | 0.1909 | 0.2028 |
| D1 | 3.500 | | | 0.1378 | | |
| E | 5.000 | 4.850 | 5.150 | 0.1969 | 0.1909 | 0.2028 |
| E1 | 3.500 | | | 0.1378 | | |
| e | 0.500 | | | 0.0197 | | |
| F | 0.750 | | | 0.0295 | | |
| ddd | 0.080 | | | 0.0031 | | |
| eee | 0.150 | | | 0.0059 | | |
| fff | 0.050 | | | 0.0020 | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 35*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 56. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>LFBGA100 - 10 × 10 mm / 0.8 mm pitch | 44 | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | |
| | **Thermal resistance junction-ambient**<br>LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | |
| | **Thermal resistance junction-ambient**<br>TFBGA64 - 5 × 5 mm / 0.5 mm pitch | 65 | |
| | **Thermal resistance junction-ambient**<br>LQFP48 - 7 x 7 mm / 0.5 mm pitch | 55 | |
| | **Thermal resistance junction-ambient**<br>VFQFPN 36 - 6 × 6 mm / 0.5 mm pitch | 18 | |

### 6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.