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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFQFN Exposed Pad
Supplier Device Package	36-VFQFPN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103t8u7tr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x8 and STM32F103xB medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F103x8 and STM32F103xB performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx medium-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.

2.3 Overview

2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

Twenty Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F103xx performance line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.3.16 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.17 Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

2.3.18 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

2.3.19 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.20 Universal serial bus (USB)

The STM32F103xx performance line embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3 Pinouts and pin description

Figure 3. STM32F103xx performance line LFBGA100 ballout

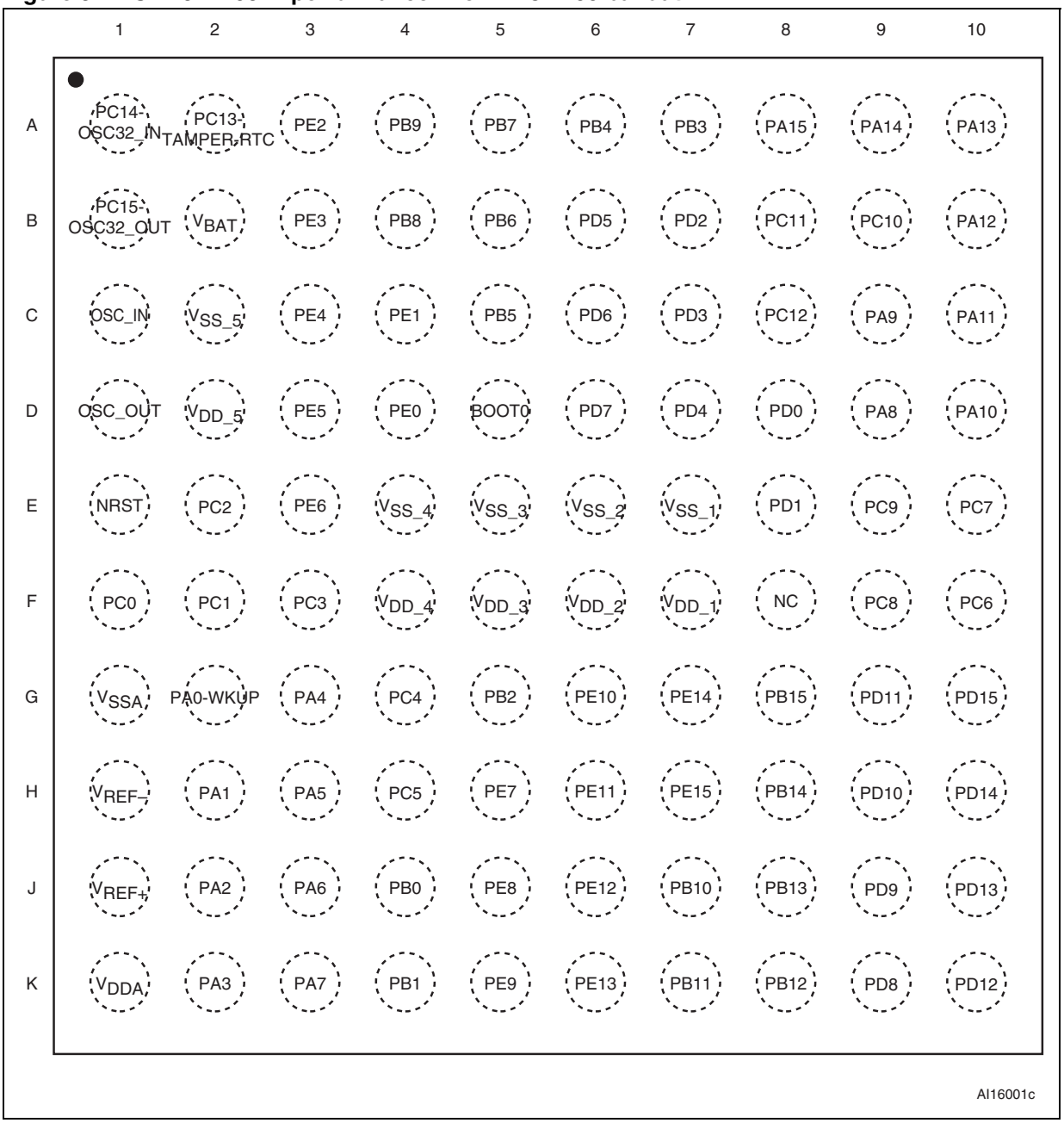


Figure 5. STM32F103xx performance line LQFP64 pinout

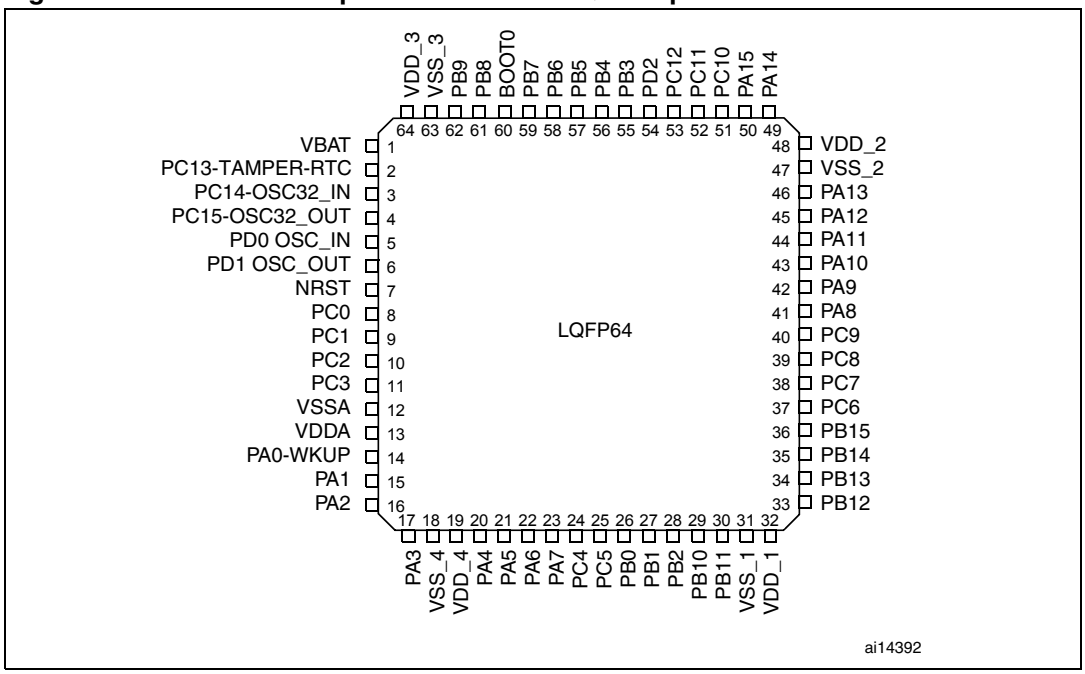


Figure 6. STM32F103xx performance line TFBGA64 ballout

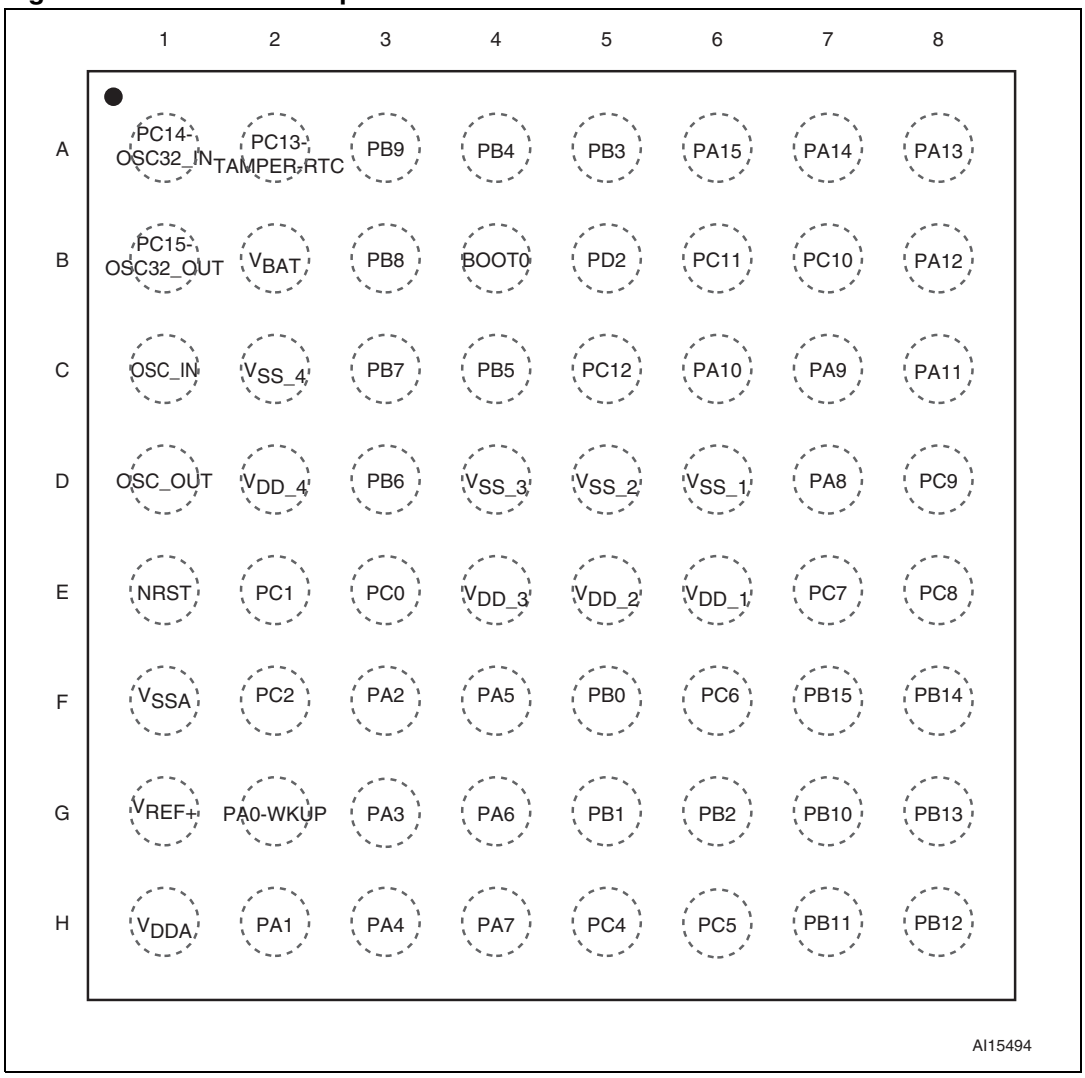


Table 5. Medium-density STM32F103xx pin definitions

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A3	-		-	1	-	PE2	I/O	FT	PE2	TRACECK	
B3	-		-	2	-	PE3	I/O	FT	PE3	TRACED0	
C3	-		-	3	-	PE4	I/O	FT	PE4	TRACED1	
D3	-		-	4	-	PE5	I/O	FT	PE5	TRACED2	
E3	-		-	5	-	PE6	I/O	FT	PE6	TRACED3	
B2	1	B2	1	6	-	V_{BAT}	S		V_{BAT}		
A2	2	A2	2	7	-	PC13-TAMPER-RTC(4)	I/O		PC13(5)	TAMPER-RTC	
A1	3	A1	3	8	-	PC14-OSC32_IN(4)	I/O		PC14(5)	OSC32_IN	
B1	4	B1	4	9	-	PC15-OSC32_OUT(4)	I/O		PC15(5)	OSC32_OUT	
C2	-	-	-	10	-	V_{SS_5}	S		V_{SS_5}		
D2	-	-	-	11	-	V_{DD_5}	S		V_{DD_5}		
C1	5	C1	5	12	2	OSC_IN	I		OSC_IN		
D1	6	D1	6	13	3	OSC_OUT	O		OSC_OUT		
E1	7	E1	7	14	4	NRST	I/O		NRST		
F1	-	E3	8	15	-	PC0	I/O		PC0	ADC12_IN10	
F2	-	E2	9	16	-	PC1	I/O		PC1	ADC12_IN11	
E2	-	F2	10	17	-	PC2	I/O		PC2	ADC12_IN12	
F3	-	-(6)	11	18	-	PC3	I/O		PC3	ADC12_IN13	
G1	8	F1	12	19	5	V_{SSA}	S		V_{SSA}		
H1	-	-	-	20	-	V_{REF-}	S		V_{REF-}		
J1	-	G1(6)	-	21	-	V_{REF+}	S		V_{REF+}		
K1	9	H1	13	22	6	V_{DDA}	S		V_{DDA}		
G2	10	G2	14	23	7	PA0-WKUP	I/O		PA0	WKUP/ USART2_CTS(7)/ ADC12_IN0/ TIM2_CH1_ETR(7)	
H2	11	H2	15	24	8	PA1	I/O		PA1	USART2_RTS(7)/ ADC12_IN1/ TIM2_CH2(7)	
J2	12	F3	16	25	9	PA2	I/O		PA2	USART2_TX(7)/ ADC12_IN2/ TIM2_CH3(7)	

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
F7	24	E6	32	50	19	V_{DD_1}	S		V_{DD_1}		
K8	25	H8	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK(7)/ TIM1_BKIN(7)	
J8	26	G8	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(7)/ TIM1_CH1N (7)	
H8	27	F8	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(7) TIM1_CH2N (7)	
G8	28	F7	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(7)	
K9	-	-	-	55	-	PD8	I/O	FT	PD8		USART3_TX
J9	-	-	-	56	-	PD9	I/O	FT	PD9		USART3_RX
H9	-	-	-	57	-	PD10	I/O	FT	PD10		USART3_CK
G9	-	-	-	58	-	PD11	I/O	FT	PD11		USART3_CTS
K10	-	-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1 / USART3_RTS
J10	-	-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2
H10	-	-	-	61	-	PD14	I/O	FT	PD14		TIM4_CH3
G10	-	-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4
F10	-	F6	37	63	-	PC6	I/O	FT	PC6		TIM3_CH1
E10		E7	38	64	-	PC7	I/O	FT	PC7		TIM3_CH2
F9		E8	39	65	-	PC8	I/O	FT	PC8		TIM3_CH3
E9	-	D8	40	66	-	PC9	I/O	FT	PC9		TIM3_CH4
D9	29	D7	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(7)/MCO	
C9	30	C7	42	68	21	PA9	I/O	FT	PA9	USART1_TX(7)/ TIM1_CH2(7)	
D10	31	C6	43	69	22	PA10	I/O	FT	PA10	USART1_RX(7)/ TIM1_CH3(7)	
C10	32	C8	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ CANRX(7)/ USBDM TIM1_CH4(7)	
B10	33	B8	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/ CANTX(7) //USBDP TIM1_ETR(7)	

Figure 10. Pin loading conditions

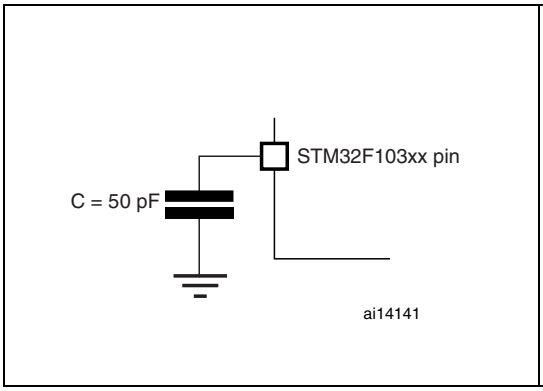
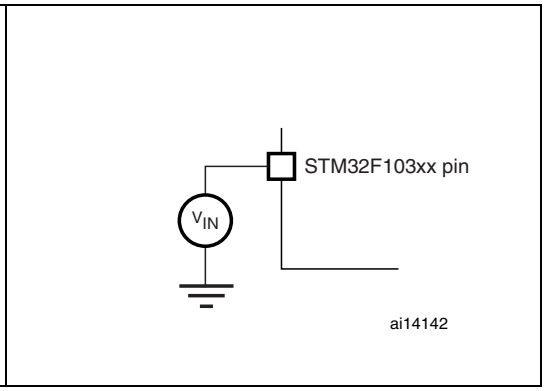
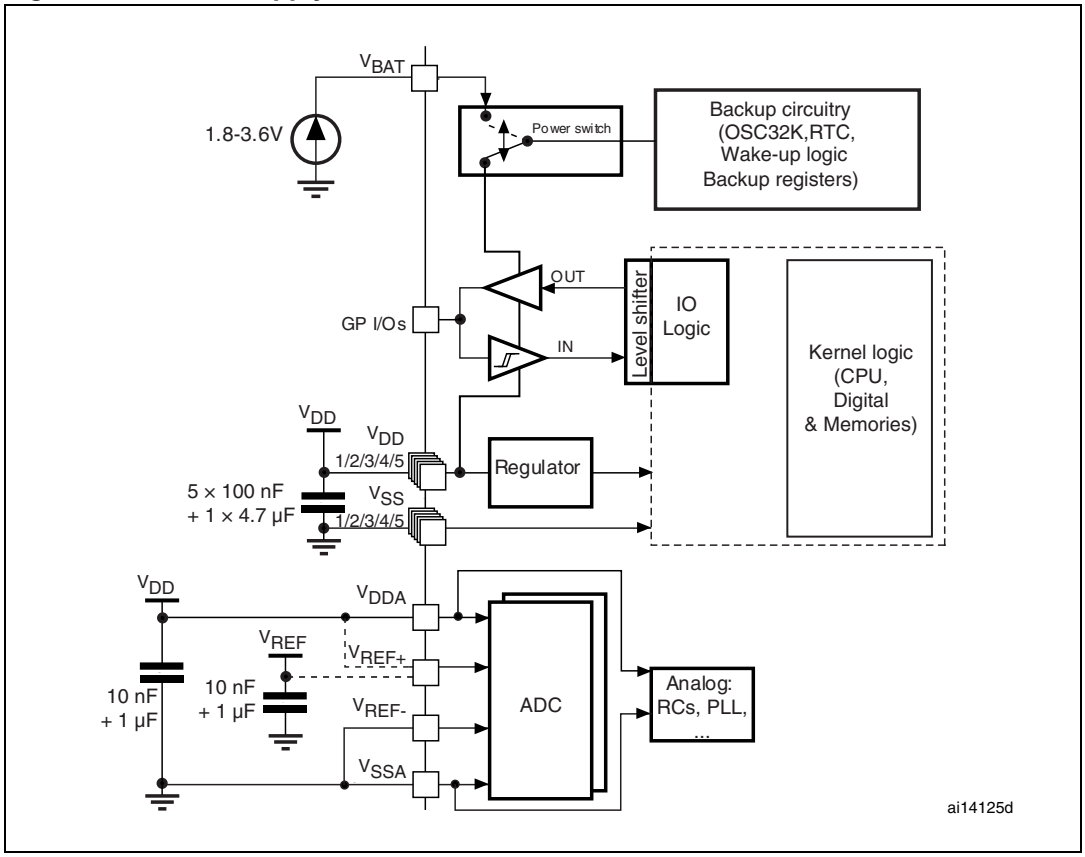


Figure 11. Pin input voltage



5.1.6 Power supply scheme

Figure 12. Power supply scheme



Caution: In *Figure 12*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 9. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LFBGA100		454	mW
		LQFP100		434	
		TFBGA64		308	
		LQFP64		444	
		LQFP48		363	
		VFQFPN36		1110	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 45: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 81*).
4. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 81*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	µs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Figure 17. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at V_{DD} = 3.3 V and 3.6 V

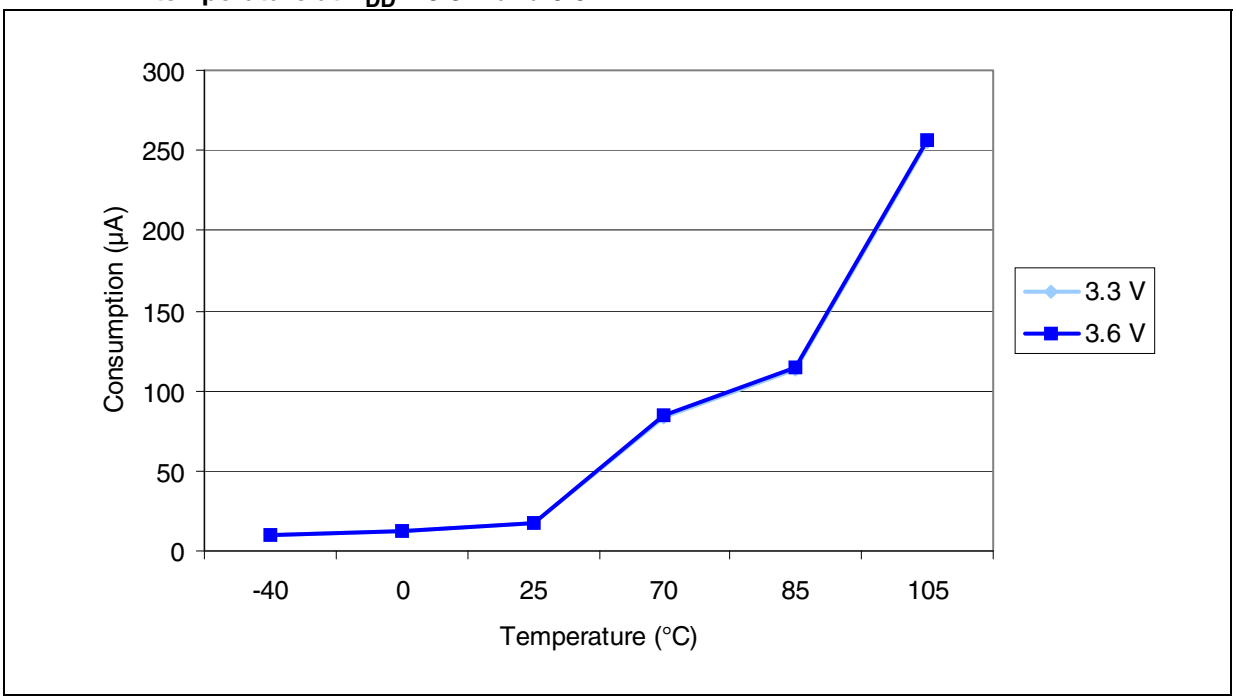


Figure 18. Typical current consumption in Standby mode versus temperature at V_{DD} = 3.3 V and 3.6 V

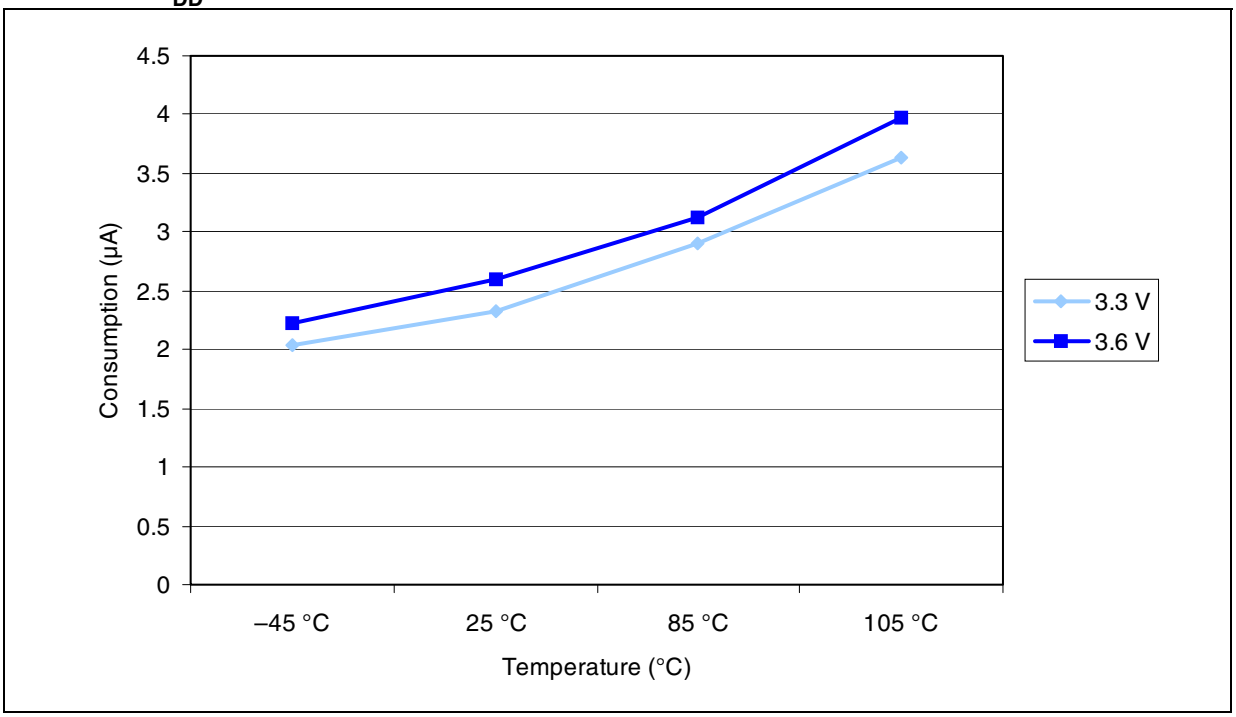


Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	14.4	5.5	mA
			48 MHz	9.9	3.9	
			36 MHz	7.6	3.1	
			24 MHz	5.3	2.3	
			16 MHz	3.8	1.8	
			8 MHz	2.1	1.2	
			4 MHz	1.6	1.1	
			2 MHz	1.3	1	
			1 MHz	1.11	0.98	
			500 kHz	1.04	0.96	
			125 kHz	0.98	0.95	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	12.3	4.4	
			48 MHz	9.3	3.3	
			36 MHz	7	2.5	
			24 MHz	4.8	1.8	
			16 MHz	3.2	1.2	
			8 MHz	1.6	0.6	
			4 MHz	1	0.5	
			2 MHz	0.72	0.47	
			1 MHz	0.56	0.44	
			500 kHz	0.49	0.42	
			125 kHz	0.43	0.41	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C	–2	±1	2.5	%
		T_A = –10 to 85 °C	–1.5	±1	2.2	%
		T_A = 0 to 70 °C	–1.3	±1	2	%
		T_A = 25 °C	–1.1	±1	1.8	%
$t_{su(HSI)}$	HSI oscillator startup time		1		2	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	µA

1. Guaranteed by design, not tested in production.
2. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption		0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	Wakeup on HSI RC clock	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 µs	3.6	µs
	Wakeup from Stop mode (regulator in low power mode)	HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs	50	µs

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 27. PLL characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)		1	8.0	25	MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock		16		72	MHz
t_{LOCK}	PLL lock time				200	µs

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 28. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20		40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20		40	ms

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

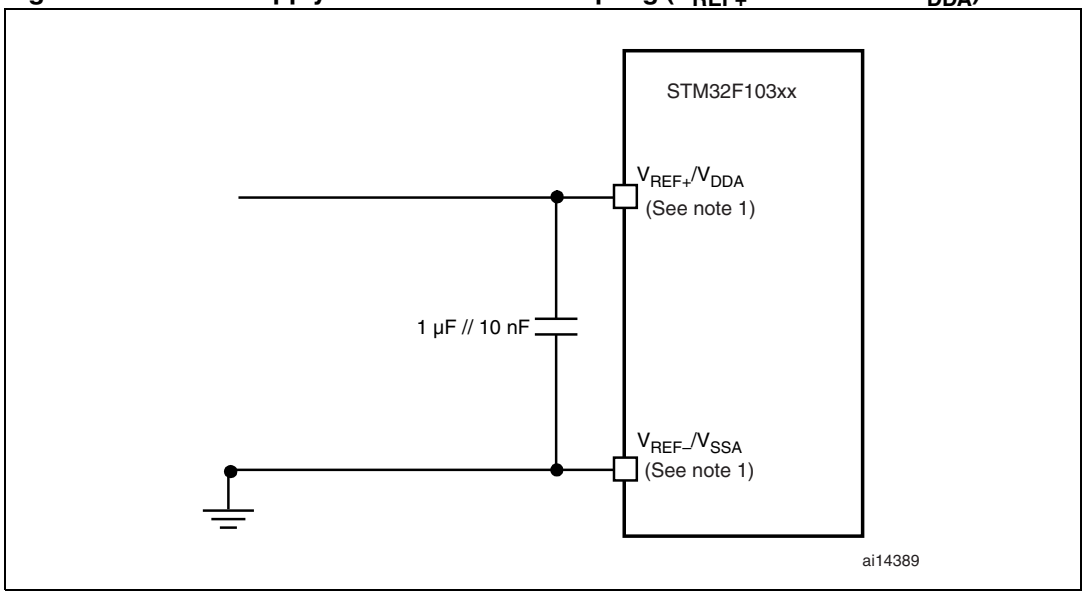
Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 t_{PCLK}		
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	73		
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (2)	Data input setup time Master mode	SPI1	1		
		SPI2	5		
$t_{su(SI)}$(2)	Data input setup time Slave mode		1		
$t_{h(MI)}$ (2)	Data input hold time Master mode	SPI1	1		
		SPI2	5		
$t_{h(SI)}$(2)	Data input hold time Slave mode		3		
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 24 MHz	0	4 t_{PCLK}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$(2)		Master mode (after enable edge)	4		

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 33. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{25}[1]	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}[2]	Startup time	4		10	µs
T_{S_temp}[3][2]	ADC sampling time when reading the temperature			17.1	µs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 35*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 56. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LFBGA100 - 10 × 10 mm / 0.8 mm pitch	44	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient TFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient VFQFPN 36 - 6 × 6 mm / 0.5 mm pitch	18	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 58. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	STM32F103CBT6, STM32F103T6 and STM32F103T8 root part numbers added (see *Table 2: STM32F103xx medium-density device features and peripheral counts*) VFQFPN36 package added (see *Section 6: Package characteristics*). All packages are ECOPACK® compliant. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). *Table 5: Medium-density STM32F103xx pin definitions* updated and clarified. *Table 26: Low-power mode wakeup timings* updated. T_A min corrected in *Table 12: Embedded internal reference voltage*. *Note 2* added below *Table 22: HSE 4-16 MHz oscillator characteristics*. $V_{ESD(CDM)}$ value added to *Table 32: ESD absolute maximum ratings*. *Note 3* added and V_{OH} parameter description modified in *Table 35: Output voltage characteristics*. *Note 1* modified under *Table 36: I/O AC characteristics*. *Equation 1* and *Table 46: R_{AIN} max for f_{ADC} = 14 MHz* added to *Section 5.3.17: 12-bit ADC characteristics*. V_{AIN}, t_S max, t_{CONV}, V_{REF+} min and t_{lat} max modified, notes modified and t_{latr} added in *Table 45: ADC characteristics*. *Figure 30: ADC accuracy characteristics* updated. *Note 1* modified below *Figure 31: Typical connection diagram using the ADC*. *Electrostatic discharge (ESD) on page 55* modified. Number of TIM4 channels modified in *Figure 1: STM32F103xx performance line block diagram*. Maximum current consumption *Table 13*, *Table 14* and *Table 15* updated. V_{hys}modified in *Table 34: I/O static characteristics*. *Table 48: ADC accuracy* updated. t_{VDD} modified in *Table 10: Operating conditions at power-up / power-down*. V_{FESD} value added in *Table 30: EMS characteristics*. Values corrected, note 2 modified and note 3 removed in *Table 26: Low-power mode wakeup timings*. *Table 16: Typical and maximum current consumptions in Stop and Standby modes*: Typical values added for V_{DD}/V_{BAT} = 2.4 V, *Note 2* modified, *Note 2* added. *Table 21: Typical current consumption in Standby mode* added. *On-chip peripheral current consumption on page 46* added. ACC_{HSI} values updated in *Table 24: HSI oscillator characteristics*. V_{prog} added to *Table 28: Flash memory characteristics*. Upper option byte address modified in *Figure 9: Memory map*. Typical f_{LSI} value added in *Table 25: LSI oscillator characteristics* and internal RC value corrected from 32 to 40 kHz in entire document. T_{S_temp} added to *Table 49: TS characteristics*. N_{END} modified in *Table 29: Flash memory endurance and data retention*. $T_{S\_vrefint}$ added to *Table 12: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 56*. All I/Os are CMOS and TTL compliant. *Figure 32: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})* modified. t_{JITTER} and f_{VCO} removed from *Table 27: PLL characteristics*. *Appendix A: Important notes on page 81* added. Added *Figure 14*, *Figure 15*, *Figure 16* and *Figure 18*.