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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103v8t6tr

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x8 and STM32F103xB medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F103x8 and STM32F103xB performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx medium-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx medium-density performance line family includes devices in six different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx medium-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 2. STM32F103xx medium-density device features and peripheral counts

Peripheral		STM32F103Tx	STM32F103Cx		STM32F103Rx		STM32F103Vx	
Flash - Kbytes		64	64	128	64	128	64	128
SRAM - Kbytes		20	20	20	20		20	
Timers	General-purpose	3	3	3	3		3	
	Advanced-control	1	1		1		1	
Communication	SPI	1	2	2	2		2	
	I^2C	1	2	2	2		2	
	USART	2	3	3	3		3	
	USB	1	1	1	1		1	
	CAN	1	1	1	1		1	
GPIOs		26	37		51		80	
12-bit synchronized ADC Number of channels		2 10 channels	2 10 channels		2 16 channels		2 16 channels	
CPU frequency		72 MHz						
Operating voltage		2.0 to 3.6 V						
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C (see *Table 9*) Junction temperature: –40 to + 125 °C (see *Table 9*)						
Packages		VFQFPN36	LQFP48		LQFP64, TFBGA64		LQFP100, LFBGA100	

can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

2.3.22 ADC (analog-to-digital converter)

Two 12-bit analog-to-digital converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

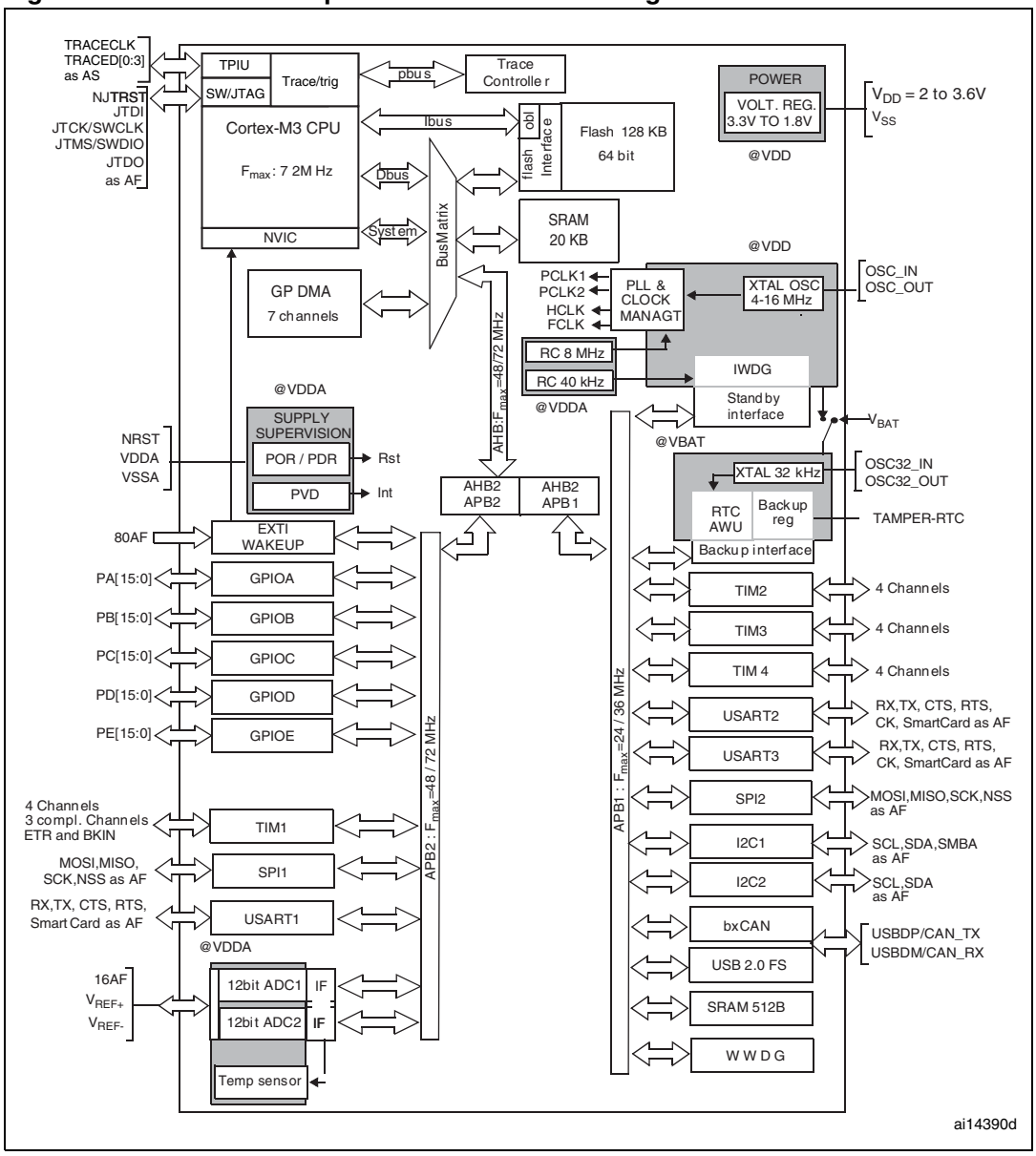
2.3.23 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 1. STM32F103xx performance line block diagram



1. T_A = –40 °C to +105 °C (junction temperature up to 125 °C).
2. AF = alternate function on I/O port pin.

Figure 5. STM32F103xx performance line LQFP64 pinout

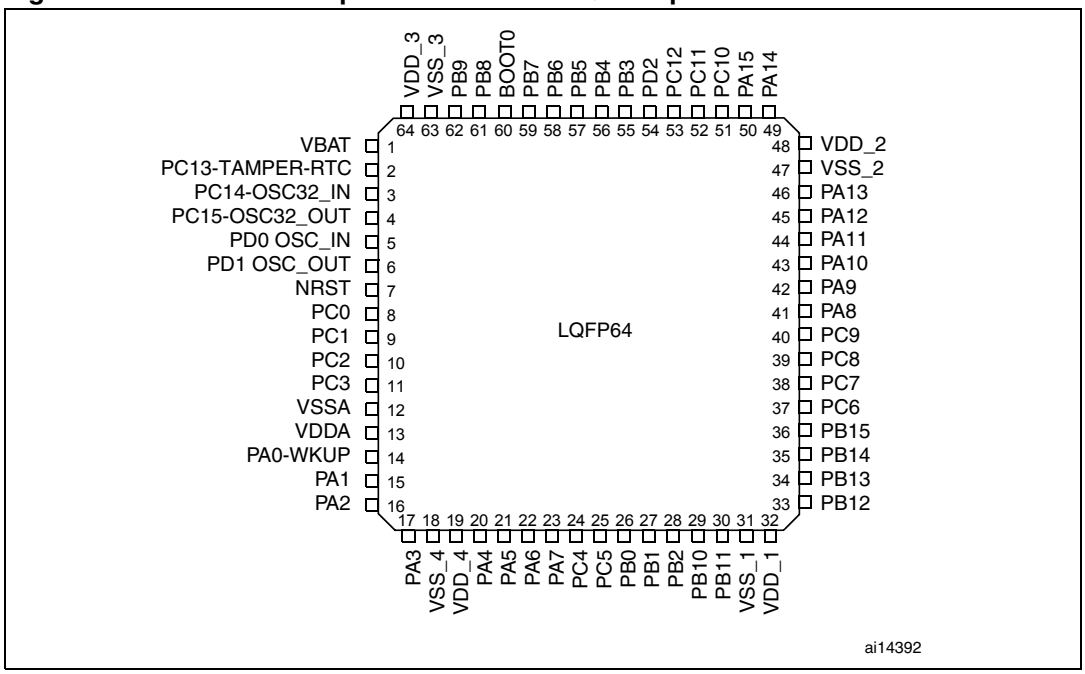


Figure 6. STM32F103xx performance line TFBGA64 ballout

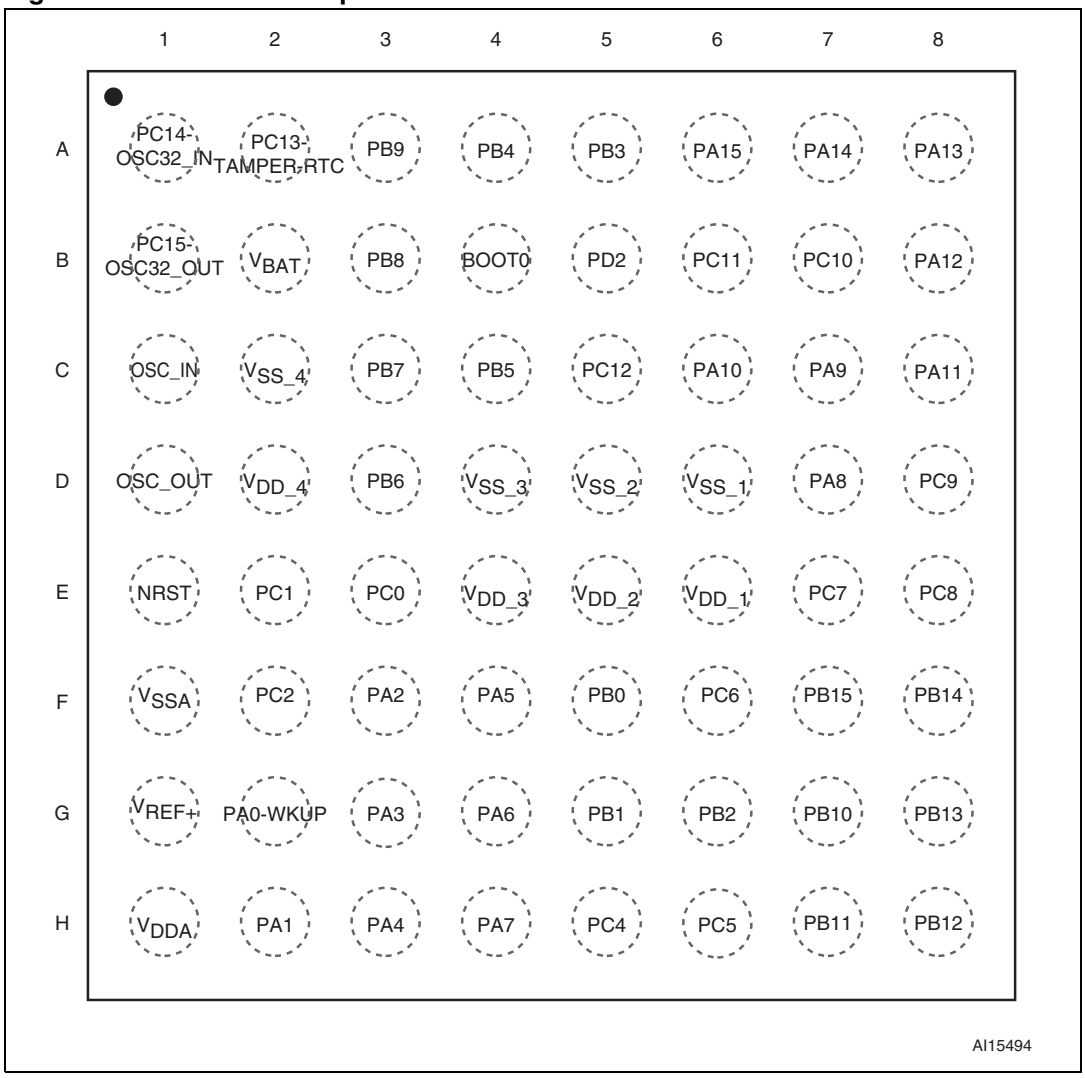


Table 5. Medium-density STM32F103xx pin definitions

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A3	-		-	1	-	PE2	I/O	FT	PE2	TRACECK	
B3	-		-	2	-	PE3	I/O	FT	PE3	TRACED0	
C3	-		-	3	-	PE4	I/O	FT	PE4	TRACED1	
D3	-		-	4	-	PE5	I/O	FT	PE5	TRACED2	
E3	-		-	5	-	PE6	I/O	FT	PE6	TRACED3	
B2	1	B2	1	6	-	V_{BAT}	S		V_{BAT}		
A2	2	A2	2	7	-	PC13-TAMPER-RTC(4)	I/O		PC13(5)	TAMPER-RTC	
A1	3	A1	3	8	-	PC14-OSC32_IN(4)	I/O		PC14(5)	OSC32_IN	
B1	4	B1	4	9	-	PC15-OSC32_OUT(4)	I/O		PC15(5)	OSC32_OUT	
C2	-	-	-	10	-	V_{SS_5}	S		V_{SS_5}		
D2	-	-	-	11	-	V_{DD_5}	S		V_{DD_5}		
C1	5	C1	5	12	2	OSC_IN	I		OSC_IN		
D1	6	D1	6	13	3	OSC_OUT	O		OSC_OUT		
E1	7	E1	7	14	4	NRST	I/O		NRST		
F1	-	E3	8	15	-	PC0	I/O		PC0	ADC12_IN10	
F2	-	E2	9	16	-	PC1	I/O		PC1	ADC12_IN11	
E2	-	F2	10	17	-	PC2	I/O		PC2	ADC12_IN12	
F3	-	-(6)	11	18	-	PC3	I/O		PC3	ADC12_IN13	
G1	8	F1	12	19	5	V_{SSA}	S		V_{SSA}		
H1	-	-	-	20	-	V_{REF-}	S		V_{REF-}		
J1	-	G1(6)	-	21	-	V_{REF+}	S		V_{REF+}		
K1	9	H1	13	22	6	V_{DDA}	S		V_{DDA}		
G2	10	G2	14	23	7	PA0-WKUP	I/O		PA0	WKUP/ USART2_CTS(7)/ ADC12_IN0/ TIM2_CH1_ETR(7)	
H2	11	H2	15	24	8	PA1	I/O		PA1	USART2_RTS(7)/ ADC12_IN1/ TIM2_CH2(7)	
J2	12	F3	16	25	9	PA2	I/O		PA2	USART2_TX(7)/ ADC12_IN2/ TIM2_CH3(7)	

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
F7	24	E6	32	50	19	V_{DD_1}	S		V_{DD_1}		
K8	25	H8	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK(7)/ TIM1_BKIN(7)	
J8	26	G8	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(7)/ TIM1_CH1N (7)	
H8	27	F8	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(7) TIM1_CH2N (7)	
G8	28	F7	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(7)	
K9	-	-	-	55	-	PD8	I/O	FT	PD8		USART3_TX
J9	-	-	-	56	-	PD9	I/O	FT	PD9		USART3_RX
H9	-	-	-	57	-	PD10	I/O	FT	PD10		USART3_CK
G9	-	-	-	58	-	PD11	I/O	FT	PD11		USART3_CTS
K10	-	-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1 / USART3_RTS
J10	-	-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2
H10	-	-	-	61	-	PD14	I/O	FT	PD14		TIM4_CH3
G10	-	-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4
F10	-	F6	37	63	-	PC6	I/O	FT	PC6		TIM3_CH1
E10		E7	38	64	-	PC7	I/O	FT	PC7		TIM3_CH2
F9		E8	39	65	-	PC8	I/O	FT	PC8		TIM3_CH3
E9	-	D8	40	66	-	PC9	I/O	FT	PC9		TIM3_CH4
D9	29	D7	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(7)/MCO	
C9	30	C7	42	68	21	PA9	I/O	FT	PA9	USART1_TX(7)/ TIM1_CH2(7)	
D10	31	C6	43	69	22	PA10	I/O	FT	PA10	USART1_RX(7)/ TIM1_CH3(7)	
C10	32	C8	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ CANRX(7)/ USBDM TIM1_CH4(7)	
B10	33	B8	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/ CANTX(7) //USBDP TIM1_ETR(7)	

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 32. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

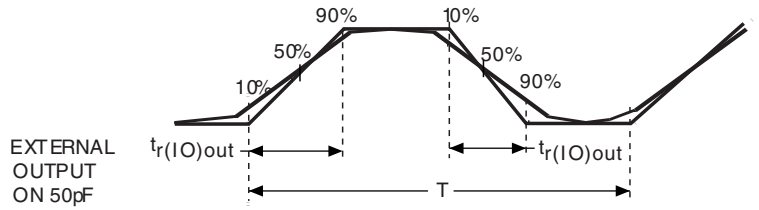
- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 33. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

Figure 23. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 34*).

Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 37. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

5.3.15 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The STM32F103xx performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

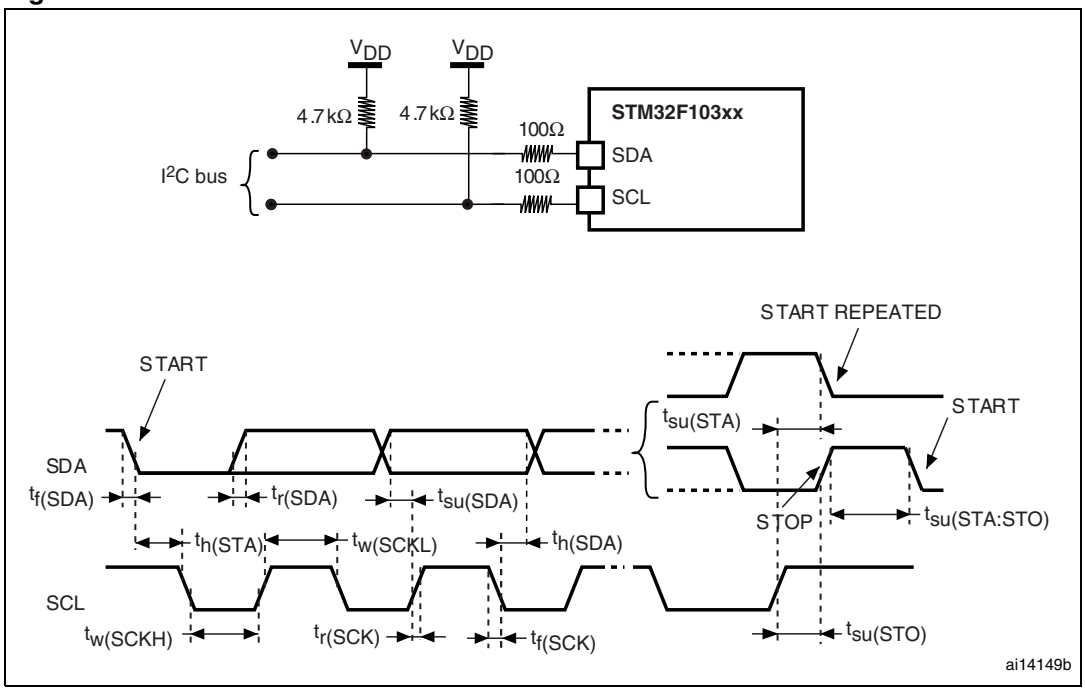
The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 39. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 25. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Table 43. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP, USBDM)	0.2		V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)		0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers

Figure 29. USB timings: definition of data signal rise and fall time

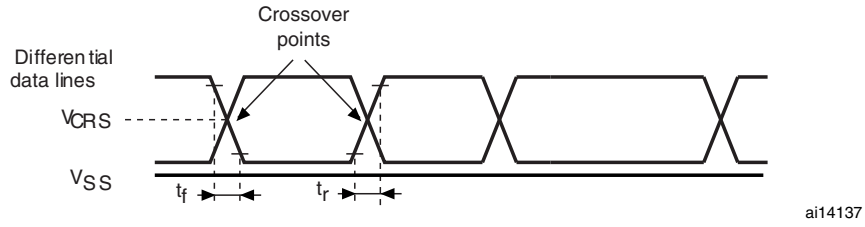


Table 44. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics					
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

5.3.16 CAN (controller area network) interface

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

Table 48. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

Figure 30. ADC accuracy characteristics

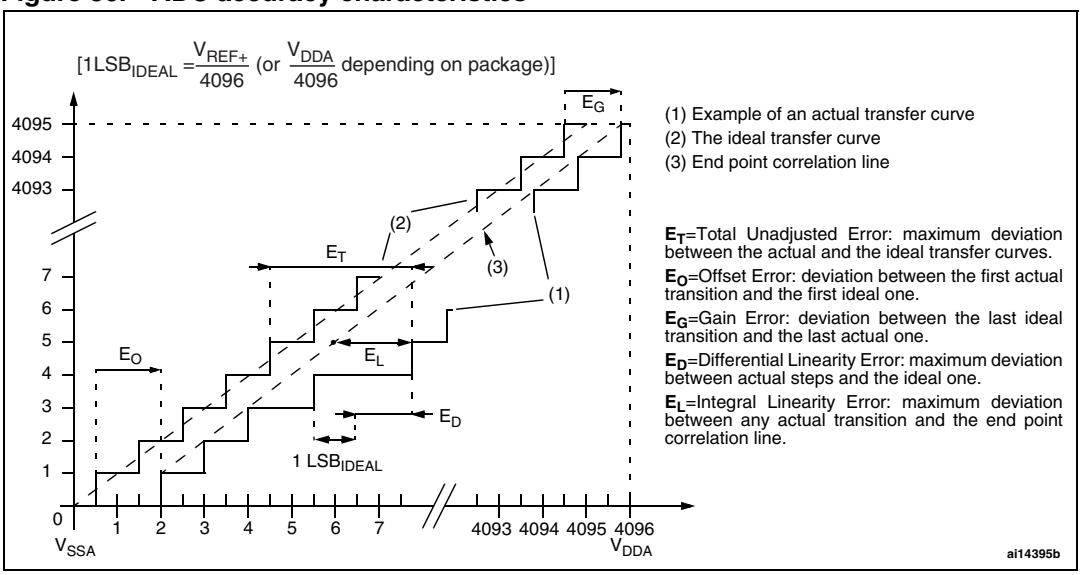


Figure 38. LQFP100, 100-pin low-profile quad flat package outline(1)

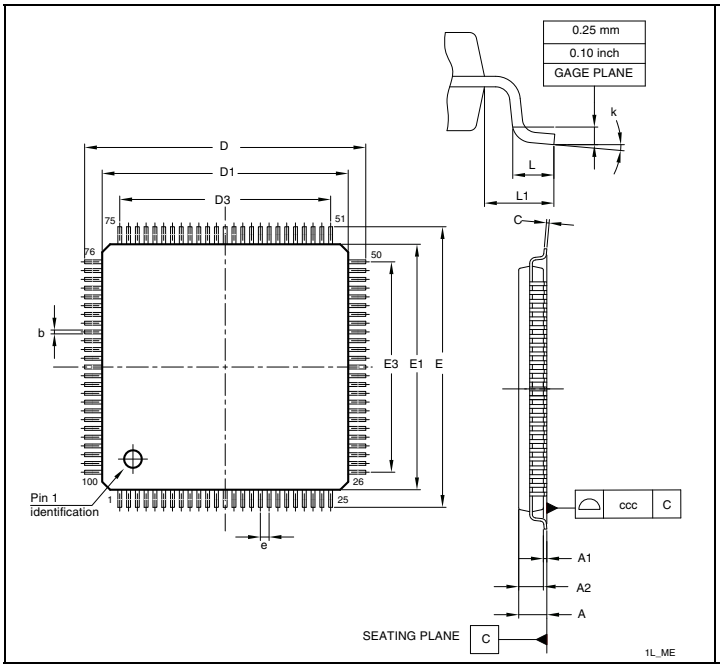
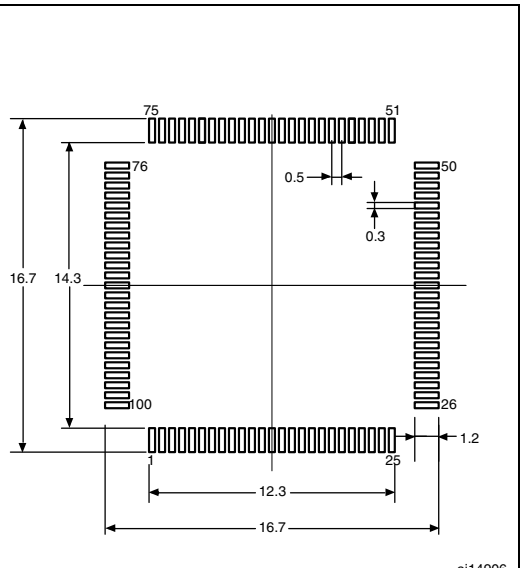


Figure 39. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 52. LQPF100, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	16	15.8	16.2	0.6299	0.622	0.6378
D1	14	13.8	14.2	0.5512	0.5433	0.5591
D3	12			0.4724		
E	16	15.8	16.2	0.6299	0.622	0.6378
E1	14	13.8	14.2	0.5512	0.5433	0.5591
E3	12			0.4724		
e	0.5			0.0197		
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
k	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 58. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	STM32F103CBT6, STM32F103T6 and STM32F103T8 root part numbers added (see *Table 2: STM32F103xx medium-density device features and peripheral counts*) VFQFPN36 package added (see *Section 6: Package characteristics*). All packages are ECOPACK® compliant. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). *Table 5: Medium-density STM32F103xx pin definitions* updated and clarified. *Table 26: Low-power mode wakeup timings* updated. T_A min corrected in *Table 12: Embedded internal reference voltage*. *Note 2* added below *Table 22: HSE 4-16 MHz oscillator characteristics*. $V_{ESD(CDM)}$ value added to *Table 32: ESD absolute maximum ratings*. *Note 3* added and V_{OH} parameter description modified in *Table 35: Output voltage characteristics*. *Note 1* modified under *Table 36: I/O AC characteristics*. *Equation 1* and *Table 46: R_{AIN} max for f_{ADC} = 14 MHz* added to *Section 5.3.17: 12-bit ADC characteristics*. V_{AIN}, t_S max, t_{CONV}, V_{REF+} min and t_{lat} max modified, notes modified and t_{latr} added in *Table 45: ADC characteristics*. *Figure 30: ADC accuracy characteristics* updated. *Note 1* modified below *Figure 31: Typical connection diagram using the ADC*. *Electrostatic discharge (ESD) on page 55* modified. Number of TIM4 channels modified in *Figure 1: STM32F103xx performance line block diagram*. Maximum current consumption *Table 13*, *Table 14* and *Table 15* updated. V_{hys}modified in *Table 34: I/O static characteristics*. *Table 48: ADC accuracy* updated. t_{VDD} modified in *Table 10: Operating conditions at power-up / power-down*. V_{FESD} value added in *Table 30: EMS characteristics*. Values corrected, note 2 modified and note 3 removed in *Table 26: Low-power mode wakeup timings*. *Table 16: Typical and maximum current consumptions in Stop and Standby modes*: Typical values added for V_{DD}/V_{BAT} = 2.4 V, *Note 2* modified, *Note 2* added. *Table 21: Typical current consumption in Standby mode* added. *On-chip peripheral current consumption on page 46* added. ACC_{HSI} values updated in *Table 24: HSI oscillator characteristics*. V_{prog} added to *Table 28: Flash memory characteristics*. Upper option byte address modified in *Figure 9: Memory map*. Typical f_{LSI} value added in *Table 25: LSI oscillator characteristics* and internal RC value corrected from 32 to 40 kHz in entire document. T_{S_temp} added to *Table 49: TS characteristics*. N_{END} modified in *Table 29: Flash memory endurance and data retention*. $T_{S\_vrefint}$ added to *Table 12: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 56*. All I/Os are CMOS and TTL compliant. *Figure 32: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})* modified. t_{JITTER} and f_{VCO} removed from *Table 27: PLL characteristics*. *Appendix A: Important notes on page 81* added. Added *Figure 14*, *Figure 15*, *Figure 16* and *Figure 18*.