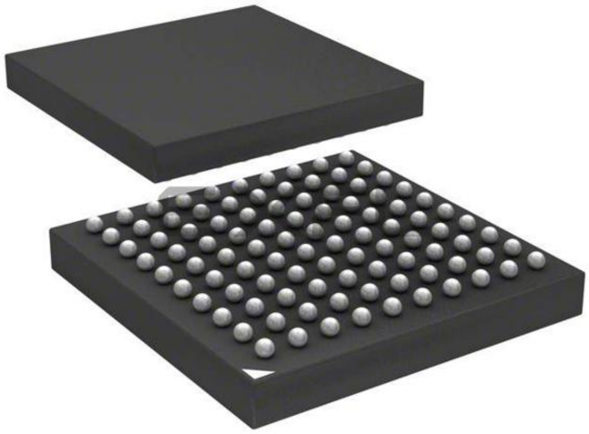
STMicroelectronics - STM32F103VBH7 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vbh7

can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to three synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

Figure 4. STM32F103xx performance line LQFP100 pinout

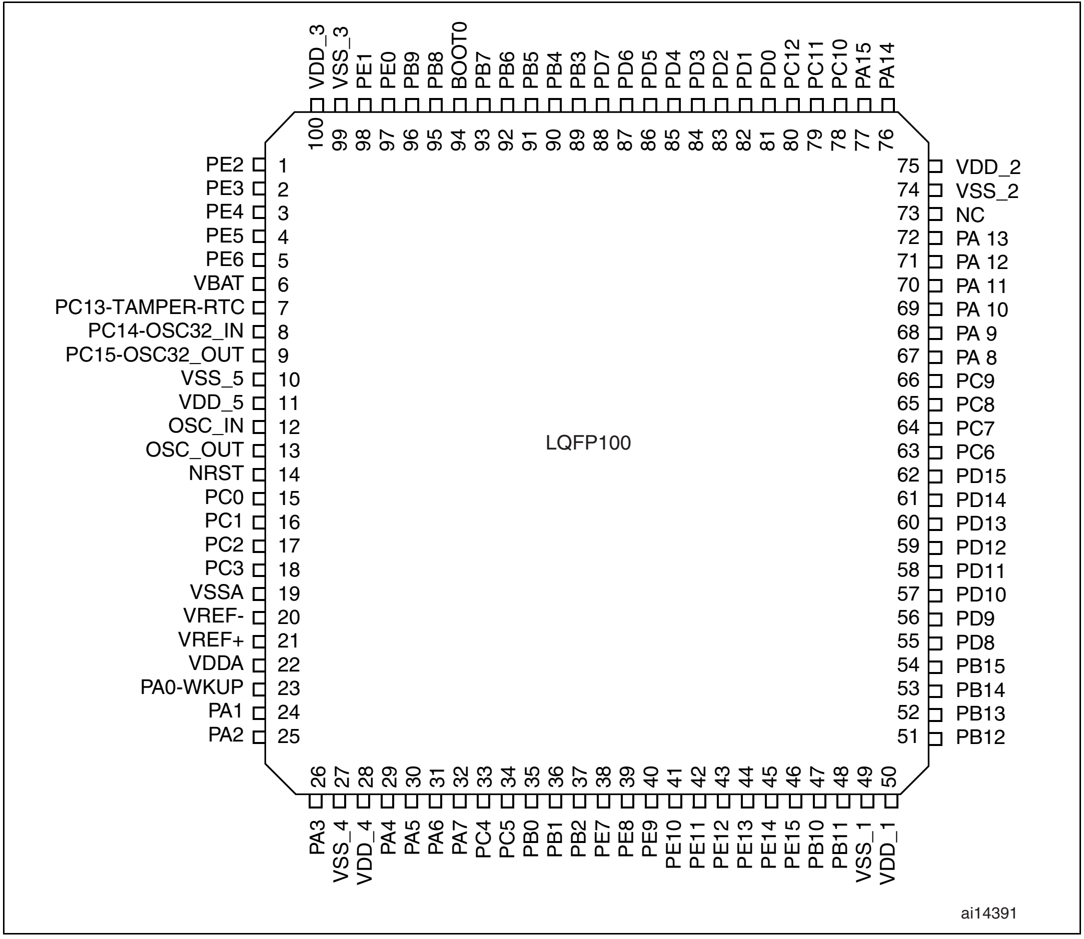


Table 5. Medium-density STM32F103xx pin definitions

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A3	-		-	1	-	PE2	I/O	FT	PE2	TRACECK	
B3	-		-	2	-	PE3	I/O	FT	PE3	TRACED0	
C3	-		-	3	-	PE4	I/O	FT	PE4	TRACED1	
D3	-		-	4	-	PE5	I/O	FT	PE5	TRACED2	
E3	-		-	5	-	PE6	I/O	FT	PE6	TRACED3	
B2	1	B2	1	6	-	V_{BAT}	S		V_{BAT}		
A2	2	A2	2	7	-	PC13-TAMPER-RTC(4)	I/O		PC13(5)	TAMPER-RTC	
A1	3	A1	3	8	-	PC14-OSC32_IN(4)	I/O		PC14(5)	OSC32_IN	
B1	4	B1	4	9	-	PC15-OSC32_OUT(4)	I/O		PC15(5)	OSC32_OUT	
C2	-	-	-	10	-	V_{SS_5}	S		V_{SS_5}		
D2	-	-	-	11	-	V_{DD_5}	S		V_{DD_5}		
C1	5	C1	5	12	2	OSC_IN	I		OSC_IN		
D1	6	D1	6	13	3	OSC_OUT	O		OSC_OUT		
E1	7	E1	7	14	4	NRST	I/O		NRST		
F1	-	E3	8	15	-	PC0	I/O		PC0	ADC12_IN10	
F2	-	E2	9	16	-	PC1	I/O		PC1	ADC12_IN11	
E2	-	F2	10	17	-	PC2	I/O		PC2	ADC12_IN12	
F3	-	-(6)	11	18	-	PC3	I/O		PC3	ADC12_IN13	
G1	8	F1	12	19	5	V_{SSA}	S		V_{SSA}		
H1	-	-	-	20	-	V_{REF-}	S		V_{REF-}		
J1	-	G1(6)	-	21	-	V_{REF+}	S		V_{REF+}		
K1	9	H1	13	22	6	V_{DDA}	S		V_{DDA}		
G2	10	G2	14	23	7	PA0-WKUP	I/O		PA0	WKUP/ USART2_CTS(7)/ ADC12_IN0/ TIM2_CH1_ETR(7)	
H2	11	H2	15	24	8	PA1	I/O		PA1	USART2_RTS(7)/ ADC12_IN1/ TIM2_CH2(7)	
J2	12	F3	16	25	9	PA2	I/O		PA2	USART2_TX(7)/ ADC12_IN2/ TIM2_CH3(7)	

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
K2	13	G3	17	26	10	PA3	I/O		PA3	USART2_RX(7)/ ADC12_IN3/ TIM2_CH4(7)	
E4	-	C2	18	27	-	V_{SS_4}	S		V_{SS_4}		
F4	-	D2	19	28	-	V_{DD_4}	S		V_{DD_4}		
G3	14	H3	20	29	11	PA4	I/O		PA4	SPI1_NSS(7)/ USART2_CK(7)/ ADC12_IN4	
H3	15	F4	21	30	12	PA5	I/O		PA5	SPI1_SCK(7)/ ADC12_IN5	
J3	16	G4	22	31	13	PA6	I/O		PA6	SPI1_MISO(7)/ ADC12_IN6/ TIM3_CH1(7)	TIM1_BKIN
K3	17	H4	23	32	14	PA7	I/O		PA7	SPI1_MOSI(7)/ ADC12_IN7/ TIM3_CH2(7)	TIM1_CH1N
G4	-	H5	24	33		PC4	I/O		PC4	ADC12_IN14	
H4	-	H6	25	34		PC5	I/O		PC5	ADC12_IN15	
J4	18	F5	26	35	15	PB0	I/O		PB0	ADC12_IN8/ TIM3_CH3(7)	TIM1_CH2N
K4	19	G5	27	36	16	PB1	I/O		PB1	ADC12_IN9/ TIM3_CH4(7)	TIM1_CH3N
G5	20	G6	28	37	17	PB2	I/O	FT	PB2/BOOT1		
H5	-	-	-	38	-	PE7	I/O	FT	PE7		TIM1_ETR
J5	-	-	-	39	-	PE8	I/O	FT	PE8		TIM1_CH1N
K5	-	-	-	40	-	PE9	I/O	FT	PE9		TIM1_CH1
G6	-	-	-	41	-	PE10	I/O	FT	PE10		TIM1_CH2N
H6	-	-	-	42	-	PE11	I/O	FT	PE11		TIM1_CH2
J6	-	-	-	43	-	PE12	I/O	FT	PE12		TIM1_CH3N
K6	-	-	-	44	-	PE13	I/O	FT	PE13		TIM1_CH3
G7	-	-	-	45	-	PE14	I/O	FT	PE14		TIM1_CH4
H7	-	-	-	46	-	PE15	I/O	FT	PE15		TIM1_BKIN
J7	21	G7	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(7)	TIM2_CH3
K7	22	H7	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(7)	TIM2_CH4
E7	23	D6	31	49	18	V_{SS_1}	S		V_{SS_1}		

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
F7	24	E6	32	50	19	V_{DD_1}	S		V_{DD_1}		
K8	25	H8	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK(7)/ TIM1_BKIN(7)	
J8	26	G8	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS(7)/ TIM1_CH1N (7)	
H8	27	F8	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS(7) TIM1_CH2N (7)	
G8	28	F7	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI/ TIM1_CH3N(7)	
K9	-	-	-	55	-	PD8	I/O	FT	PD8		USART3_TX
J9	-	-	-	56	-	PD9	I/O	FT	PD9		USART3_RX
H9	-	-	-	57	-	PD10	I/O	FT	PD10		USART3_CK
G9	-	-	-	58	-	PD11	I/O	FT	PD11		USART3_CTS
K10	-	-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1 / USART3_RTS
J10	-	-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2
H10	-	-	-	61	-	PD14	I/O	FT	PD14		TIM4_CH3
G10	-	-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4
F10	-	F6	37	63	-	PC6	I/O	FT	PC6		TIM3_CH1
E10		E7	38	64	-	PC7	I/O	FT	PC7		TIM3_CH2
F9		E8	39	65	-	PC8	I/O	FT	PC8		TIM3_CH3
E9	-	D8	40	66	-	PC9	I/O	FT	PC9		TIM3_CH4
D9	29	D7	41	67	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1(7)/MCO	
C9	30	C7	42	68	21	PA9	I/O	FT	PA9	USART1_TX(7)/ TIM1_CH2(7)	
D10	31	C6	43	69	22	PA10	I/O	FT	PA10	USART1_RX(7)/ TIM1_CH3(7)	
C10	32	C8	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/ CANRX(7)/ USBDM TIM1_CH4(7)	

B10	33	B8	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/
										CANTX(7) //USBDP
										TIM1_ETR(7)	

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the $2\ V \leq V_{DD} \leq 3.6\ V$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

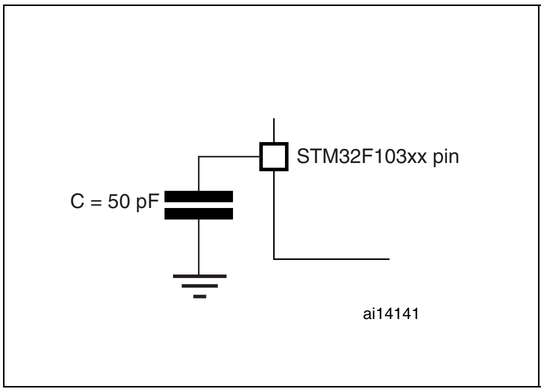
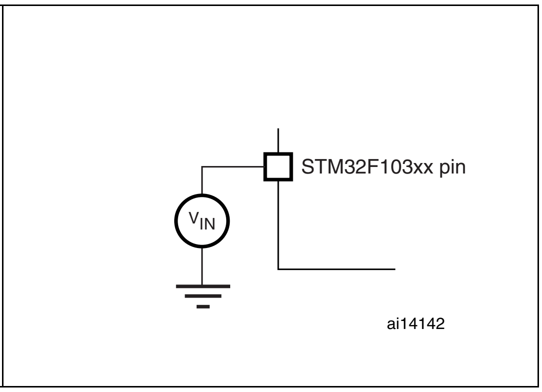
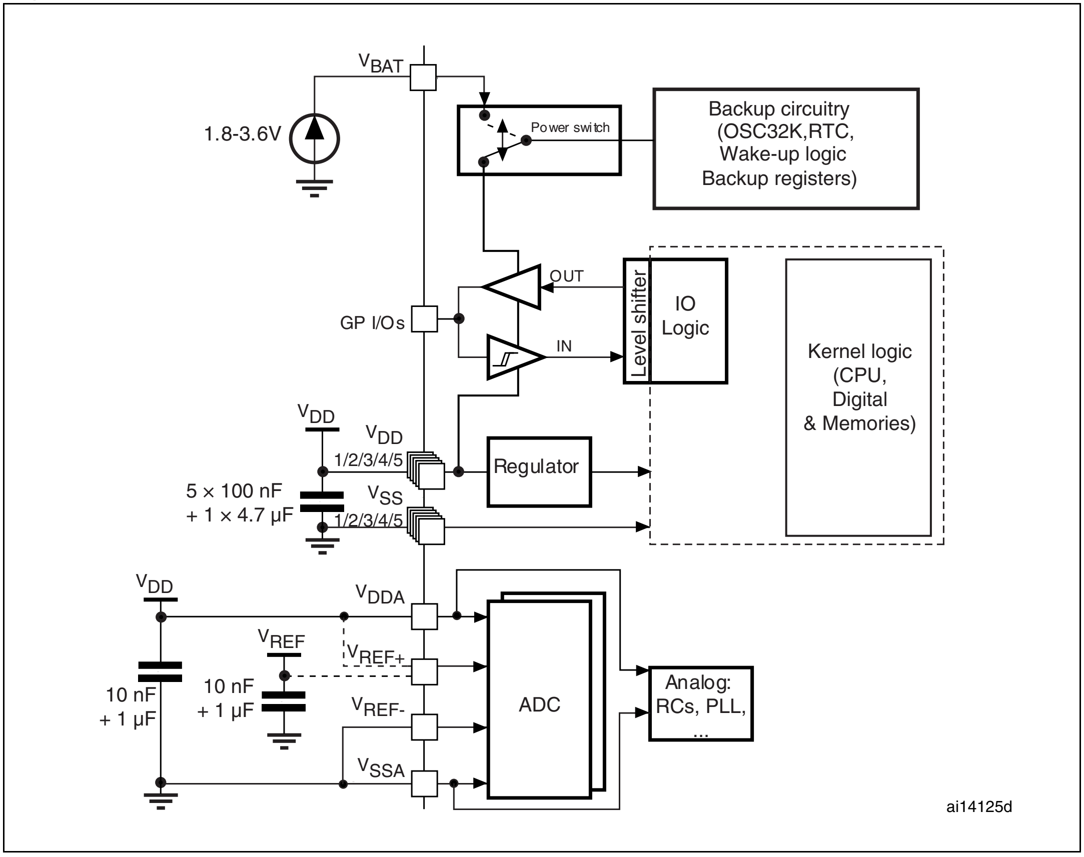


Figure 11. Pin input voltage



5.1.6 Power supply scheme

Figure 12. Power supply scheme



Caution: In *Figure 12*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	– 25	
$I_{INJ(PIN)}$ (2)(3)	Injected current on NRST pin	± 5	
	Injected current on HSE OSC_IN and LSE OSC_IN pins	± 5	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.

3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.

4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	36	
f_{PCLK2}	Internal APB2 clock frequency		0	72	
V_{DD}	Standard operating voltage		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.8	3.6	V

5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage			5.1	17.1(2)	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max[1]		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock[2], all peripherals enabled	72 MHz	30	32	mA
			48 MHz	20	20.5	
			36 MHz	15.5	16	
			24 MHz	11.5	12	
			16 MHz	8.5	9	
			8 MHz	5.5	6	
		External clock[2], all peripherals disabled	72 MHz	7.5	8	
			48 MHz	6	6.5	
			36 MHz	5	5.5	
			24 MHz	4.5	5	
			16 MHz	4	4.5	
			8 MHz	3	4	

1. based on characterization, tested in production at $V_{DD\ max}$, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

1. Guaranteed by design, not tested in production.

Figure 19. High-speed external clock source AC timing diagram

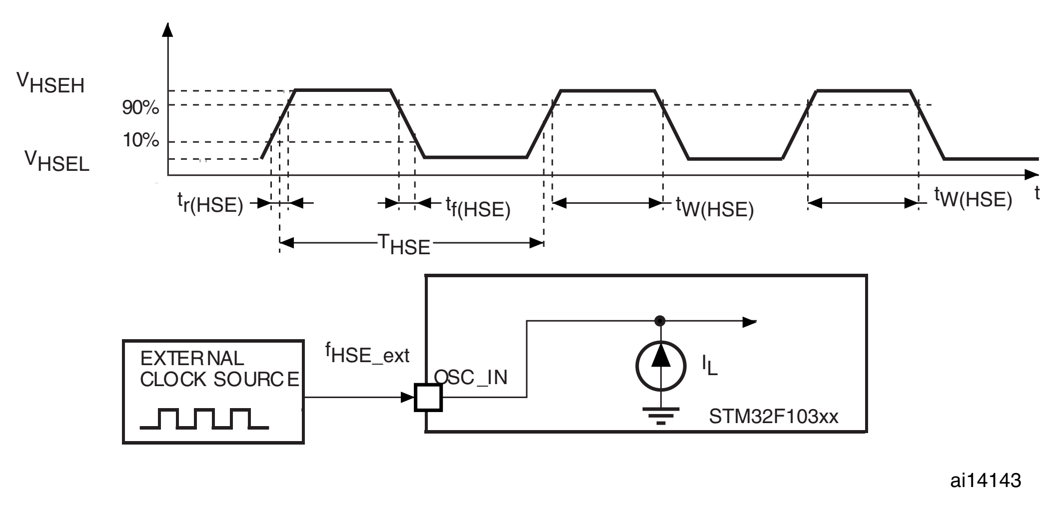
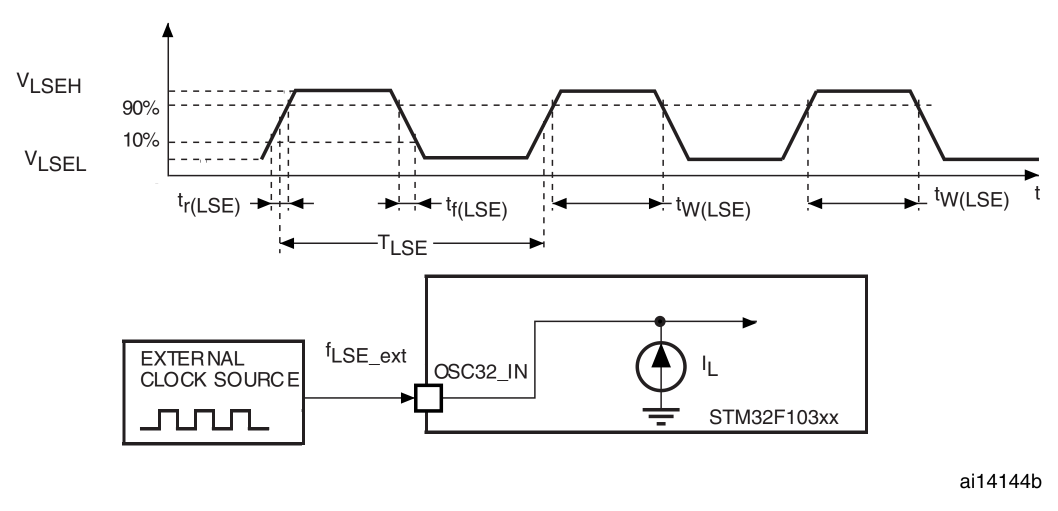


Figure 20. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: *For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.*
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

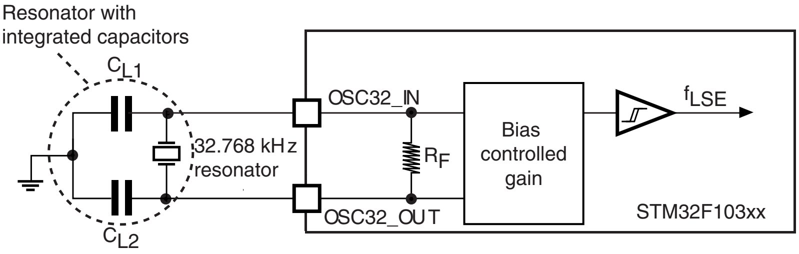
Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of $C_L = 6$ pF, and $C_{stray} = 2$ pF, then $C_{L1} = C_{L2} = 8$ pF.

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			5		MΩ
C_{L1} C_{L2}(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ			15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, $V_{IN} = V_{SS}$			1.4	µA
g_m	Oscillator Transconductance		5			µA/V
$t_{SU(LSE)}$(4)	startup time	V_{DD} is stabilized		3		s

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs above the table.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 22. Typical application with a 32.768 kHz crystal



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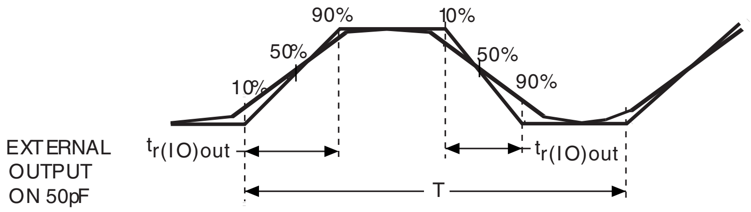
5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Figure 23. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 34*).

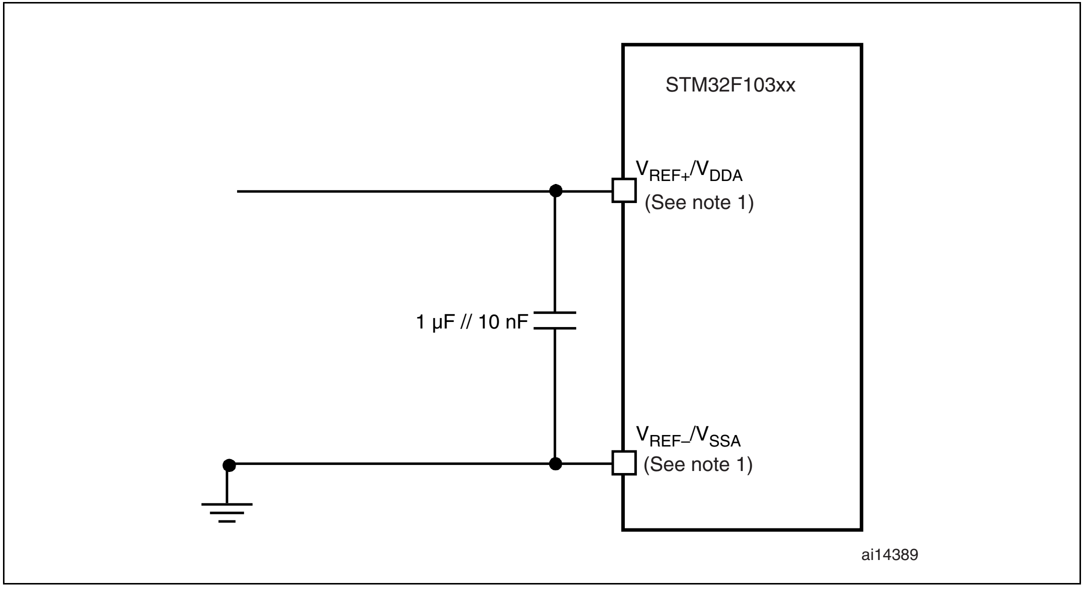
Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 37. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 33. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4		10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature			17.1	µs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 57: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$

$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

$P_{Dmax} = 175 + 272 = 447\text{ mW}$

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 56* T_{Jmax} is calculated as follows:

- For LQFP100, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 57: Ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$

$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

$P_{Dmax} = 70 + 64 = 134\text{ mW}$

Thus: P_{Dmax} = 134 mW

7 Ordering information scheme

Table 57. Ordering information scheme

Example: STM32 F 103 C 8 T 7 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

103 = performance line

Pin count

T = 36 pins
C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size(1)

8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory

Package

H = BGA
T = LQFP
U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and real

1. Although STM32F103x6 devices are not described in this datasheet, orderable part numbers that do not show the A internal code after temperature range code 6 or 7 should be referred to this datasheet for the electrical characteristics. The low-density datasheet only covers STM32F103x6 devices that feature the A code.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 58. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	STM32F103CBT6, STM32F103T6 and STM32F103T8 root part numbers added (see *Table 2: STM32F103xx medium-density device features and peripheral counts*) VFQFPN36 package added (see *Section 6: Package characteristics*). All packages are ECOPACK® compliant. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). *Table 5: Medium-density STM32F103xx pin definitions* updated and clarified. *Table 26: Low-power mode wakeup timings* updated. T_A min corrected in *Table 12: Embedded internal reference voltage*. *Note 2* added below *Table 22: HSE 4-16 MHz oscillator characteristics*. $V_{ESD(CDM)}$ value added to *Table 32: ESD absolute maximum ratings*. *Note 3* added and V_{OH} parameter description modified in *Table 35: Output voltage characteristics*. *Note 1* modified under *Table 36: I/O AC characteristics*. *Equation 1* and *Table 46: R_{AIN} max for f_{ADC} = 14 MHz* added to *Section 5.3.17: 12-bit ADC characteristics*. V_{AIN}, t_S max, t_{CONV}, V_{REF+} min and t_{lat} max modified, notes modified and t_{latr} added in *Table 45: ADC characteristics*. *Figure 30: ADC accuracy characteristics* updated. *Note 1* modified below *Figure 31: Typical connection diagram using the ADC*. *Electrostatic discharge (ESD) on page 55* modified. Number of TIM4 channels modified in *Figure 1: STM32F103xx performance line block diagram*. Maximum current consumption *Table 13*, *Table 14* and *Table 15* updated. V_{hys}modified in *Table 34: I/O static characteristics*. *Table 48: ADC accuracy* updated. t_{VDD} modified in *Table 10: Operating conditions at power-up / power-down*. V_{FESD} value added in *Table 30: EMS characteristics*. Values corrected, note 2 modified and note 3 removed in *Table 26: Low-power mode wakeup timings*. *Table 16: Typical and maximum current consumptions in Stop and Standby modes*: Typical values added for V_{DD}/V_{BAT} = 2.4 V, *Note 2* modified, *Note 2* added. *Table 21: Typical current consumption in Standby mode* added. *On-chip peripheral current consumption on page 46* added. ACC_{HSI} values updated in *Table 24: HSI oscillator characteristics*. V_{prog} added to *Table 28: Flash memory characteristics*. Upper option byte address modified in *Figure 9: Memory map*. Typical f_{LSI} value added in *Table 25: LSI oscillator characteristics* and internal RC value corrected from 32 to 40 kHz in entire document. T_{S_temp} added to *Table 49: TS characteristics*. N_{END} modified in *Table 29: Flash memory endurance and data retention*. $T_{S\_vrefint}$ added to *Table 12: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 56*. All I/Os are CMOS and TTL compliant. *Figure 32: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})* modified. t_{JITTER} and f_{VCO} removed from *Table 27: PLL characteristics*. *Appendix A: Important notes on page 81* added. Added *Figure 14*, *Figure 15*, *Figure 16* and *Figure 18*.

Table 58. Document revision history (continued)

Date	Revision	Changes
14-Mar-2008	5	*Figure 2: Clock tree on page 20* added. Maximum T_J value given in *Table 8: Thermal characteristics on page 35*. CRC feature added (see *CRC (cyclic redundancy check) calculation unit on page 9* and *Figure 9: Memory map on page 31* for address). I_{DD} modified in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. ACC_{HSI} modified in *Table 24: HSI oscillator characteristics on page 51*, note 2 removed. P_D, T_A and T_J added, t_{prog} values modified and t_{prog} description clarified in *Table 28: Flash memory characteristics on page 52*. t_{RET} modified in *Table 29: Flash memory endurance and data retention*. $V_{NF(NRST)}$ unit corrected in *Table 37: NRST pin characteristics on page 59*. *Table 41: SPI characteristics on page 63* modified. I_{VREF} added to *Table 45: ADC characteristics on page 67*. *Table 47: ADC accuracy - limited test conditions* added. *Table 48: ADC accuracy* modified. LQFP100 package specifications updated (see *Section 6: Package characteristics on page 72*). Recommended LQFP100, LQFP 64, LQFP48 and VFQFPN36 footprints added (see *Figure 39*, *Figure 41*, *Figure 45* and *Figure 35*). *Section 6.2: Thermal characteristics on page 81* modified, *Section 6.2.1* and *Section 6.2.2* added. *Appendix A: Important notes on page 81* removed.
21-Mar-2008	6	Small text changes. *Figure 9: Memory map* clarified. In *Table 29: Flash memory endurance and data retention*: – N_{END} tested over the whole temperature range – cycling conditions specified for t_{RET} – t_{RET} min modified at T_A = 55 °C V_{25}, Avg_Slope and T_L modified in *Table 49: TS characteristics*. CRC feature removed.
22-May-2008	7	CRC feature added back. Small text changes. *Section 1: Introduction* modified. *Section 2.2: Full compatibility throughout the family* added. I_{DD} at T_A max = 105 °C added to *Table 16: Typical and maximum current consumptions in Stop and Standby modes on page 42*. I_{DD_VBAT} removed from *Table 21: Typical current consumption in Standby mode on page 47*. Values added to *Table 40: SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V) on page 62*. *Figure 26: SPI timing diagram - slave mode and CPHA = 0 on page 64* modified. *Equation 1* corrected. t_{RET} at T_A = 105 °C modified in *Table 29: Flash memory endurance and data retention on page 53*. V_{USB} added to *Table 43: USB DC electrical characteristics on page 66*. *Figure 46: LQFP100 P_D max vs. T_A on page 83* modified. Axx option added to *Table 57: Ordering information scheme on page 84*.

Table 58. Document revision history (continued)

Date	Revision	Changes
21-Jul-2008	8	*Power supply supervisor* updated and V_{DDA} added to *Table 9: General operating conditions*. Capacitance modified in *Figure 12: Power supply scheme on page 33*. Table notes revised in *Section 5: Electrical characteristics*. *Table 16: Typical and maximum current consumptions in Stop and Standby modes* modified. Data added to *Table 16: Typical and maximum current consumptions in Stop and Standby modes* and *Table 21: Typical current consumption in Standby mode* removed. f_{HSE_ext} modified in *Table 20: High-speed external user clock characteristics on page 47*. f_{PLL_IN} modified in *Table 27: PLL characteristics on page 52*. Minimum SDA and SCL fall time value for Fast mode removed from *Table 39: I^{2}C characteristics on page 61*, note 1 modified. $t_{h(NSS)}$ modified in *Table 41: SPI characteristics on page 63* and *Figure 26: SPI timing diagram - slave mode and CPHA = 0 on page 64*. C_{ADC} modified in *Table 45: ADC characteristics on page 67* and *Figure 31: Typical connection diagram using the ADC* modified. Typical T_{S_temp} value removed from *Table 49: TS characteristics on page 71*. LQFP48 package specifications updated (see *Table 55* and *Table 45*), *Section 6: Package characteristics* revised. Axx option removed from *Table 57: Ordering information scheme on page 84*. Small text changes.
22-Sep-2008	9	STM32F103x6 part numbers removed (see *Table 57: Ordering information scheme*). Small text changes. *General-purpose timers (TIMx)* and *Advanced-control timer (TIM1) on page 15* updated. Notes updated in *Table 5: Medium-density STM32F103xx pin definitions on page 26*. *Note 2* modified below *Table 6: Voltage characteristics on page 34*, $\|\Delta V_{DDx}\|$ min and $\|\Delta V_{DDx}\|$ min removed. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 38*. I_{DD} in standby mode at 85 °C modified in *Table 16: Typical and maximum current consumptions in Stop and Standby modes on page 42*. *General input/output characteristics on page 56* modified. f_{HCLK} conditions modified in *Table 30: EMS characteristics on page 54*. Θ_{JA} and pitch value modified for LFBGA100 package in *Table 56: Package thermal characteristics*. Small text changes.