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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vbt7tr

2.1 Device overview

Table 2. STM32F103xx medium-density device features and peripheral counts

Peripheral		STM32F103Tx	STM32F103Cx		STM32F103Rx		STM32F103Vx	
Flash - Kbytes		64	64	128	64	128	64	128
SRAM - Kbytes		20	20	20	20		20	
Timers	General-purpose	3	3	3	3		3	
	Advanced-control	1	1		1		1	
Communication	SPI	1	2	2	2		2	
	I^2C	1	2	2	2		2	
	USART	2	3	3	3		3	
	USB	1	1	1	1		1	
	CAN	1	1	1	1		1	
GPIOs		26	37		51		80	
12-bit synchronized ADC Number of channels		2 10 channels	2 10 channels		2 16 channels		2 16 channels	
CPU frequency		72 MHz						
Operating voltage		2.0 to 3.6 V						
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C (see *Table 9*) Junction temperature: –40 to + 125 °C (see *Table 9*)						
Packages		VFQFPN36	LQFP48		LQFP64, TFBGA64		LQFP100, LFBGA100	

Table 5. Medium-density STM32F103xx pin definitions

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
A3	-		-	1	-	PE2	I/O	FT	PE2	TRACECK	
B3	-		-	2	-	PE3	I/O	FT	PE3	TRACED0	
C3	-		-	3	-	PE4	I/O	FT	PE4	TRACED1	
D3	-		-	4	-	PE5	I/O	FT	PE5	TRACED2	
E3	-		-	5	-	PE6	I/O	FT	PE6	TRACED3	
B2	1	B2	1	6	-	V_{BAT}	S		V_{BAT}		
A2	2	A2	2	7	-	PC13-TAMPER-RTC(4)	I/O		PC13(5)	TAMPER-RTC	
A1	3	A1	3	8	-	PC14-OSC32_IN(4)	I/O		PC14(5)	OSC32_IN	
B1	4	B1	4	9	-	PC15-OSC32_OUT(4)	I/O		PC15(5)	OSC32_OUT	
C2	-	-	-	10	-	V_{SS_5}	S		V_{SS_5}		
D2	-	-	-	11	-	V_{DD_5}	S		V_{DD_5}		
C1	5	C1	5	12	2	OSC_IN	I		OSC_IN		
D1	6	D1	6	13	3	OSC_OUT	O		OSC_OUT		
E1	7	E1	7	14	4	NRST	I/O		NRST		
F1	-	E3	8	15	-	PC0	I/O		PC0	ADC12_IN10	
F2	-	E2	9	16	-	PC1	I/O		PC1	ADC12_IN11	
E2	-	F2	10	17	-	PC2	I/O		PC2	ADC12_IN12	
F3	-	-(6)	11	18	-	PC3	I/O		PC3	ADC12_IN13	
G1	8	F1	12	19	5	V_{SSA}	S		V_{SSA}		
H1	-	-	-	20	-	V_{REF-}	S		V_{REF-}		
J1	-	G1(6)	-	21	-	V_{REF+}	S		V_{REF+}		
K1	9	H1	13	22	6	V_{DDA}	S		V_{DDA}		
G2	10	G2	14	23	7	PA0-WKUP	I/O		PA0	WKUP/ USART2_CTS(7)/ ADC12_IN0/ TIM2_CH1_ETR(7)	
H2	11	H2	15	24	8	PA1	I/O		PA1	USART2_RTS(7)/ ADC12_IN1/ TIM2_CH2(7)	
J2	12	F3	16	25	9	PA2	I/O		PA2	USART2_TX(7)/ ADC12_IN2/ TIM2_CH3(7)	

Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
K2	13	G3	17	26	10	PA3	I/O		PA3	USART2_RX(7)/ ADC12_IN3/ TIM2_CH4(7)	
E4	-	C2	18	27	-	V_{SS_4}	S		V_{SS_4}		
F4	-	D2	19	28	-	V_{DD_4}	S		V_{DD_4}		
G3	14	H3	20	29	11	PA4	I/O		PA4	SPI1_NSS(7)/ USART2_CK(7)/ ADC12_IN4	
H3	15	F4	21	30	12	PA5	I/O		PA5	SPI1_SCK(7)/ ADC12_IN5	
J3	16	G4	22	31	13	PA6	I/O		PA6	SPI1_MISO(7)/ ADC12_IN6/ TIM3_CH1(7)	TIM1_BKIN
K3	17	H4	23	32	14	PA7	I/O		PA7	SPI1_MOSI(7)/ ADC12_IN7/ TIM3_CH2(7)	TIM1_CH1N
G4	-	H5	24	33		PC4	I/O		PC4	ADC12_IN14	
H4	-	H6	25	34		PC5	I/O		PC5	ADC12_IN15	
J4	18	F5	26	35	15	PB0	I/O		PB0	ADC12_IN8/ TIM3_CH3(7)	TIM1_CH2N
K4	19	G5	27	36	16	PB1	I/O		PB1	ADC12_IN9/ TIM3_CH4(7)	TIM1_CH3N
G5	20	G6	28	37	17	PB2	I/O	FT	PB2/BOOT1		
H5	-	-	-	38	-	PE7	I/O	FT	PE7		TIM1_ETR
J5	-	-	-	39	-	PE8	I/O	FT	PE8		TIM1_CH1N
K5	-	-	-	40	-	PE9	I/O	FT	PE9		TIM1_CH1
G6	-	-	-	41	-	PE10	I/O	FT	PE10		TIM1_CH2N
H6	-	-	-	42	-	PE11	I/O	FT	PE11		TIM1_CH2
J6	-	-	-	43	-	PE12	I/O	FT	PE12		TIM1_CH3N
K6	-	-	-	44	-	PE13	I/O	FT	PE13		TIM1_CH3
G7	-	-	-	45	-	PE14	I/O	FT	PE14		TIM1_CH4
H7	-	-	-	46	-	PE15	I/O	FT	PE15		TIM1_BKIN
J7	21	G7	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(7)	TIM2_CH3
K7	22	H7	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(7)	TIM2_CH4
E7	23	D6	31	49	18	V_{SS_1}	S		V_{SS_1}		

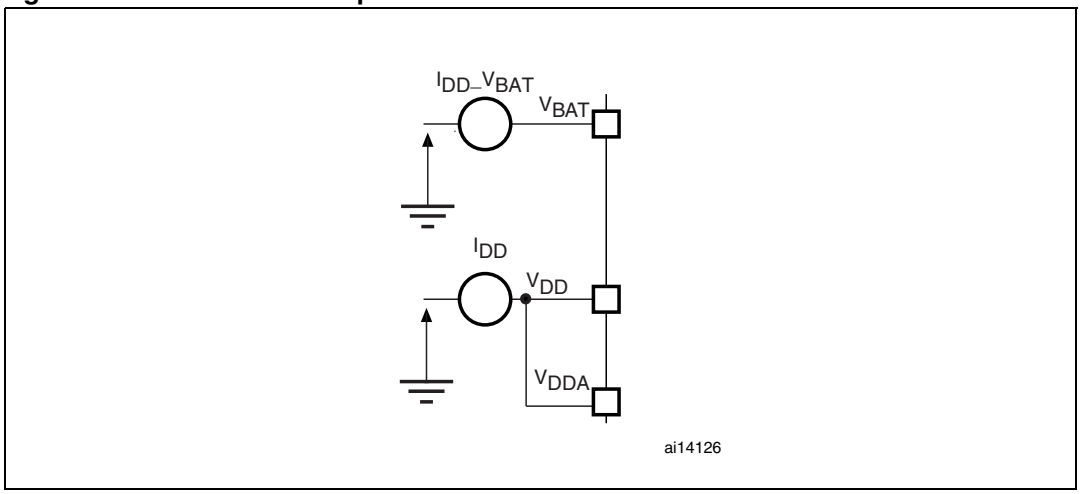
Table 5. Medium-density STM32F103xx pin definitions (continued)

Pins						Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
LFBGA100	LQFP48	TFBGA64	LQFP64	LQFP100	VFQFPN36					Default	Remap
D4	-	-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR	
C4	-	-	-	98	-	PE1	I/O	FT	PE1		
E5	47	D4	63	99	36	V_{SS_3}	S		V_{SS_3}		
F5	48	E4	64	100	1	V_{DD_3}	S		V_{DD_3}		

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 10*.
4. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 is restricted: only one I/O at a time can be used as an output, the speed has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
8. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages, and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
   The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

5.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin(2)	V_{SS} – 0.3	+5.5	
	Input voltage on any other pin(2)	V_{SS} – 0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see *Table 7: Current characteristics*). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{IN}$max while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	30	32	mA
			48 MHz	20	20.5	
			36 MHz	15.5	16	
			24 MHz	11.5	12	
			16 MHz	8.5	9	
			8 MHz	5.5	6	
		External clock(2), all peripherals disabled	72 MHz	7.5	8	
			48 MHz	6	6.5	
			36 MHz	5	5.5	
			24 MHz	4.5	5	
			16 MHz	4	4.5	
			8 MHz	3	4	

1. based on characterization, tested in production at $V_{DD\ max}$, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C	–2	±1	2.5	%
		T_A = –10 to 85 °C	–1.5	±1	2.2	%
		T_A = 0 to 70 °C	–1.3	±1	2	%
		T_A = 25 °C	–1.1	±1	1.8	%
$t_{su(HSI)}$	HSI oscillator startup time		1		2	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	µA

1. Guaranteed by design, not tested in production.
2. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption		0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

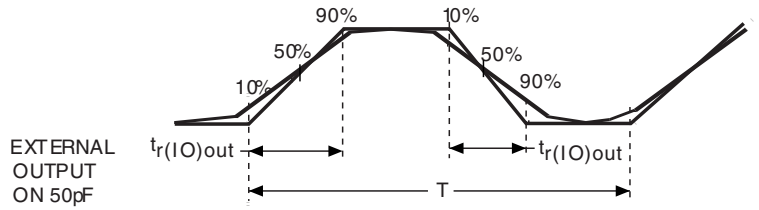
Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Figure 23. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 34*).

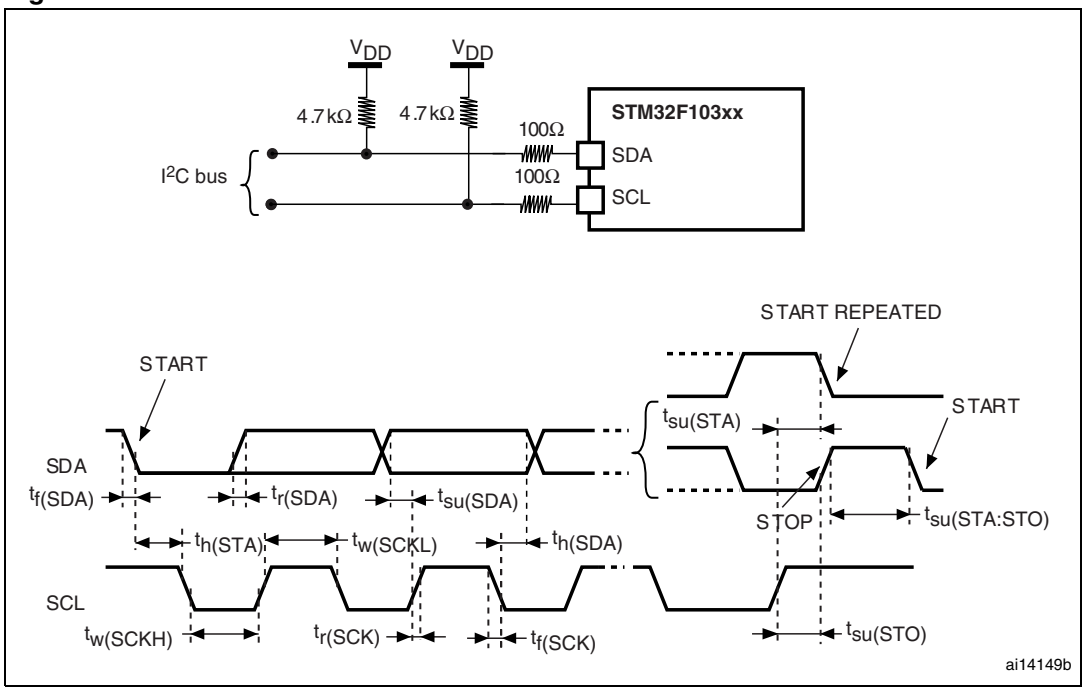
Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 37. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 25. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 t_{PCLK}		
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	73		
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (2)	Data input setup time Master mode	SPI1	1		
		SPI2	5		
$t_{su(SI)}$(2)	Data input setup time Slave mode		1		
$t_{h(MI)}$ (2)	Data input hold time Master mode	SPI1	1		
		SPI2	5		
$t_{h(SI)}$(2)	Data input hold time Slave mode		3		
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 24 MHz	0	4 t_{PCLK}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$(2)		Master mode (after enable edge)	4		

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 26. SPI timing diagram - slave mode and CPHA = 0

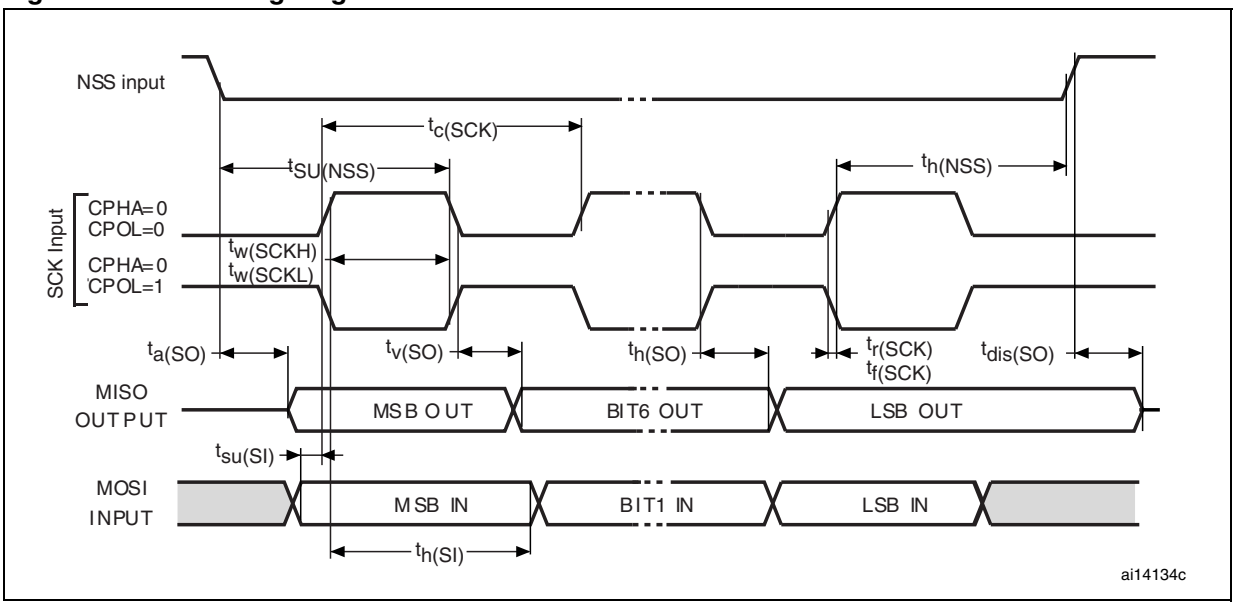
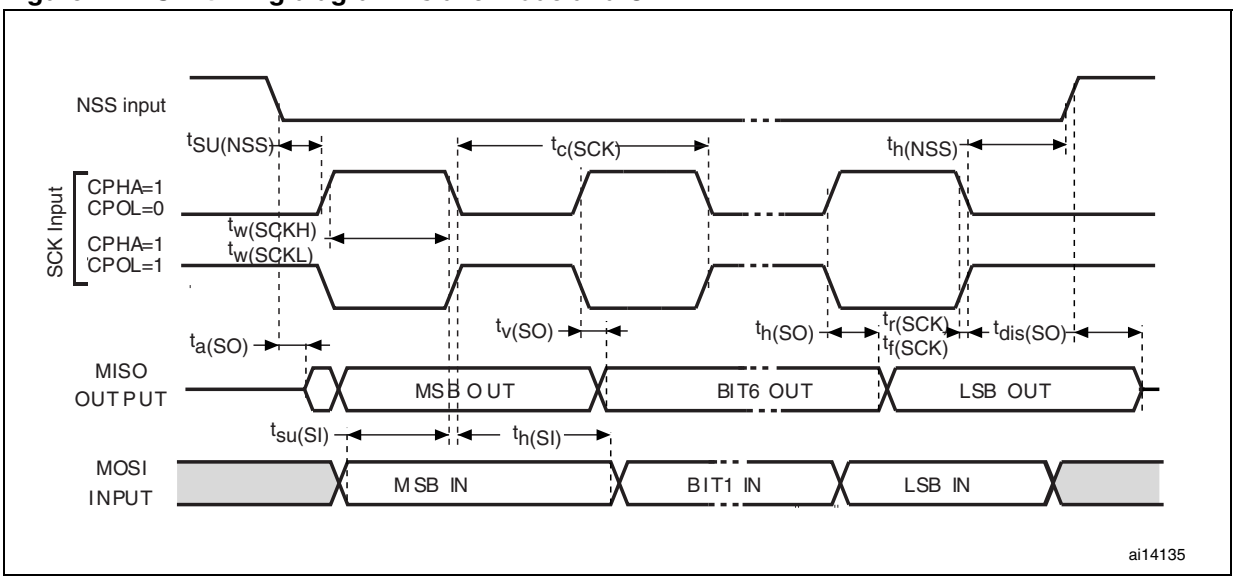
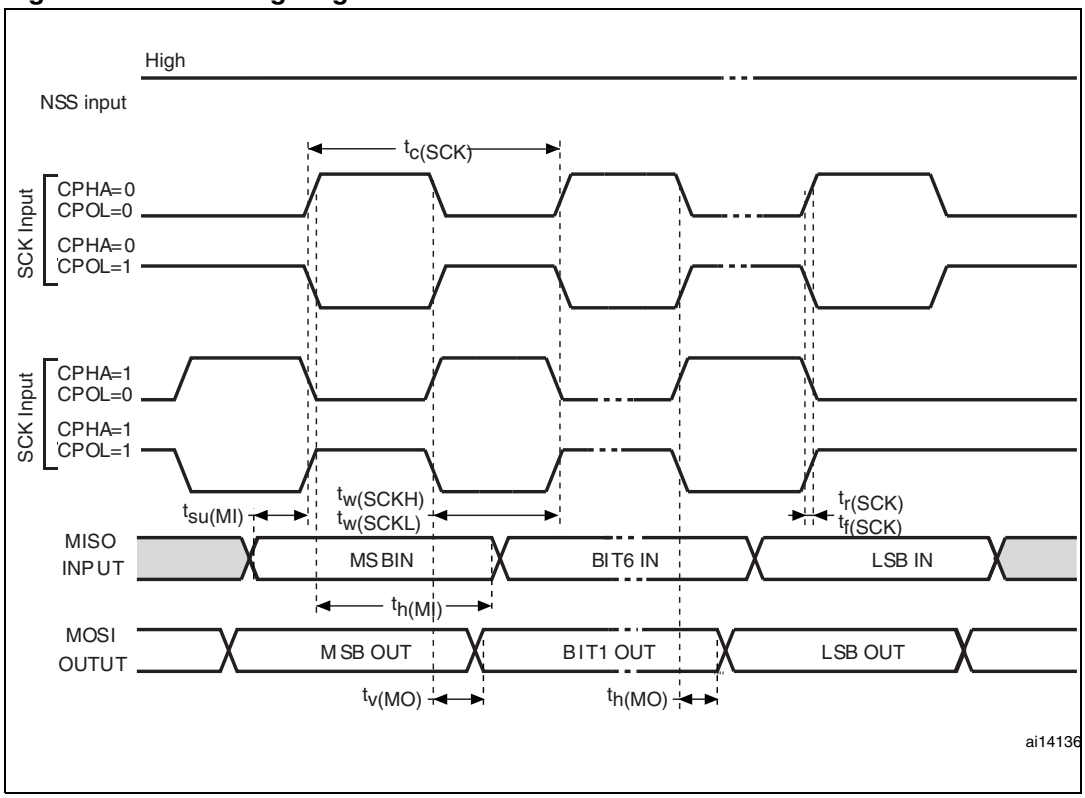


Figure 27. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 28. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

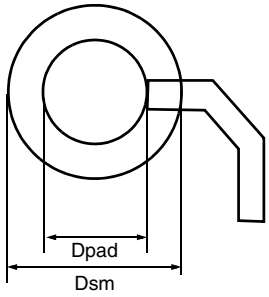
The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Figure 37. Recommended PCB design rules (0.80/0.75 mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

Figure 38. LQFP100, 100-pin low-profile quad flat package outline(1)

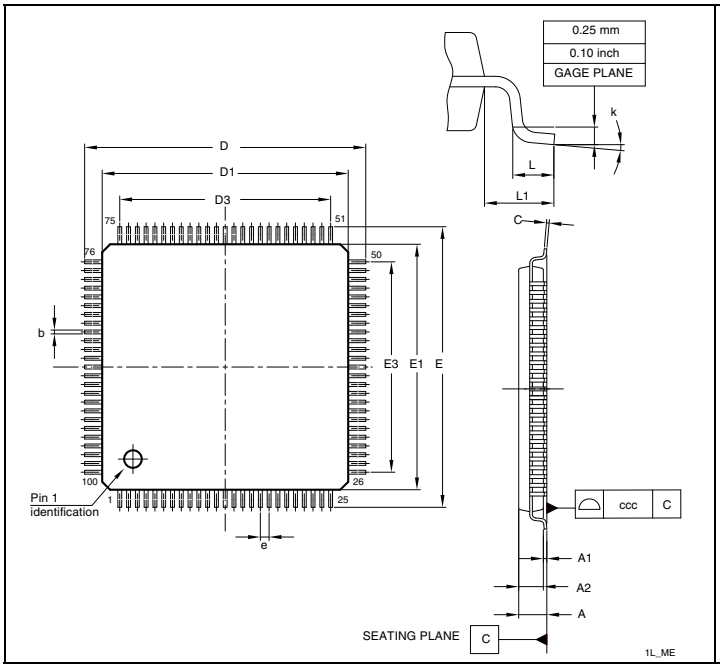
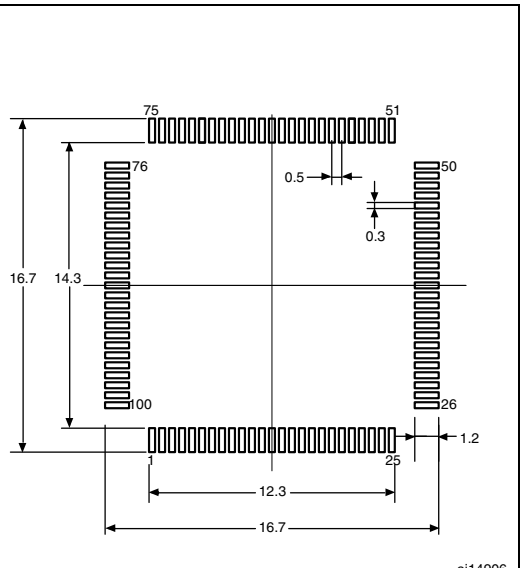


Figure 39. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 52. LQPF100, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	16	15.8	16.2	0.6299	0.622	0.6378
D1	14	13.8	14.2	0.5512	0.5433	0.5591
D3	12			0.4724		
E	16	15.8	16.2	0.6299	0.622	0.6378
E1	14	13.8	14.2	0.5512	0.5433	0.5591
E3	12			0.4724		
e	0.5			0.0197		
L	0.6	0.45	0.75	0.0236	0.0177	0.0295
L1	1			0.0394		
k	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP64, 64-pin low-profile quad flat package outline(1)

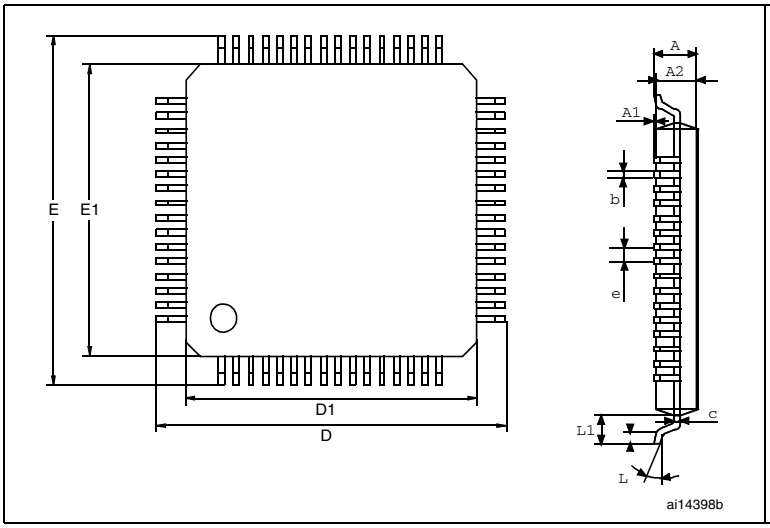
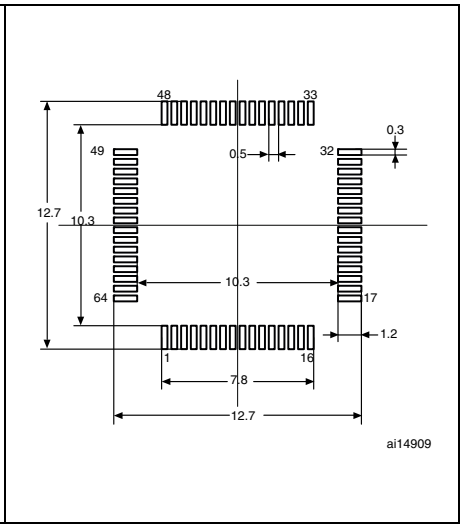


Figure 41. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 53. LQFP64, 64-pin low-profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7 Ordering information scheme

Table 57. Ordering information scheme

Example: STM32 F 103 C 8 T 7 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

103 = performance line

Pin count

T = 36 pins
C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size(1)

8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory

Package

H = BGA
T = LQFP
U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and real

1. Although STM32F103x6 devices are not described in this datasheet, orderable part numbers that do not show the A internal code after temperature range code 6 or 7 should be referred to this datasheet for the electrical characteristics. The low-density datasheet only covers STM32F103x6 devices that feature the A code.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 58. Document revision history

Date	Revision	Changes
01-jun-2007	1	Initial release.
20-Jul-2007	2	Flash memory size modified in *Note 7*, *Note 4*, *Note 7*, *Note 8* and BGA100 pins added to *Table 5: Medium-density STM32F103xx pin definitions*. *Figure 3: STM32F103xx performance line LFBGA100 ballout* added. T_{HSE} changed to T_{LSE} in *Figure 20: Low-speed external clock source AC timing diagram*. V_{BAT} ranged modified in *Power supply schemes*. $t_{SU(LSE)}$ changed to $t_{SU(HSE)}$ in *Table 22: HSE 4-16 MHz oscillator characteristics*. $I_{DD(HSI)}$ max value added to *Table 24: HSI oscillator characteristics*. Sample size modified and machine model removed in *Electrostatic discharge (ESD)*. Number of parts modified and standard reference updated in *Static latch-up*. 25 °C and 85 °C conditions removed and class name modified in *Table 33: Electrical sensitivities*. R_{PU} and R_{PD} min and max values added to *Table 34: I/O static characteristics*. R_{PU} min and max values added to *Table 37: NRST pin characteristics*. *Figure 25: I^2C bus AC waveforms and measurement circuit* and *Figure 24: Recommended NRST pin protection* corrected. Notes removed below *Table 9*, *Table 37*, *Table 43*. I_{DD} typical values changed in *Table 11: Maximum current consumption in Run and Sleep modes*. *Table 38: TIMx characteristics* modified. t_{STAB}, V_{REF+} value, t_{lat} and f_{TRIG} added to *Table 45: ADC characteristics*. In *Table 29: Flash memory endurance and data retention*, typical endurance and data retention for T_A = 85 °C added, data retention for T_A = 25 °C removed. V_{BG} changed to V_{REFINT} in *Table 12: Embedded internal reference voltage*. Document title changed. *Controller area network (CAN)* section modified. *Figure 12: Power supply scheme* modified. *Features on page 1* list optimized. Small text changes.

Table 58. Document revision history (continued)

Date	Revision	Changes
21-Jul-2008	8	*Power supply supervisor* updated and V_{DDA} added to *Table 9: General operating conditions*. Capacitance modified in *Figure 12: Power supply scheme on page 33*. Table notes revised in *Section 5: Electrical characteristics*. *Table 16: Typical and maximum current consumptions in Stop and Standby modes* modified. Data added to *Table 16: Typical and maximum current consumptions in Stop and Standby modes* and *Table 21: Typical current consumption in Standby mode* removed. f_{HSE_ext} modified in *Table 20: High-speed external user clock characteristics on page 47*. f_{PLL_IN} modified in *Table 27: PLL characteristics on page 52*. Minimum SDA and SCL fall time value for Fast mode removed from *Table 39: I^2C characteristics on page 61*, note 1 modified. $t_{h(NSS)}$ modified in *Table 41: SPI characteristics on page 63* and *Figure 26: SPI timing diagram - slave mode and CPHA = 0 on page 64*. C_{ADC} modified in *Table 45: ADC characteristics on page 67* and *Figure 31: Typical connection diagram using the ADC* modified. Typical T_{S_temp} value removed from *Table 49: TS characteristics on page 71*. LQFP48 package specifications updated (see *Table 55* and *Table 45*), *Section 6: Package characteristics* revised. Axx option removed from *Table 57: Ordering information scheme on page 84*. Small text changes.
22-Sep-2008	9	STM32F103x6 part numbers removed (see *Table 57: Ordering information scheme*). Small text changes. *General-purpose timers (TIMx)* and *Advanced-control timer (TIM1) on page 15* updated. Notes updated in *Table 5: Medium-density STM32F103xx pin definitions on page 26*. *Note 2* modified below *Table 6: Voltage characteristics on page 34*, $\lvert\Delta V_{DDx}\rvert$ min and $\lvert\Delta V_{DDx}\rvert$ min removed. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 38*. I_{DD} in standby mode at 85 °C modified in *Table 16: Typical and maximum current consumptions in Stop and Standby modes on page 42*. *General input/output characteristics on page 56* modified. f_{HCLK} conditions modified in *Table 30: EMS characteristics on page 54*. Θ_{JA} and pitch value modified for LFBGA100 package in *Table 56: Package thermal characteristics*. Small text changes.

Table 58. Document revision history (continued)

Date	Revision	Changes
23-Apr-2009	10	I/O information clarified *on page 1*. *Figure 3: STM32F103xx performance line LFBGA100 ballout* modified. *Figure 9: Memory map* modified. *Table 4: Timer feature comparison* added. PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column in *Table 5: Medium-density STM32F103xx pin definitions*. P_D for LFBGA100 corrected in *Table 9: General operating conditions*. Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified. *Figure 17* shows a typical curve (title modified). ACC_{HSI} max values modified in *Table 24: HSI oscillator characteristics*. TFBGA64 package added (see *Table 54* and *Table 42*). Small text changes.