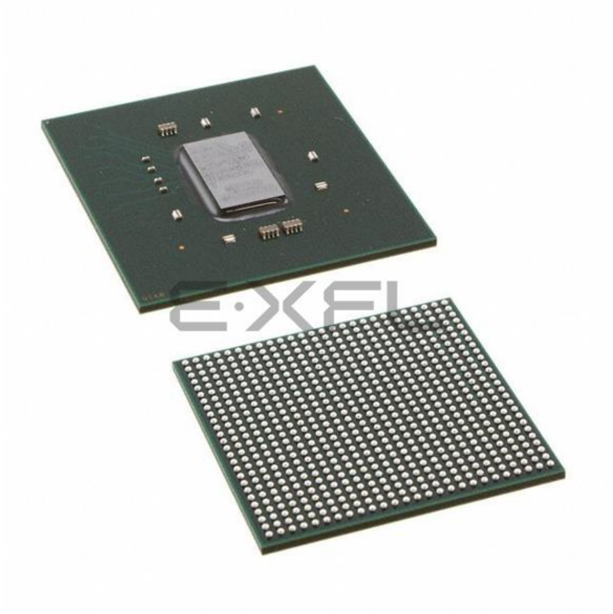
AMD Xilinx - XC7K160T-2FF676C Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	12675
Number of Logic Elements/Cells	162240
Total RAM Bits	11980800
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k160t-2ff676c

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.40	100	–0.40	100
V_{CCO} + 0.45	100	–0.45	61.7
V_{CCO} + 0.50	100	–0.50	25.8
V_{CCO} + 0.55	100	–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: **Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks[1][2]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.40	100	–0.40	100
V_{CCO} + 0.45	100	–0.45	100
V_{CCO} + 0.50	100	–0.50	100
V_{CCO} + 0.55	100	–0.55	100
V_{CCO} + 0.60	50.0	–0.60	50.0
V_{CCO} + 0.65	50.0	–0.65	50.0
V_{CCO} + 0.70	47.0	–0.70	50.0
V_{CCO} + 0.75	21.2	–0.75	50.0

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 17: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	2.0V	1866	1866	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	1066	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	800	800	800	Mb/s
RLDRAM III(3)	HP	2.0V	800	667	667	533	MHz
	HP	1.8V	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+(4)	HP	2.0V	550	500	450	450	MHz
	HP	1.8V					
	HR	N/A	500	450	400	400	MHz
RLDRAM II	HP	2.0V	533	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
LPDDR2(3)	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 18: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}(3)	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III(4)	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+(5)	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2(4)	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.31	1.42	1.64	1.51	5.27	5.63	6.05	4.13	6.03	6.49	7.04	4.64	ns
LVTTL_S8	1.31	1.42	1.64	1.51	4.45	4.83	5.30	3.86	5.21	5.69	6.29	4.38	ns
LVTTL_S12	1.31	1.42	1.64	1.51	4.45	4.83	5.29	3.84	5.21	5.69	6.28	4.36	ns
LVTTL_S16	1.31	1.42	1.64	1.51	3.47	3.88	4.40	3.39	4.23	4.74	5.39	3.91	ns
LVTTL_S24	1.31	1.42	1.64	1.51	3.58	3.99	4.51	3.61	4.34	4.85	5.50	4.13	ns
LVTTL_F4	1.31	1.42	1.64	1.51	4.70	4.98	5.29	3.58	5.46	5.84	6.28	4.09	ns
LVTTL_F8	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.06	4.42	4.92	5.55	3.58	ns
LVTTL_F12	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.05	4.42	4.92	5.55	3.56	ns
LVTTL_F16	1.31	1.42	1.64	1.51	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVTTL_F24	1.31	1.42	1.64	1.51	2.41	2.64	2.89	2.94	3.17	3.50	3.88	3.45	ns
LVDS_25(1)	0.64	0.68	0.80	0.83	1.36	1.47	1.55	1.58	2.12	2.33	2.54	2.09	ns
MINI_LVDS_25	0.68	0.70	0.79	0.83	1.36	1.47	1.55	1.59	2.12	2.33	2.54	2.11	ns
BLVDS_25(1)	0.65	0.69	0.80	0.83	1.83	2.02	2.20	2.16	2.59	2.88	3.19	2.67	ns
RSDS_25 (point to point)(1)	0.63	0.68	0.79	0.83	1.36	1.48	1.55	1.59	2.12	2.34	2.54	2.11	ns
PPDS_25(1)	0.65	0.69	0.80	0.83	1.36	1.49	1.58	1.59	2.12	2.35	2.57	2.11	ns
TMDS_33(1)	0.72	0.76	0.86	0.83	1.43	1.54	1.60	1.70	2.19	2.40	2.59	2.22	ns
PCI33_3(1)	1.28	1.41	1.65	1.50	2.71	3.08	3.52	3.42	3.47	3.94	4.51	3.94	ns
HSUL_12	0.63	0.64	0.71	0.79	2.06	2.31	2.59	2.13	2.82	3.17	3.58	2.64	ns
DIFF_HSUL_12	0.58	0.61	0.70	0.81	1.83	2.04	2.26	1.92	2.59	2.90	3.25	2.44	ns
HSTL_I_S	0.61	0.64	0.73	0.79	1.55	1.69	1.80	1.91	2.31	2.55	2.79	2.42	ns
HSTL_II_S	0.61	0.64	0.73	0.78	1.21	1.34	1.43	1.70	1.97	2.20	2.42	2.22	ns
HSTL_I_18_S	0.64	0.67	0.76	0.79	1.28	1.39	1.45	1.58	2.04	2.25	2.44	2.09	ns
HSTL_II_18_S	0.64	0.67	0.76	0.79	1.18	1.31	1.40	1.69	1.94	2.17	2.39	2.20	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.78	1.42	1.54	1.61	1.84	2.18	2.40	2.60	2.36	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.79	1.15	1.24	1.27	1.78	1.91	2.10	2.26	2.30	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	0.79	1.27	1.38	1.43	1.67	2.03	2.24	2.42	2.19	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	0.81	1.14	1.23	1.26	1.72	1.90	2.09	2.25	2.23	ns

Table 19: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVCMOS15_S16	0.66	0.69	0.81	0.90	1.76	1.95	2.13	1.91	2.52	2.81	3.12	2.42	ns
LVCMOS15_F4	0.66	0.69	0.81	0.90	3.39	3.60	3.80	1.98	4.15	4.46	4.79	2.50	ns
LVCMOS15_F8	0.66	0.69	0.81	0.90	1.79	1.99	2.18	1.92	2.55	2.85	3.17	2.44	ns
LVCMOS15_F12	0.66	0.69	0.81	0.90	1.40	1.54	1.65	1.67	2.16	2.40	2.64	2.19	ns
LVCMOS15_F16	0.66	0.69	0.81	0.90	1.37	1.51	1.61	1.66	2.13	2.37	2.60	2.17	ns
LVCMOS12_S4	0.88	0.91	1.00	1.01	3.85	4.22	4.69	2.89	4.61	5.08	5.68	3.41	ns
LVCMOS12_S8	0.88	0.91	1.00	1.01	2.52	2.96	3.52	2.41	3.28	3.82	4.51	2.92	ns
LVCMOS12_S12(1)	0.88	0.91	1.00	1.01	2.06	2.31	2.59	2.11	2.82	3.17	3.58	2.63	ns
LVCMOS12_F4	0.88	0.91	1.00	1.01	3.44	3.73	4.06	2.30	4.20	4.59	5.05	2.81	ns
LVCMOS12_F8	0.88	0.91	1.00	1.01	1.72	2.04	2.40	1.86	2.48	2.90	3.39	2.38	ns
LVCMOS12_F12(1)	0.88	0.91	1.00	1.01	1.54	1.71	1.87	1.69	2.30	2.57	2.86	2.20	ns
SSTL135_S	0.61	0.64	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
SSTL15_S	0.61	0.64	0.73	0.73	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
SSTL18_I_S	0.64	0.67	0.76	0.79	1.59	1.74	1.85	1.95	2.35	2.60	2.84	2.47	ns
SSTL18_II_S	0.64	0.67	0.76	0.78	1.27	1.40	1.50	1.63	2.03	2.26	2.49	2.14	ns
DIFF_SSTL135_S	0.59	0.61	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
DIFF_SSTL15_S	0.63	0.67	0.77	0.79	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	0.79	1.50	1.63	1.72	1.95	2.26	2.49	2.71	2.47	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	0.79	1.13	1.22	1.25	1.66	1.89	2.08	2.24	2.17	ns
SSTL135_F	0.61	0.64	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
SSTL15_F	0.61	0.64	0.73	0.73	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
SSTL18_I_F	0.64	0.67	0.76	0.79	1.12	1.22	1.26	1.44	1.88	2.08	2.25	1.95	ns
SSTL18_II_F	0.64	0.67	0.76	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
DIFF_SSTL135_F	0.59	0.61	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
DIFF_SSTL15_F	0.63	0.67	0.77	0.79	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	0.79	1.10	1.19	1.23	1.52	1.86	2.05	2.22	2.03	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	0.79	1.02	1.10	1.14	1.50	1.78	1.96	2.13	2.02	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 21 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	0.62	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	2.17	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	1.86	ns

Output Serializer/Deserializer Switching Characteristics

Table 25: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.44/–0.24	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.49/–0.15	0.56/–0.15	0.68/–0.15	0.67/–0.25	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.27/–0.15	0.30/–0.15	0.34/–0.15	0.46/–0.25	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/–0.15	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/–0.15	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Table 31: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	0.34/0.40	ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	0.54/0.19	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	0.65/0.37	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	0.60/0.38	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.76	0.83	0.93	1.06	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing(11)	1.59/–0.68	1.76/–0.68	2.01/–0.68	2.07/–0.60	ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	372.44	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	372.44	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	317.36	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	322.48	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	322.48	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.27	427.35	350.88	267.38	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	372.44	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	254.13	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 32: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.24/ 0.12	0.27/ 0.14	0.31/ 0.16	0.38/ 0.12	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.28/ 0.13	0.32/ 0.14	0.39/ 0.15	0.51/ 0.16	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.15/ 0.15	0.17/ 0.17	0.20/ 0.20	0.31/ 0.21	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.21/ 0.19	0.27/ 0.22	0.35/ 0.26	0.46/ 0.20	ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.21/ 0.12	0.24/ 0.14	0.27/ 0.16	0.31/ 0.12	ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.22/ 0.13	0.25/ 0.14	0.30/ 0.15	0.34/ 0.16	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B,} input to M register CLK using multiplier	2.04/ –0.01	2.34/ –0.01	2.79/ –0.01	3.66/ –0.06	ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$	{A, D} input to AD register CLK	1.09/ –0.02	1.25/ –0.02	1.49/ –0.02	1.94/ –0.23	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$	{A, B,} input to P register CLK using multiplier	3.41/ –0.24	3.90/ –0.24	4.64/ –0.24	5.89/ –0.41	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.33/ –0.62	3.81/ –0.62	4.53/ –0.62	5.70/ –1.42	ns
$T_{DSPDCK\_\{A, B\} \_PREG}$/ $T_{DSPCKD\_\{A, B\} \_PREG}$	A or B input to P register CLK not using multiplier	1.47/ –0.24	1.68/ –0.24	2.00/ –0.24	2.37/ –0.41	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.30/ –0.22	1.49/ –0.22	1.78/ –0.22	2.11/ –0.36	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.12/ –0.13	1.28/ –0.13	1.52/ –0.13	1.81/ –0.21	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.30/ 0.05	0.36/ 0.06	0.44/ 0.09	0.55/ 0.09	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.24/ 0.08	0.29/ 0.09	0.36/ 0.11	0.43/ 0.11	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.31/ –0.02	0.36/ –0.02	0.44/ –0.02	0.58/ 0.12	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.26/ 0.15	0.29/ 0.17	0.33/ 0.20	0.39/ 0.25	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.31/ 0.01	0.36/ 0.01	0.45/ 0.01	0.54/ 0.00	ns

Table 36: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.12	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.20/0.16	0.23/0.20	0.38/0.21	0.28/0.09	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	560.00	MHz

Table 37: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC7K70T	0.29	0.40	0.40	0.47	ns
		XC7K160T	0.42	0.53	0.57	0.59	ns
		XC7K325T	0.59	0.74	0.79	0.91	ns
		XC7K355T	0.45	0.57	0.59	0.69	ns
		XC7K410T	0.60	0.74	0.79	0.91	ns
		XC7K420T	0.60	0.74	0.79	0.91	ns
		XC7K480T	0.60	0.74	0.79	0.91	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	0.12	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

Table 38: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN Setup/Hold	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
   See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 39: **PLL Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F_{INMAX}	Maximum Input Clock Frequency	1066.00	933.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum Input Clock Frequency	19.00	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25.00	25.00	25.00	25.00	%
	Allowable Input Duty Cycle: 50—199 MHz	30.00	30.00	30.00	30.00	%
	Allowable Input Duty Cycle: 200—399 MHz	35.00	35.00	35.00	35.00	%
	Allowable Input Duty Cycle: 400—499 MHz	40.00	40.00	40.00	40.00	%
	Allowable Input Duty Cycle: >500 MHz	45.00	45.00	45.00	45.00	%
PLL_F_{VCOMIN}	Minimum PLL VCO Frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO Frequency	2133.00	1866.00	1600.00	1600.00	MHz
PLL_$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical(1)	1.00	1.00	1.00	1.00	MHz
	High PLL Bandwidth at Typical(1)	4.00	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL Output Jitter	Note 3				
PLL_$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(4)	0.20	0.20	0.20	0.25	ns
PLL_$T_{LOCKMAX}$	PLL Maximum Lock Time	100	100	100	100	µs
PLL_F_{OUTMAX}	PLL Maximum Output Frequency	1066.00	933.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL Minimum Output Frequency(5)	6.25	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
PLL_$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns

Table 42: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7K70T	0.95	0.95	0.95	1.74	ns
		XC7K160T	0.96	0.96	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 43: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7K70T	0.84	0.84	0.84	1.45	ns
		XC7K160T	0.89	0.89	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 44: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* BUFIO.						
$T_{ICKOFCS}$	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.90	ns

Table 47: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No Delay clock-capable clock input and IFF(2) with PLL	XC7K70T	2.75/–0.32	3.04/–0.32	3.33/–0.32	2.42/–0.54	ns
		XC7K160T	2.85/–0.31	3.16/–0.31	3.46/–0.31	2.59/–0.56	ns
		XC7K325T	2.91/–0.27	3.24/–0.27	3.54/–0.27	2.80/–0.56	ns
		XC7K355T	2.79/–0.27	3.12/–0.27	3.40/–0.27	2.67/–0.52	ns
		XC7K410T	2.91/–0.27	3.24/–0.27	3.53/–0.27	2.78/–0.56	ns
		XC7K420T	2.83/–0.20	3.12/–0.20	3.41/–0.20	2.61/–0.50	ns
		XC7K480T	2.83/–0.20	3.12/–0.20	3.41/–0.20	2.61/–0.50	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	–0.44/1.87	ns
	Setup/Hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	–0.44/1.87	ns

Table 49: Sample Window

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{SAMP}	Sampling Error at Receiver Pins(1)	0.51	0.56	0.61	0.56	ns
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	0.30	0.35	0.40	0.35	ns

Notes:

1. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 53: **GTX Transceiver Performance *(Cont'd)***

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1[1]		-2L[2]		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
$F_{GQPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	175.01	175.01	156.25	125.00	MHz

Table 55: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

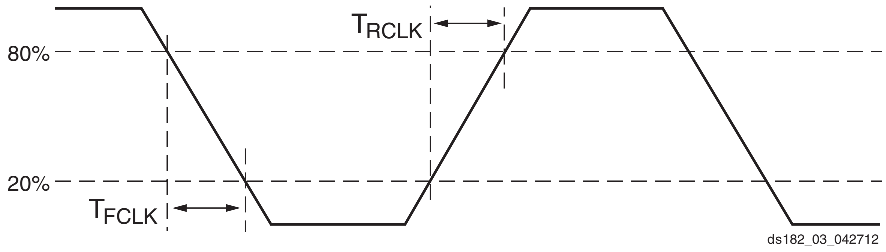

Figure 3: **Reference Clock Timing Parameters**

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: **PCI Express Protocol Characteristics(1)**

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(3)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 63: **CEI-6G and CEI-11G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter[1]	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance[1]	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter[2]	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance[2]	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: **SFP+ Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40[1]	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40[1]	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 67: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference[5]						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for new BitGen option XADCEnhancedLinearity = ON.
3. See the ADC chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
4. See the Timing chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 68: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T_{PL}[1]	Program latency	5	5	5	5	ms, Max
T_{POR}[1]	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250	250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay	150	150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	70.00	MHz, Max

Revision History

The following table shows the revision history for this document:

Date	Version	Description
03/01/11	1.0	Initial Xilinx release.
04/01/11	1.1	Added the XC7K355T, XC7K420T, and XC7K480T devices throughout data sheet. Added the extended temperature range discussion to page 1. Updated V_{CCAUX_IO} in Table 2. Edits to clarify Power-On/Off Power Supply Sequencing power sequencing discussion. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7. Updated MMCM_F_{INDUTY} and added $F_{INJITTER}$, $T_{OUTJITTER}$, $T_{EXTFDVAR}$, and Note 3 to Table 38. Removed the SBG324 package from Table 50. Updated the Notice of Disclaimer.
10/04/11	1.2	Replaced -1L with -2L throughout this data sheet. Updated Min/Max values and removed Note 5 from Table 2. Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8. Updated V_{ICM} in Table 12 and Table 13. Added Note 1 to table 12. Updated Table 69 including adding Note 1. Added *Absolute Maximum Ratings for GTX Transceivers*. Revised the reference clock maximum frequency (F_{GCLK}) in Table 55. Added Table 57. Added LVTTL and removed SSTL135_II and SSTL15_II specifications from Table 19. Removed HSTL_III from Table 20. Removed the *I/O Standard Adjustment Measurement Methodology* section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT\_JIT}$ in Table 26. Added T_{AS}/T_{AH} to Table 28. Added $T_{RDCK\_DI\_WF\_NC}$/$T_{RCKD\_DI\_WF\_NC}$ and $T_{RDCK\_DI\_RF}$/$T_{RCKD\_DI\_RF}$ to Table 31. Completely updated Table 68. Updated the AC Switching Characteristics in Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 26 through Table 38, Table 40 though Table 37, and Table 67.
11/03/11	1.3	Revised the V_{OCM} specification in Table 12. Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 38 and PLL to the symbol names in Table 39. In Table 40 through Table 47, updated the pin-to-pin descriptions with the SSTL15 standard. Updated units in Table 49.
02/13/12	1.4	Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical values to Table 3. Updated the notes in Table 6. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8. Rearranged Table 9, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11. Revised the specifications in Table 12 and Table 13. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 67. Revised DDR LVDS transmitter data width in Table 16. Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 28 as they are no longer applicable. Updated specifications in Table 68. Updated Note 1 in Table 37. In the GTX Transceiver DC Input and Output Levels section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 51. Added Note 4 to Table 53. In Table 55, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 57. Added Table 58 and Table 59 along with GTX Transceiver Protocol Jitter Characteristics in Table 60 through Table 65.
05/23/12	1.5	Reorganized entire data sheet including adding Table 44 and Table 48. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing, page 6 with regards to GTX transceivers. Updated many parameters in Table 9 including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 16 and removed notes 2 and 3. Updated Table 17. Updated the AC Switching Characteristics based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and -2L (0.9V) speed specifications throughout the document. In Table 31, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 55. Updated many of the XADC specifications in Table 67 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 68 to Table 38 and Table 39.

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