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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	12675
Number of Logic Elements/Cells	162240
Total RAM Bits	11980800
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k160t-3ffg676e

Table 2: Recommended Operating Conditions ⁽¹⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
$V_{MGTAVTTRCAL}$ ⁽⁸⁾	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

- All voltages are relative to ground.
- V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .
- Each voltage listed requires the filter circuit described in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#).
- For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V $\pm 3\%$ for lower power consumption.
- For lower power consumption, $V_{MGTAVCC}$ should be 1.0V $\pm 3\%$ over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	μA
C_{IN} ⁽²⁾	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$	90	–	330	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$	68	–	250	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	34	–	220	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	23	–	150	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	12	–	120	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3V$	68	–	330	μA
	Pad pull-down (when selected) @ $V_{IN} = 1.8V$	45	–	180	μA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT} ⁽³⁾	Battery supply current	–	–	150	nA

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than T_{VCCO2VCCAUX} for each power-on/off cycle to maintain device reliability levels.
- The T_{VCCO2VCCAUX} time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTVCCAUX}. Both V_{MGTAVCC} and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

- When V_{MGTAVTT} is powered before V_{MGTAVCC} and V_{MGTAVTT} - V_{MGTAVCC} > 150 mV and V_{MGTAVCC} < 0.7V, the V_{MGTAVTT} current draw can increase by 460 mA per transceiver during V_{MGTAVCC} ramp up. The duration of the current draw can be up to 0.3 x T_{MGTAVCC} (ramp time from GND to 90% of V_{MGTAVCC}). The reverse is true for power-down.
- When V_{MGTAVTT} is powered before V_{CCINT} and V_{MGTAVTT} - V_{CCINT} > 150 mV and V_{CCINT} < 0.7V, the V_{MGTAVTT} current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 7 shows the minimum current, in addition to I_{CCQ} , that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

Table 7: Power-On Current for Kintex-7 Devices

Device	$I_{CCINTMIN}$ Typ ⁽¹⁾	$I_{CCAUXMIN}$ Typ ⁽¹⁾	I_{CCOMIN} Typ ⁽¹⁾	I_{CCAUX_IOMIN} Typ ⁽¹⁾	$I_{CCBRAMMIN}$ Typ ⁽¹⁾	Units
XC7K70T	$I_{CCINTQ} + 450$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K160T	$I_{CCINTQ} + 550$	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K325T	$I_{CCINTQ} + 600$	$I_{CCAUXQ} + 80$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K355T	$I_{CCINTQ} + 1450$	$I_{CCAUXQ} + 109$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 81$	mA
XC7K410T	$I_{CCINTQ} + 1500$	$I_{CCAUXQ} + 125$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 90$	mA
XC7K420T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA
XC7K480T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA

Notes:

- Typical values are specified at nominal voltage, 25°C.
- Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 8: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

Table 10: Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$			$V_{OCM}^{(3)}$			$V_{OD}^{(4)}$		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	—	—	—	1.250	—	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO}-0.405$	$V_{CCO}-0.300$	$V_{CCO}-0.190$	0.400	0.600	0.800

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{OCM} is the output common mode voltage.
- V_{OD} is the output differential voltage ($Q - \bar{Q}$).
- V_{OD} for BLVDS will vary significantly depending on topology and loading.
- LVDS_25 is specified in Table 12.
- LVDS is specified in Table 13.

Table 11: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	—	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	—	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{OL} is the single-ended low-output voltage.
- V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in ISE® software 14.3 v1.07 for the -3, -2, -2L(1.0V), -1, and v1.06 for -2L(0.9V) speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 14](#) correlates the current status of each Kintex-7 device on a per speed grade basis.

Table 14: Kintex-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7K70T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K160T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K325T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K355T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K410T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K420T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K480T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_I_F	0.61	0.64	0.73	0.79	1.10	1.19	1.23	1.41	1.86	2.05	2.22	1.92	ns
HSTL_II_F	0.61	0.64	0.73	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
HSTL_I_18_F	0.64	0.67	0.76	0.79	1.05	1.18	1.28	1.44	1.81	2.04	2.27	1.95	ns
HSTL_II_18_F	0.64	0.67	0.76	0.79	1.03	1.14	1.23	1.42	1.79	2.00	2.22	1.94	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	0.78	1.09	1.18	1.22	1.48	1.85	2.04	2.21	2.00	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	0.79	1.02	1.11	1.14	1.48	1.78	1.97	2.13	2.00	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	0.79	1.08	1.17	1.21	1.48	1.84	2.03	2.20	2.00	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	0.81	1.01	1.10	1.13	1.48	1.77	1.96	2.12	2.00	ns
LVC MOS33_S4	1.31	1.40	1.60	1.54	5.23	5.61	6.09	4.13	5.99	6.47	7.08	4.64	ns
LVC MOS33_S8	1.31	1.40	1.60	1.54	4.46	4.85	5.33	3.84	5.22	5.71	6.32	4.36	ns
LVC MOS33_S12	1.31	1.40	1.60	1.54	3.46	3.89	4.42	3.41	4.22	4.75	5.41	3.92	ns
LVC MOS33_S16	1.31	1.40	1.60	1.54	3.06	3.43	3.88	3.72	3.82	4.29	4.87	4.23	ns
LVC MOS33_F4	1.31	1.40	1.60	1.54	4.70	5.01	5.36	3.58	5.46	5.87	6.35	4.09	ns
LVC MOS33_F8	1.31	1.40	1.60	1.54	3.62	4.04	4.56	3.06	4.38	4.90	5.55	3.58	ns
LVC MOS33_F12	1.31	1.40	1.60	1.54	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVC MOS33_F16	1.31	1.40	1.60	1.54	2.44	2.69	2.96	2.88	3.20	3.55	3.95	3.39	ns
LVC MOS25_S4	1.08	1.16	1.32	1.36	4.49	4.80	5.16	3.44	5.25	5.66	6.15	3.95	ns
LVC MOS25_S8	1.08	1.16	1.32	1.36	3.66	4.04	4.49	3.20	4.42	4.90	5.48	3.72	ns
LVC MOS25_S12	1.08	1.16	1.32	1.36	2.77	3.10	3.49	2.80	3.53	3.96	4.48	3.31	ns
LVC MOS25_S16	1.08	1.16	1.32	1.36	3.24	3.62	4.09	3.14	4.00	4.48	5.08	3.66	ns
LVC MOS25_F4	1.08	1.16	1.32	1.36	3.96	4.31	4.72	3.06	4.72	5.17	5.71	3.58	ns
LVC MOS25_F8	1.08	1.16	1.32	1.36	2.43	2.87	3.42	2.50	3.19	3.73	4.41	3.02	ns
LVC MOS25_F12	1.08	1.16	1.32	1.36	2.23	2.63	3.13	2.48	2.99	3.49	4.12	3.00	ns
LVC MOS25_F16	1.08	1.16	1.32	1.36	1.92	2.17	2.45	2.33	2.68	3.03	3.44	2.84	ns
LVC MOS18_S4	0.64	0.66	0.74	0.87	3.24	3.45	3.66	1.91	4.00	4.31	4.65	2.42	ns
LVC MOS18_S8	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVC MOS18_S12	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVC MOS18_S16	0.64	0.66	0.74	0.87	1.82	2.03	2.24	1.84	2.58	2.89	3.23	2.36	ns
LVC MOS18_S24 ⁽¹⁾	0.64	0.66	0.74	0.87	1.74	1.92	2.08	1.92	2.50	2.78	3.07	2.44	ns
LVC MOS18_F4	0.64	0.66	0.74	0.87	3.12	3.31	3.49	1.77	3.88	4.17	4.48	2.28	ns
LVC MOS18_F8	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVC MOS18_F12	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVC MOS18_F16	0.64	0.66	0.74	0.87	1.52	1.68	1.81	1.72	2.28	2.54	2.80	2.23	ns
LVC MOS18_F24 ⁽¹⁾	0.64	0.66	0.74	0.87	1.34	1.46	1.55	1.66	2.10	2.32	2.54	2.17	ns
LVC MOS15_S4	0.66	0.69	0.81	0.90	3.48	3.74	4.03	2.22	4.24	4.60	5.02	2.73	ns
LVC MOS15_S8	0.66	0.69	0.81	0.90	2.37	2.67	3.01	2.41	3.13	3.53	4.00	2.92	ns
LVC MOS15_S12	0.66	0.69	0.81	0.90	1.83	2.03	2.23	1.91	2.59	2.89	3.22	2.42	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVC MOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVC MOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVC MOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVC MOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVC MOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVC MOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVC MOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVC MOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVC MOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVC MOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVC MOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVC MOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVC MOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVC MOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVC MOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVC MOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVC MOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVC MOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVC MOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVC MOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVC MOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVC MOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVC MOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVC MOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVC MOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVC MOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVC MOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVC MOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVC MOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVC MOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVC MOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
T _{ISCKCK_BITSLIP} / T _{ISCKC_BITSLIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	0.02/0.21	ns
T _{ISCKCK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	0.51/−0.22	ns
T _{ISCKCK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	−0.17/0.40	ns
Setup/Hold for Data Lines						
T _{ISDCK_D} /T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.03/0.19	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	0.19/0.19	ns
Sequential Delays						
T _{ISCO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	0.67	ns
Propagation Delays						
T _{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	0.14	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.44/−0.24	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	0.67/−0.25	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input Setup/Hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	0.46/−0.25	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/−0.15	ns
T _{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.70	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/−0.15	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Block RAM and FIFO Switching Characteristics

Table 31: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO_DO_REG}^{(1)}$	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.57	1.80	2.08	2.44	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.54	0.63	0.75	0.86	ns, Max
$T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.35	2.58	3.26	4.49	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.62	0.69	0.80	0.94	ns, Max
$T_{RCKO_DO_CASCOUT}$ and $T_{RCKO_DO_CASCOUT_REG}$	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.21	2.45	2.80	3.19	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	0.98	1.08	1.24	1.32	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.65	0.74	0.89	0.97	ns, Max
$T_{RCKO_POINTERS}$	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.79	0.87	0.98	1.10	ns, Max
$T_{RCKO_PARITY_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.93	ns, Max
$T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	4.15	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.89	ns, Max
$T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.98	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCK_ADDR}/T_{RCKC_ADDR}$	ADDR inputs ⁽⁸⁾	0.38/0.27	0.42/0.28	0.48/0.31	0.65/0.38	ns, Min
$T_{RDCK_DI_WF_NC}/T_{RCKD_DI_WF_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.49/0.51	0.55/0.53	0.63/0.57	0.78/0.64	ns, Min
$T_{RDCK_DI_RF}/T_{RCKD_DI_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.17/0.25	0.19/0.29	0.21/0.35	0.25/0.32	ns, Min
$T_{RDCK_DI_ECC}/T_{RCKD_DI_ECC}$	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.42/0.37	0.47/0.39	0.53/0.43	0.66/0.46	ns, Min
$T_{RDCK_DI_ECCW}/T_{RCKD_DI_ECCW}$	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.79/0.37	0.87/0.39	0.99/0.43	1.17/0.41	ns, Min
$T_{RDCK_DI_ECC_FIFO}/T_{RCKD_DI_ECC_FIFO}$	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.89/0.47	0.98/0.50	1.12/0.54	1.32/0.65	ns, Min
$T_{RCK_INJECTBITERR}/T_{RCKC_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	0.78/0.41	ns, Min
T_{RCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	0.48/0.22	ns, Min
$T_{RCK_REGCE}/T_{RCKC_REGCE}$	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	0.34/0.16	ns, Min
$T_{RCK_RSTREG}/T_{RCKC_RSTREG}$	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	0.35/0.06	ns, Min

Table 31: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCKK_RSTRAM}/T_{RCKC_RSTRAM}$	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	0.34/0.40	ns, Min
$T_{RCKK_WEA}/T_{RCKC_WEA}$	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	0.54/0.19	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	0.65/0.37	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	0.60/0.38	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers ⁽¹⁰⁾	0.76	0.83	0.93	1.06	ns, Max
$T_{RREC_RST}/T_{RREM_RST}$	FIFO reset recovery and removal timing ⁽¹¹⁾	1.59/–0.68	1.76/–0.68	2.01/–0.68	2.07/–0.60	ns, Max
Maximum Frequency						
$F_{MAX_BRAM_WF_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	372.44	MHz
$F_{MAX_BRAM_RF_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	372.44	MHz
$F_{MAX_BRAM_RF_DELAYED_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	317.36	MHz
$F_{MAX_CAS_WF_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	322.48	MHz
$F_{MAX_CAS_RF_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	322.48	MHz
$F_{MAX_CAS_RF_DELAYED_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.27	427.35	350.88	267.38	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	372.44	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	254.13	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- These parameters include both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F _{INMAX}	Maximum Input Clock Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F _{INMIN}	Minimum Input Clock Frequency	10.00	10.00	10.00	10.00	MHz
MMCM_F _{INJITTER}	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
MMCM_F _{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25.00	25.00	25.00	25.00	%
	Allowable Input Duty Cycle: 50—199 MHz	30.00	30.00	30.00	30.00	%
	Allowable Input Duty Cycle: 200—399 MHz	35.00	35.00	35.00	35.00	%
	Allowable Input Duty Cycle: 400—499 MHz	40.00	40.00	40.00	40.00	%
	Allowable Input Duty Cycle: >500 MHz	45.00	45.00	45.00	45.00	%
MMCM_F _{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO Frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO Frequency	1600.00	1440.00	1200.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM Bandwidth at Typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static Phase Offset of the MMCM Outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM Output Jitter	Note 3				
MMCM_T _{OUTDUTY}	MMCM Output Clock Duty Cycle Precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
MMCM_T _{LOCKMAX}	MMCM Maximum Lock Time	100.00	100.00	100.00	100.00	μs
MMCM_F _{OUTMAX}	MMCM Maximum Output Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM Minimum Output Frequency ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
MMCM_RST _{MINPULSE}	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550.00	500.00	450.00	450.00	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300.00	300.00	300.00	300.00	MHz
MMCM_F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10.00	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{MMCMDCK_DI} / T _{MMCMCKD_DI}	DI Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7K70T	4.98	5.49	6.17	7.04	ns
		XC7K160T	5.23	5.77	6.48	7.38	ns
		XC7K325T	5.72	6.31	7.09	8.07	ns
		XC7K355T	5.34	5.87	6.57	7.51	ns
		XC7K410T	5.84	6.44	7.22	8.21	ns
		XC7K420T	5.50	6.04	6.77	7.73	ns
		XC7K480T	5.50	6.04	6.77	7.73	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7K70T	5.29	5.83	6.55	7.47	ns
		XC7K160T	5.84	6.45	7.24	8.24	ns
		XC7K325T	6.33	6.99	7.84	8.92	ns
		XC7K355T	5.95	6.55	7.32	8.36	ns
		XC7K410T	6.45	7.12	7.97	9.07	ns
		XC7K420T	6.41	7.06	7.90	9.01	ns
		XC7K480T	6.41	7.06	7.90	9.01	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 42: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7K70T	0.95	0.95	0.95	1.74	ns
		XC7K160T	0.96	0.96	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 43: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFPLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7K70T	0.84	0.84	0.84	1.45	ns
		XC7K160T	0.89	0.89	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 44: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> BUFIO.						
T _{ICKOFCS}	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.90	ns

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) for further details.

Table 51: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

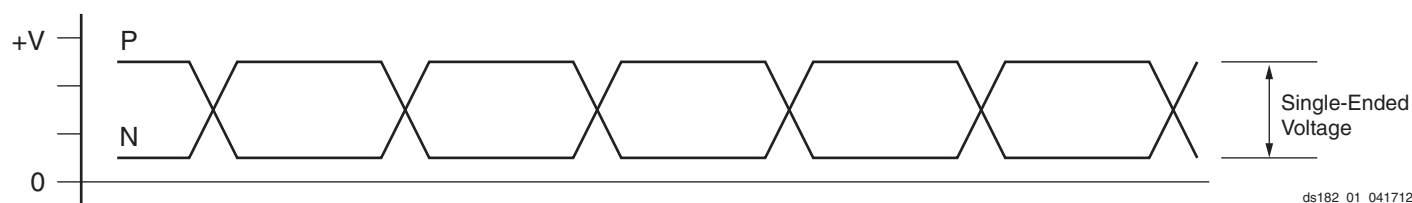


Figure 1: Single-Ended Peak-to-Peak Voltage

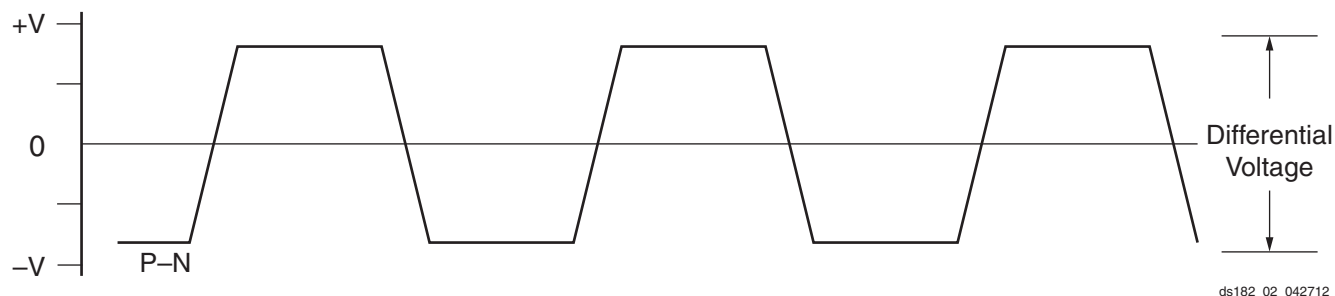


Figure 2: Differential Peak-to-Peak Voltage

Table 53: GTX Transceiver Performance (Cont'd)

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3	-2/-2L		-1 ⁽¹⁾		-2L ⁽²⁾			
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F _{GQPLL} RANGE2	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	125.00	MHz

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

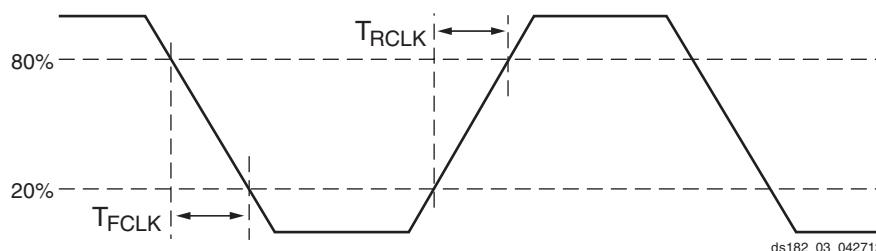


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL /Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x10 ⁶	UI

Table 57: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3 ⁽³⁾	-2/-2L ⁽³⁾	-1 ⁽⁴⁾	-2L ⁽⁵⁾	
F _{TXOUT}	TXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F _{RXOUT}	RXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz

Notes:

1. Clocking must be implemented as described in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2L (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	40	–	ps
T _{FTX}	TX Fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{12.5}	Total Jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
DJ _{12.5}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{11.18}	Total Jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
DJ _{11.18}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI

Table 68: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Master/Slave Serial Mode Programming Switching						
T _{DCC} /T _{CCKD}	DIN Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCC} /T _{SMCCKD}	D[31:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{SMWCC} /T _{SMCCKW}	RDWR_B Setup/Hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T _{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F _{RBCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup/Hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F _{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] Setup/Hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T _{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
T _{SPICCF}	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 69 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 69: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	—	—	115	mA
t_j	Temperature range	15	—	125	$^{\circ}\text{C}$

Notes:

1. The FPGA must not be configured during eFUSE programming.

Date	Version	Description
07/25/12	1.6	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 9. Updated parameters in Table 3. Added Table 4 and Table 5. Changed the typical values for many of the devices in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated speed specification to v1.06 (-3, -2, -2L(1.0V), -1) and v1.05 (-2L(0.9V)) with appropriate changes to Table 14 and Table 15 including production release of the XC7K325T and the XC7K410T in the -2, -2L(1.0V), and -1 speed designations. Added notes and specifications to Table 17 and Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 51 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 67 updated Note 1 and added Note 4. In Table 68, updated T_{POR} and F_{EMCCK}.
09/04/12	1.7	Updated Table 14 and Table 15 for production release of the XC7K160T in the -2, -2L(1.0V), and -1 speed designations.
09/26/12	1.8	In Table 2 , revised V_{CCINT} and V_{CCBRAM} and added Note 2 . Updated Table 14 and Table 15 for production release of the XC7K480T in the -2, -2L(1.0V), and -1 speed designations and the XC7K325T and XC7K410T in the -3 speed designation.
10/10/12	1.9	Updated the $I_{CCINTMIN}$ value for the XC7K355T in Table 7 . Updated Table 14 and Table 15 for production release of the XC7K420T in the -2, -2L(1.0V), and -1 speed designations.
10/25/12	2.0	Updated the AC Switching Characteristics based upon ISE 14.3 v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and ISE 14.3 v1.06 for the -2L (0.9V) speed specifications throughout the document. Updated Table 14 and Table 15 for production release of the XC7K355T in the -2, -2L(1.0V), and -1 speed designations. Also updated Table 14 and Table 15 for production release of the XC7K325T and XC7K410T in the -2L (0.9V). Added values for Table 16 -2L (0.9V). Added package skew values to Table 50. In Table 53, increased -1 speed grade (FF package) F_{GTMAX} value from 6.6 Gb/s to 8.0 Gb/s.
10/31/12	2.1	Updated Table 14 and Table 15 for production release of the XC7K70T in the -2, -2L(1.0V), and -1 speed designations.
11/26/12	2.2	Updated Table 14 and Table 15 for production release of -3 speed designation for XC7K70T, XC7K160T, XC7K355T, XC7K420T, and XC7K480T. Removed Note 4 from Table 67 .
12/05/12	2.3	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K160T, XC7K420T, and XC7K480T. Updated Note 1 in Table 50 .
12/12/12	2.4	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K70T and XC7K355T. Added Internal Configuration Access Port section to Table 68 .

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