AMD Xilinx - XC7K325T-2FBG900I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	25475
Number of Logic Elements/Cells	326080
Total RAM Bits	16404480
Number of I/O	500
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k325t-2fbg900i

Table 2: **Recommended Operating Conditions (1) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
$V_{MGTAVTTRCAL}$ (8)	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
8. Each voltage listed requires the filter circuit described in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide*.
9. For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V ±3% for lower power consumption.
10. For lower power consumption, $V_{MGTAVCC}$ should be 1.0V ±3% over the entire CPLL frequency range.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN} (2)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT} (3)	Battery supply current	–	–	150	nA

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.40	100	–0.40	100
V_{CCO} + 0.45	100	–0.45	61.7
V_{CCO} + 0.50	100	–0.50	25.8
V_{CCO} + 0.55	100	–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: **Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks[1][2]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.40	100	–0.40	100
V_{CCO} + 0.45	100	–0.45	100
V_{CCO} + 0.50	100	–0.50	100
V_{CCO} + 0.55	100	–0.55	100
V_{CCO} + 0.60	50.0	–0.60	50.0
V_{CCO} + 0.65	50.0	–0.65	50.0
V_{CCO} + 0.70	47.0	–0.70	50.0
V_{CCO} + 0.75	21.2	–0.75	50.0

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information.

Table 12: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information.

Table 13: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		1.710	1.800	1.890	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.300	1.200	1.425	V

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 15 lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 15: **Kintex-7 Device Production Software and Speed Specification Release**

Device	Speed Grade Designations			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7K70T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K160T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K325T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K355T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K410T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K420T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K480T	ISE 14.2 v1.06			ISE 14.3 v1.06

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 11. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 16: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.31	1.42	1.64	1.51	5.27	5.63	6.05	4.13	6.03	6.49	7.04	4.64	ns
LVTTL_S8	1.31	1.42	1.64	1.51	4.45	4.83	5.30	3.86	5.21	5.69	6.29	4.38	ns
LVTTL_S12	1.31	1.42	1.64	1.51	4.45	4.83	5.29	3.84	5.21	5.69	6.28	4.36	ns
LVTTL_S16	1.31	1.42	1.64	1.51	3.47	3.88	4.40	3.39	4.23	4.74	5.39	3.91	ns
LVTTL_S24	1.31	1.42	1.64	1.51	3.58	3.99	4.51	3.61	4.34	4.85	5.50	4.13	ns
LVTTL_F4	1.31	1.42	1.64	1.51	4.70	4.98	5.29	3.58	5.46	5.84	6.28	4.09	ns
LVTTL_F8	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.06	4.42	4.92	5.55	3.58	ns
LVTTL_F12	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.05	4.42	4.92	5.55	3.56	ns
LVTTL_F16	1.31	1.42	1.64	1.51	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVTTL_F24	1.31	1.42	1.64	1.51	2.41	2.64	2.89	2.94	3.17	3.50	3.88	3.45	ns
LVDS_25(1)	0.64	0.68	0.80	0.83	1.36	1.47	1.55	1.58	2.12	2.33	2.54	2.09	ns
MINI_LVDS_25	0.68	0.70	0.79	0.83	1.36	1.47	1.55	1.59	2.12	2.33	2.54	2.11	ns
BLVDS_25(1)	0.65	0.69	0.80	0.83	1.83	2.02	2.20	2.16	2.59	2.88	3.19	2.67	ns
RSDS_25 (point to point)(1)	0.63	0.68	0.79	0.83	1.36	1.48	1.55	1.59	2.12	2.34	2.54	2.11	ns
PPDS_25(1)	0.65	0.69	0.80	0.83	1.36	1.49	1.58	1.59	2.12	2.35	2.57	2.11	ns
TMDS_33(1)	0.72	0.76	0.86	0.83	1.43	1.54	1.60	1.70	2.19	2.40	2.59	2.22	ns
PCI33_3(1)	1.28	1.41	1.65	1.50	2.71	3.08	3.52	3.42	3.47	3.94	4.51	3.94	ns
HSUL_12	0.63	0.64	0.71	0.79	2.06	2.31	2.59	2.13	2.82	3.17	3.58	2.64	ns
DIFF_HSUL_12	0.58	0.61	0.70	0.81	1.83	2.04	2.26	1.92	2.59	2.90	3.25	2.44	ns
HSTL_I_S	0.61	0.64	0.73	0.79	1.55	1.69	1.80	1.91	2.31	2.55	2.79	2.42	ns
HSTL_II_S	0.61	0.64	0.73	0.78	1.21	1.34	1.43	1.70	1.97	2.20	2.42	2.22	ns
HSTL_I_18_S	0.64	0.67	0.76	0.79	1.28	1.39	1.45	1.58	2.04	2.25	2.44	2.09	ns
HSTL_II_18_S	0.64	0.67	0.76	0.79	1.18	1.31	1.40	1.69	1.94	2.17	2.39	2.20	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.78	1.42	1.54	1.61	1.84	2.18	2.40	2.60	2.36	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.79	1.15	1.24	1.27	1.78	1.91	2.10	2.26	2.30	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	0.79	1.27	1.38	1.43	1.67	2.03	2.24	2.42	2.19	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	0.81	1.14	1.23	1.26	1.72	1.90	2.09	2.25	2.23	ns

Table 19: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_I_F	0.61	0.64	0.73	0.79	1.10	1.19	1.23	1.41	1.86	2.05	2.22	1.92	ns
HSTL_II_F	0.61	0.64	0.73	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
HSTL_I_18_F	0.64	0.67	0.76	0.79	1.05	1.18	1.28	1.44	1.81	2.04	2.27	1.95	ns
HSTL_II_18_F	0.64	0.67	0.76	0.79	1.03	1.14	1.23	1.42	1.79	2.00	2.22	1.94	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	0.78	1.09	1.18	1.22	1.48	1.85	2.04	2.21	2.00	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	0.79	1.02	1.11	1.14	1.48	1.78	1.97	2.13	2.00	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	0.79	1.08	1.17	1.21	1.48	1.84	2.03	2.20	2.00	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	0.81	1.01	1.10	1.13	1.48	1.77	1.96	2.12	2.00	ns
LVCMOS33_S4	1.31	1.40	1.60	1.54	5.23	5.61	6.09	4.13	5.99	6.47	7.08	4.64	ns
LVCMOS33_S8	1.31	1.40	1.60	1.54	4.46	4.85	5.33	3.84	5.22	5.71	6.32	4.36	ns
LVCMOS33_S12	1.31	1.40	1.60	1.54	3.46	3.89	4.42	3.41	4.22	4.75	5.41	3.92	ns
LVCMOS33_S16	1.31	1.40	1.60	1.54	3.06	3.43	3.88	3.72	3.82	4.29	4.87	4.23	ns
LVCMOS33_F4	1.31	1.40	1.60	1.54	4.70	5.01	5.36	3.58	5.46	5.87	6.35	4.09	ns
LVCMOS33_F8	1.31	1.40	1.60	1.54	3.62	4.04	4.56	3.06	4.38	4.90	5.55	3.58	ns
LVCMOS33_F12	1.31	1.40	1.60	1.54	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVCMOS33_F16	1.31	1.40	1.60	1.54	2.44	2.69	2.96	2.88	3.20	3.55	3.95	3.39	ns
LVCMOS25_S4	1.08	1.16	1.32	1.36	4.49	4.80	5.16	3.44	5.25	5.66	6.15	3.95	ns
LVCMOS25_S8	1.08	1.16	1.32	1.36	3.66	4.04	4.49	3.20	4.42	4.90	5.48	3.72	ns
LVCMOS25_S12	1.08	1.16	1.32	1.36	2.77	3.10	3.49	2.80	3.53	3.96	4.48	3.31	ns
LVCMOS25_S16	1.08	1.16	1.32	1.36	3.24	3.62	4.09	3.14	4.00	4.48	5.08	3.66	ns
LVCMOS25_F4	1.08	1.16	1.32	1.36	3.96	4.31	4.72	3.06	4.72	5.17	5.71	3.58	ns
LVCMOS25_F8	1.08	1.16	1.32	1.36	2.43	2.87	3.42	2.50	3.19	3.73	4.41	3.02	ns
LVCMOS25_F12	1.08	1.16	1.32	1.36	2.23	2.63	3.13	2.48	2.99	3.49	4.12	3.00	ns
LVCMOS25_F16	1.08	1.16	1.32	1.36	1.92	2.17	2.45	2.33	2.68	3.03	3.44	2.84	ns
LVCMOS18_S4	0.64	0.66	0.74	0.87	3.24	3.45	3.66	1.91	4.00	4.31	4.65	2.42	ns
LVCMOS18_S8	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVCMOS18_S12	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVCMOS18_S16	0.64	0.66	0.74	0.87	1.82	2.03	2.24	1.84	2.58	2.89	3.23	2.36	ns
LVCMOS18_S24(1)	0.64	0.66	0.74	0.87	1.74	1.92	2.08	1.92	2.50	2.78	3.07	2.44	ns
LVCMOS18_F4	0.64	0.66	0.74	0.87	3.12	3.31	3.49	1.77	3.88	4.17	4.48	2.28	ns
LVCMOS18_F8	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVCMOS18_F12	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVCMOS18_F16	0.64	0.66	0.74	0.87	1.52	1.68	1.81	1.72	2.28	2.54	2.80	2.23	ns
LVCMOS18_F24(1)	0.64	0.66	0.74	0.87	1.34	1.46	1.55	1.66	2.10	2.32	2.54	2.17	ns
LVCMOS15_S4	0.66	0.69	0.81	0.90	3.48	3.74	4.03	2.22	4.24	4.60	5.02	2.73	ns
LVCMOS15_S8	0.66	0.69	0.81	0.90	2.37	2.67	3.01	2.41	3.13	3.53	4.00	2.92	ns
LVCMOS15_S12	0.66	0.69	0.81	0.90	1.83	2.03	2.23	1.91	2.59	2.89	3.22	2.42	ns

Table 19: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVCMOS15_S16	0.66	0.69	0.81	0.90	1.76	1.95	2.13	1.91	2.52	2.81	3.12	2.42	ns
LVCMOS15_F4	0.66	0.69	0.81	0.90	3.39	3.60	3.80	1.98	4.15	4.46	4.79	2.50	ns
LVCMOS15_F8	0.66	0.69	0.81	0.90	1.79	1.99	2.18	1.92	2.55	2.85	3.17	2.44	ns
LVCMOS15_F12	0.66	0.69	0.81	0.90	1.40	1.54	1.65	1.67	2.16	2.40	2.64	2.19	ns
LVCMOS15_F16	0.66	0.69	0.81	0.90	1.37	1.51	1.61	1.66	2.13	2.37	2.60	2.17	ns
LVCMOS12_S4	0.88	0.91	1.00	1.01	3.85	4.22	4.69	2.89	4.61	5.08	5.68	3.41	ns
LVCMOS12_S8	0.88	0.91	1.00	1.01	2.52	2.96	3.52	2.41	3.28	3.82	4.51	2.92	ns
LVCMOS12_S12(1)	0.88	0.91	1.00	1.01	2.06	2.31	2.59	2.11	2.82	3.17	3.58	2.63	ns
LVCMOS12_F4	0.88	0.91	1.00	1.01	3.44	3.73	4.06	2.30	4.20	4.59	5.05	2.81	ns
LVCMOS12_F8	0.88	0.91	1.00	1.01	1.72	2.04	2.40	1.86	2.48	2.90	3.39	2.38	ns
LVCMOS12_F12(1)	0.88	0.91	1.00	1.01	1.54	1.71	1.87	1.69	2.30	2.57	2.86	2.20	ns
SSTL135_S	0.61	0.64	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
SSTL15_S	0.61	0.64	0.73	0.73	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
SSTL18_I_S	0.64	0.67	0.76	0.79	1.59	1.74	1.85	1.95	2.35	2.60	2.84	2.47	ns
SSTL18_II_S	0.64	0.67	0.76	0.78	1.27	1.40	1.50	1.63	2.03	2.26	2.49	2.14	ns
DIFF_SSTL135_S	0.59	0.61	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
DIFF_SSTL15_S	0.63	0.67	0.77	0.79	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	0.79	1.50	1.63	1.72	1.95	2.26	2.49	2.71	2.47	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	0.79	1.13	1.22	1.25	1.66	1.89	2.08	2.24	2.17	ns
SSTL135_F	0.61	0.64	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
SSTL15_F	0.61	0.64	0.73	0.73	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
SSTL18_I_F	0.64	0.67	0.76	0.79	1.12	1.22	1.26	1.44	1.88	2.08	2.25	1.95	ns
SSTL18_II_F	0.64	0.67	0.76	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
DIFF_SSTL135_F	0.59	0.61	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
DIFF_SSTL15_F	0.63	0.67	0.77	0.79	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	0.79	1.10	1.19	1.23	1.52	1.86	2.05	2.22	2.03	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	0.79	1.02	1.10	1.14	1.50	1.78	1.96	2.13	2.02	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II _T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVCMOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVCMOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVCMOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVCMOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVCMOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVCMOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVCMOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVCMOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVCMOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVCMOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVCMOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVCMOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVCMOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVCMOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVCMOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVCMOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVCMOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVCMOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVCMOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVCMOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVCMOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVCMOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVCMOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVCMOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVCMOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVCMOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVCMOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVCMOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVCMOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVCMOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVCMOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

Table 21 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	0.62	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	2.17	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	1.86	ns

Table 31: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	0.34/0.40	ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	0.54/0.19	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	0.65/0.37	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	0.60/0.38	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.76	0.83	0.93	1.06	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing(11)	1.59/–0.68	1.76/–0.68	2.01/–0.68	2.07/–0.60	ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	372.44	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	372.44	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	317.36	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	322.48	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	322.48	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.27	427.35	350.88	267.38	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	372.44	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	254.13	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 45: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7K70T	2.83/–0.29	2.95/–0.29	3.15/–0.29	4.96/–0.33	ns
		XC7K160T	3.17/–0.35	3.29/–0.35	3.55/–0.35	5.54/–0.49	ns
		XC7K325T	2.83/–0.06	2.94/–0.06	3.15/–0.06	5.18/–0.14	ns
		XC7K355T	3.26/–0.32	3.41/–0.32	3.67/–0.32	5.84/–0.49	ns
		XC7K410T	3.43/–0.34	3.59/–0.34	3.88/–0.34	6.21/–0.54	ns
		XC7K420T	3.37/–0.27	3.48/–0.27	3.76/–0.27	6.00/–0.52	ns
		XC7K480T	3.37/–0.27	3.48/–0.27	3.76/–0.27	6.00/–0.52	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 46: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay clock-capable clock input and IFF(2) with MMCM	XC7K70T	2.39/–0.22	2.65/–0.22	2.94/–0.22	2.21/–0.44	ns
		XC7K160T	2.49/–0.20	2.77/–0.20	3.07/–0.20	2.38/–0.47	ns
		XC7K325T	2.55/–0.16	2.85/–0.16	3.14/–0.16	2.60/–0.47	ns
		XC7K355T	2.43/–0.16	2.73/–0.16	3.00/–0.16	2.47/–0.43	ns
		XC7K410T	2.55/–0.16	2.84/–0.16	3.14/–0.16	2.58/–0.47	ns
		XC7K420T	2.47/–0.09	2.73/–0.09	3.02/–0.09	2.40/–0.41	ns
		XC7K480T	2.47/–0.09	2.73/–0.09	3.02/–0.09	2.40/–0.41	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

Table 50: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7K70T	FBG484	108	ps
			FBG676	135	ps
		XC7K160T	FBG484	118	ps
			FBG676	136	ps
			FFG676	161	ps
		XC7K325T	FBG676	146	ps
			FFG676	154	ps
			FBG900	163	ps
			FFG900	161	ps
		XC7K355T	FFG901	149	ps
		XC7K410T	FBG676	165	ps
			FFG676	168	ps
			FBG900	151	ps
			FFG900	146	ps
		XC7K420T	FFG901	149	ps
			FFG1156	145	ps
		XC7K480T	FFG901	149	ps
			FFG1156	145	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 53: **GTX Transceiver Performance *(Cont'd)***

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1[1]		-2L[2]		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
$F_{GQPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	175.01	175.01	156.25	125.00	MHz

Table 55: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

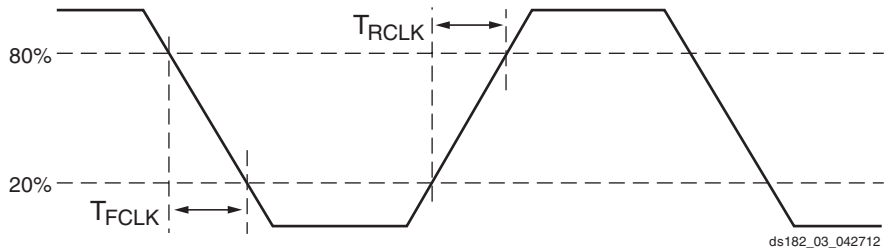

Figure 3: **Reference Clock Timing Parameters**

Table 56: **GTX Transceiver PLL /Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x10^6	UI

Table 57: **GTX Transceiver User Clock Switching Characteristics(1)(2)**

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3(3)	-2/-2L(3)	-1(4)	-2L(5)	
F_{TXOUT}	TXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz

Notes:

1. Clocking must be implemented as described in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide*.
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2L (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.500	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	40	–	ps
T_{FTX}	TX Fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{12.5}$	Total Jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$DJ_{12.5}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{11.18}$	Total Jitter(2)(4)	11.18 Gb/s	–	–	0.28	UI
$DJ_{11.18}$	Deterministic Jitter(2)(4)		–	–	0.17	UI

Table 59: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTXMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{12.5}$	Sinusoidal Jitter (QPLL)(3)	12.5 Gb/s	0.3	–	–	UI
$JT\_SJ_{11.18}$	Sinusoidal Jitter (QPLL)(3)	11.18 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32}$	Sinusoidal Jitter (QPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.95}$	Sinusoidal Jitter (QPLL)(3)	9.95 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.8}$	Sinusoidal Jitter (QPLL)(3)	9.8 Gb/s	0.3	–	–	UI
$JT\_SJ_{8.0}$	Sinusoidal Jitter (QPLL)(3)	8.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{6.6\_QPLL}$	Sinusoidal Jitter (QPLL)(3)	6.6 Gb/s	0.48	–	–	UI
$JT\_SJ_{6.6\_CPLL}$	Sinusoidal Jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter (CPLL)(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter (CPLL)(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal Jitter (CPLL)(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.6}$		6.6 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.6}$		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX and LPM or DFE mode.

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: **PCI Express Protocol Characteristics(1)**

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(3)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 63: **CEI-6G and CEI-11G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: **SFP+ Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 67: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference[5]						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for new BitGen option XADCEnhancedLinearity = ON.
3. See the ADC chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
4. See the Timing chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 68: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T_{PL}[1]	Program latency	5	5	5	5	ms, Max
T_{POR}[1]	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250	250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay	150	150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	70.00	MHz, Max

Table 68: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B Setup/Hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F_{RBCCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup/Hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO}(2)	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Master Flash Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] Setup/Hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T_{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
$T_{SPICCFC}$	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 69 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

Table 69: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.