



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	25475
Number of Logic Elements/Cells	326080
Total RAM Bits	16404480
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k325t-l2fbg676e

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than T_{VCCO2VCCAUX} for each power-on/off cycle to maintain device reliability levels.
- The T_{VCCO2VCCAUX} time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTVCCAUX}. Both V_{MGTAVCC} and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

- When V_{MGTAVTT} is powered before V_{MGTAVCC} and V_{MGTAVTT} - V_{MGTAVCC} > 150 mV and V_{MGTAVCC} < 0.7V, the V_{MGTAVTT} current draw can increase by 460 mA per transceiver during V_{MGTAVCC} ramp up. The duration of the current draw can be up to 0.3 x T_{MGTAVCC} (ramp time from GND to 90% of V_{MGTAVCC}). The reverse is true for power-down.
- When V_{MGTAVTT} is powered before V_{CCINT} and V_{MGTAVTT} - V_{CCINT} > 150 mV and V_{CCINT} < 0.7V, the V_{MGTAVTT} current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 10: Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$			$V_{OCM}^{(3)}$			$V_{OD}^{(4)}$		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	—	—	—	1.250	—	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO}-0.405$	$V_{CCO}-0.300$	$V_{CCO}-0.190$	0.400	0.600	0.800

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{OCM} is the output common mode voltage.
- V_{OD} is the output differential voltage ($Q - \bar{Q}$).
- V_{OD} for BLVDS will vary significantly depending on topology and loading.
- LVDS_25 is specified in Table 12.
- LVDS is specified in Table 13.

Table 11: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	8.00	-8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	8.00	-8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	16.00	-16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	16.00	-16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	—	20% V_{CCO}	80% V_{CCO}	0.100	-0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	—	10% V_{CCO}	90% V_{CCO}	0.100	-0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	14.25	-14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	-13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	-8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	-13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	-8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	-8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	-13.4

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{OL} is the single-ended low-output voltage.
- V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 12: LVDS_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		1.710	1.800	1.890	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.300	1.200	1.425	V

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 15](#) lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 15: Kintex-7 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7K70T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K160T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K325T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K355T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K410T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K420T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K480T	ISE 14.2 v1.06			ISE 14.3 v1.06

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 11](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 16: Networking Applications Interface Performances

Description	I/O Bank Type	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS receiver (SFI-4.2) ⁽¹⁾	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 17: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO}	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	2.0V	1866	1866	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	1066	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	800	800	800	Mb/s
RLDRAM III ⁽³⁾	HP	2.0V	800	667	667	533	MHz
	HP	1.8V	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+ ⁽⁴⁾	HP	2.0V	550	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
RLDRAM II	HP	2.0V	533	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
LPDDR2 ⁽³⁾	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), 7 Series FPGAs Memory Interface Solutions User Guide.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO} ⁽³⁾	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III ⁽⁴⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+ ⁽⁵⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2 ⁽⁴⁾	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), 7 Series FPGAs Memory Interface Solutions User Guide.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTTL_S4	1.31	1.42	1.64	1.51	5.27	5.63	6.05	4.13	6.03	6.49	7.04	4.64	ns
LVTTTL_S8	1.31	1.42	1.64	1.51	4.45	4.83	5.30	3.86	5.21	5.69	6.29	4.38	ns
LVTTTL_S12	1.31	1.42	1.64	1.51	4.45	4.83	5.29	3.84	5.21	5.69	6.28	4.36	ns
LVTTTL_S16	1.31	1.42	1.64	1.51	3.47	3.88	4.40	3.39	4.23	4.74	5.39	3.91	ns
LVTTTL_S24	1.31	1.42	1.64	1.51	3.58	3.99	4.51	3.61	4.34	4.85	5.50	4.13	ns
LVTTTL_F4	1.31	1.42	1.64	1.51	4.70	4.98	5.29	3.58	5.46	5.84	6.28	4.09	ns
LVTTTL_F8	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.06	4.42	4.92	5.55	3.58	ns
LVTTTL_F12	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.05	4.42	4.92	5.55	3.56	ns
LVTTTL_F16	1.31	1.42	1.64	1.51	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVTTTL_F24	1.31	1.42	1.64	1.51	2.41	2.64	2.89	2.94	3.17	3.50	3.88	3.45	ns
LVDS_25 ⁽¹⁾	0.64	0.68	0.80	0.83	1.36	1.47	1.55	1.58	2.12	2.33	2.54	2.09	ns
MINI_LVDS_25	0.68	0.70	0.79	0.83	1.36	1.47	1.55	1.59	2.12	2.33	2.54	2.11	ns
BLVDS_25 ⁽¹⁾	0.65	0.69	0.80	0.83	1.83	2.02	2.20	2.16	2.59	2.88	3.19	2.67	ns
RSDS_25 (point to point) ⁽¹⁾	0.63	0.68	0.79	0.83	1.36	1.48	1.55	1.59	2.12	2.34	2.54	2.11	ns
PPDS_25 ⁽¹⁾	0.65	0.69	0.80	0.83	1.36	1.49	1.58	1.59	2.12	2.35	2.57	2.11	ns
TMDS_33 ⁽¹⁾	0.72	0.76	0.86	0.83	1.43	1.54	1.60	1.70	2.19	2.40	2.59	2.22	ns
PCI33_3 ⁽¹⁾	1.28	1.41	1.65	1.50	2.71	3.08	3.52	3.42	3.47	3.94	4.51	3.94	ns
HSUL_12	0.63	0.64	0.71	0.79	2.06	2.31	2.59	2.13	2.82	3.17	3.58	2.64	ns
DIFF_HSUL_12	0.58	0.61	0.70	0.81	1.83	2.04	2.26	1.92	2.59	2.90	3.25	2.44	ns
HSTL_I_S	0.61	0.64	0.73	0.79	1.55	1.69	1.80	1.91	2.31	2.55	2.79	2.42	ns
HSTL_II_S	0.61	0.64	0.73	0.78	1.21	1.34	1.43	1.70	1.97	2.20	2.42	2.22	ns
HSTL_I_18_S	0.64	0.67	0.76	0.79	1.28	1.39	1.45	1.58	2.04	2.25	2.44	2.09	ns
HSTL_II_18_S	0.64	0.67	0.76	0.79	1.18	1.31	1.40	1.69	1.94	2.17	2.39	2.20	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.78	1.42	1.54	1.61	1.84	2.18	2.40	2.60	2.36	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.79	1.15	1.24	1.27	1.78	1.91	2.10	2.26	2.30	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	0.79	1.27	1.38	1.43	1.67	2.03	2.24	2.42	2.19	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	0.81	1.14	1.23	1.26	1.72	1.90	2.09	2.25	2.23	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS12_F8	0.64	0.67	0.78	0.95	1.27	1.42	1.55	1.41	1.91	2.18	2.37	2.02	ns
LVDCI_18	0.47	0.50	0.60	0.86	1.99	2.15	2.35	2.44	2.62	2.91	3.17	3.05	ns
LVDCI_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	2.40	2.62	2.99	3.40	3.01	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.87	1.99	2.15	2.34	1.86	2.62	2.90	3.17	2.48	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	1.83	2.62	2.99	3.40	2.44	ns
HSLVDCI_18	0.68	0.72	0.82	0.86	1.99	2.15	2.35	2.43	2.62	2.91	3.17	3.04	ns
HSLVDCI_15	0.68	0.72	0.82	0.84	1.98	2.23	2.58	2.27	2.62	2.99	3.40	2.88	ns
SSTL18_I_S	0.68	0.72	0.82	0.86	1.02	1.15	1.24	1.41	1.66	1.90	2.07	2.02	ns
SSTL18_II_S	0.68	0.72	0.82	0.87	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.76	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.78	0.88	0.98	1.08	1.26	1.51	1.74	1.90	1.87	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.78	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL15_S	0.68	0.72	0.82	0.81	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.78	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.80	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL135_S	0.69	0.72	0.82	0.89	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL12_S	0.69	0.72	0.82	0.95	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.89	1.02	1.15	1.24	1.43	1.66	1.90	2.07	2.04	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.89	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.75	0.88	0.98	1.08	1.33	1.51	1.74	1.90	1.94	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.89	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.75	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.76	0.94	1.06	1.15	1.38	1.57	1.82	1.97	1.99	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.91	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.43	1.60	1.85	2.01	2.04	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.91	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.78	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.80	1.03	1.17	1.27	1.41	1.66	1.92	2.09	2.02	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
SSTL18_I_F	0.68	0.72	0.82	0.86	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL18_II_F	0.68	0.72	0.82	0.87	0.97	1.09	1.16	1.36	1.61	1.84	1.99	1.98	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.76	0.89	1.02	1.10	1.30	1.53	1.77	1.92	1.91	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.24	1.53	1.77	1.92	1.85	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.27	1.53	1.77	1.92	1.88	ns
SSTL15_F	0.68	0.72	0.82	0.81	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.78	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.80	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL135_F	0.69	0.72	0.82	0.89	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL12_F	0.69	0.72	0.82	0.95	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.26	1.54	1.79	1.93	1.87	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.89	0.94	1.06	1.15	1.38	1.58	1.82	1.97	1.99	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.89	0.97	1.09	1.16	1.40	1.61	1.84	1.99	2.01	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.36	1.53	1.77	1.92	1.98	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.75	0.89	1.02	1.10	1.32	1.53	1.77	1.92	1.93	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.38	1.53	1.77	1.92	1.99	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.75	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.76	0.89	1.01	1.09	1.35	1.53	1.77	1.91	1.96	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.35	1.52	1.76	1.90	1.96	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.78	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.80	0.91	1.03	1.11	1.33	1.54	1.79	1.93	1.94	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	0.62	ns
$T_{IOIBUFDISABLE_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	2.17	ns
$T_{IOIBUFDISABLE_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	1.86	ns

Input/Output Logic Switching Characteristics

Table 22: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	0.56/−0.16	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	0.88/−0.30	ns
T _{IDOCKE2} /T _{IOCKDE2}	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
T _{IDOCKDE2} /T _{IOCKDDE2}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
T _{IDOCKE3} /T _{IOCKDE3}	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
T _{IDOCKDE3} /T _{IOCKDDE3}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
Combinatorial						
T _{IDIE2}	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.09	0.10	0.12	0.14	ns
T _{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.15	ns
T _{IDIE3}	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.09	0.10	0.12	0.14	ns
T _{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.15	ns
Sequential Delays						
T _{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.36	0.39	0.45	0.54	ns
T _{IDLODE2}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.55	ns
T _{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.36	0.39	0.45	0.54	ns
T _{IDLODE3}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.55	ns
T _{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	0.71	ns
T _{RQ_ILOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.32	ns
T _{GSRQ_ILOGICE2}	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
T _{RQ_ILOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.32	ns
T _{GSRQ_ILOGICE3}	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_ILOGICE2}	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.68	ns, Min
T _{RPW_ILOGICE3}	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.68	ns, Min

Input/Output Delay Switching Characteristics

Table 26: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.22	3.22	3.22	3.22	µs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.00 ⁽¹⁾	200.00	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00 ⁽¹⁾	300.00	300.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	52.00	52.00	52.00	52.00	ns
IDELAY/ODELAY						
T _{IDELAYRESOLUTION}	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT} and T _{ODELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX} / T _{ODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY/ODELAY	800.00	800.00	710.00	710.00	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin Setup/Hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	0.14/0.16	ns
T _{ODCCK_CE} / T _{ODCKC_CE}	CE pin Setup/Hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	0.28/0.06	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin Setup/Hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	0.10/0.23	ns
T _{ODCCK_INC} / T _{ODCKC_INC}	INC pin Setup/Hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	0.19/0.16	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin Setup/Hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	0.22/0.19	ns
T _{ODCCK_RST} / T _{ODCKC_RST}	RST pin Setup/Hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	0.32/0.11	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{ODDO_ODATAIN}	Propagation delay through ODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See TRACE report for actual values.

DSP48E1 Switching Characteristics

Table 32: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
T _{DSPDCK_A_AREG} /T _{DSPCKD_A_AREG}	A input to A register CLK	0.24/ 0.12	0.27/ 0.14	0.31/ 0.16	0.38/ 0.12	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.28/ 0.13	0.32/ 0.14	0.39/ 0.15	0.51/ 0.16	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.15/ 0.15	0.17/ 0.17	0.20/ 0.20	0.31/ 0.21	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.21/ 0.19	0.27/ 0.22	0.35/ 0.26	0.46/ 0.20	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.21/ 0.12	0.24/ 0.14	0.27/ 0.16	0.31/ 0.12	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.22/ 0.13	0.25/ 0.14	0.30/ 0.15	0.34/ 0.16	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
T _{DSPDCK_{A, B}_MREG_MULT} / T _{DSPCKD_B_MREG_MULT}	{A, B,} input to M register CLK using multiplier	2.04/ −0.01	2.34/ −0.01	2.79/ −0.01	3.66/ −0.06	ns
T _{DSPDCK_{A, B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.09/ −0.02	1.25/ −0.02	1.49/ −0.02	1.94/ −0.23	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
T _{DSPDCK_{A, B}_PREG_MULT} / T _{DSPCKD_{A, B}_PREG_MULT}	{A, B,} input to P register CLK using multiplier	3.41/ −0.24	3.90/ −0.24	4.64/ −0.24	5.89/ −0.41	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.33/ −0.62	3.81/ −0.62	4.53/ −0.62	5.70/ −1.42	ns
T _{DSPDCK_{A, B}_PREG} / T _{DSPCKD_{A, B}_PREG}	A or B input to P register CLK not using multiplier	1.47/ −0.24	1.68/ −0.24	2.00/ −0.24	2.37/ −0.41	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.30/ −0.22	1.49/ −0.22	1.78/ −0.22	2.11/ −0.36	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.12/ −0.13	1.28/ −0.13	1.52/ −0.13	1.81/ −0.21	ns
Setup and Hold Times of the CE Pins						
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.30/ 0.05	0.36/ 0.06	0.44/ 0.09	0.55/ 0.09	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.24/ 0.08	0.29/ 0.09	0.36/ 0.11	0.43/ 0.11	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.31/ −0.02	0.36/ −0.02	0.44/ −0.02	0.58/ 0.12	ns
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.26/ 0.15	0.29/ 0.17	0.33/ 0.20	0.39/ 0.25	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.31/ 0.01	0.36/ 0.01	0.45/ 0.01	0.54/ 0.00	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
T_DSPCKO_P_MREG	CLK MREG to P output	1.42	1.64	1.96	2.31	ns
T_DSPCKO_CARRYCASCOUT_MREG	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	2.65	ns
T_DSPCKO_P_ADREG_MULT	CLK ADREG to P output using multiplier	2.30	2.63	3.13	3.90	ns
T_DSPCKO_CARRYCASCOUT_ADREG_MULT	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	4.23	ns
Clock to Outs from Input Register Clock to Output Pins						
T_DSPCKO_P_AREG_MULT	CLK AREG to P output using multiplier	3.34	3.83	4.55	5.80	ns
T_DSPCKO_P_BREG	CLK BREG to P output not using multiplier	1.39	1.59	1.88	2.24	ns
T_DSPCKO_P_CREG	CLK CREG to P output not using multiplier	1.43	1.64	1.95	2.32	ns
T_DSPCKO_P_DREG_MULT	CLK DREG to P output using multiplier	3.32	3.80	4.51	5.74	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
T_DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	0.87	ns
T_DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	6.13	ns
T_DSPCKO_CARRYCASCOUT_BREG	CLK BREG to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	2.58	ns
T_DSPCKO_CARRYCASCOUT_DREG_MULT	CLK DREG to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	6.07	ns
T_DSPCKO_CARRYCASCOUT_CREG	CLK CREG to CARRYCASCOUT output	1.64	1.88	2.23	2.65	ns
Maximum Frequency						
F_MAX	With all registers used	741.84	650.20	547.95	429.37	MHz
F_MAX_PATDET	With pattern detector	627.35	549.75	463.61	365.90	MHz
F_MAX_MULT_NOMREG	Two register multiply without MREG	412.20	360.75	303.77	248.32	MHz
F_MAX_MULT_NOMREG_PATDET	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	225.73	MHz
F_MAX_PREADD_MULT_NOADREG	Without ADREG	468.82	408.66	342.70	263.44	MHz
F_MAX_PREADD_MULT_NOADREG_PATDET	Without ADREG with pattern detect	468.82	408.66	342.70	263.44	MHz
F_MAX_NOPIPELINEREG	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	177.15	MHz
F_MAX_NOPIPELINEREG_PATDET	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	165.32	MHz

Clock Buffers and Networks

Table 33: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$	CE pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
$T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$	S pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
$T_{BCKO_O}^{(2)}$	BUFGCTRL delay from I0/I1 to O	0.08	0.10	0.12	0.10	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	560.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKO_O} values.

Table 34: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	1.48	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	710.00	MHz

Table 35: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	1.06	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	0.57	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	0.93	ns
Maximum Frequency						
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	600.00	540.00	450.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F _{INMAX}	Maximum Input Clock Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F _{INMIN}	Minimum Input Clock Frequency	10.00	10.00	10.00	10.00	MHz
MMCM_F _{INJITTER}	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
MMCM_F _{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25.00	25.00	25.00	25.00	%
	Allowable Input Duty Cycle: 50—199 MHz	30.00	30.00	30.00	30.00	%
	Allowable Input Duty Cycle: 200—399 MHz	35.00	35.00	35.00	35.00	%
	Allowable Input Duty Cycle: 400—499 MHz	40.00	40.00	40.00	40.00	%
	Allowable Input Duty Cycle: >500 MHz	45.00	45.00	45.00	45.00	%
MMCM_F _{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO Frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO Frequency	1600.00	1440.00	1200.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM Bandwidth at Typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static Phase Offset of the MMCM Outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM Output Jitter	Note 3				
MMCM_T _{OUTDUTY}	MMCM Output Clock Duty Cycle Precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
MMCM_T _{LOCKMAX}	MMCM Maximum Lock Time	100.00	100.00	100.00	100.00	μs
MMCM_F _{OUTMAX}	MMCM Maximum Output Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM Minimum Output Frequency ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
MMCM_RST _{MINPULSE}	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550.00	500.00	450.00	450.00	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300.00	300.00	300.00	300.00	MHz
MMCM_F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10.00	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{MMCMDCK_DI} / T _{MMCMCKD_DI}	DI Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7K70T	4.98	5.49	6.17	7.04	ns
		XC7K160T	5.23	5.77	6.48	7.38	ns
		XC7K325T	5.72	6.31	7.09	8.07	ns
		XC7K355T	5.34	5.87	6.57	7.51	ns
		XC7K410T	5.84	6.44	7.22	8.21	ns
		XC7K420T	5.50	6.04	6.77	7.73	ns
		XC7K480T	5.50	6.04	6.77	7.73	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7K70T	5.29	5.83	6.55	7.47	ns
		XC7K160T	5.84	6.45	7.24	8.24	ns
		XC7K325T	6.33	6.99	7.84	8.92	ns
		XC7K355T	5.95	6.55	7.32	8.36	ns
		XC7K410T	6.45	7.12	7.97	9.07	ns
		XC7K420T	6.41	7.06	7.90	9.01	ns
		XC7K480T	6.41	7.06	7.90	9.01	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) for further details.

Table 51: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

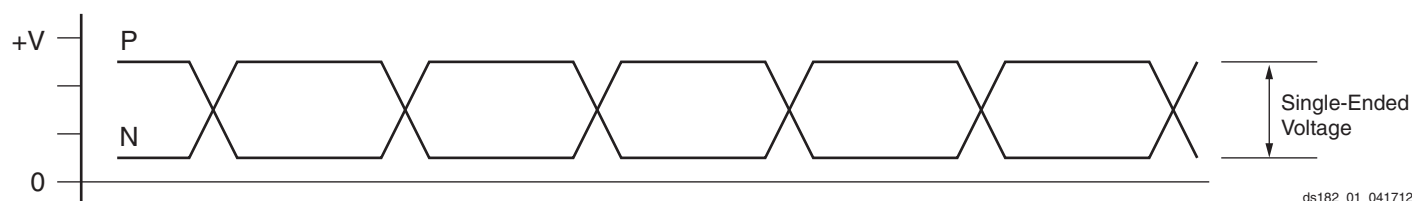


Figure 1: Single-Ended Peak-to-Peak Voltage

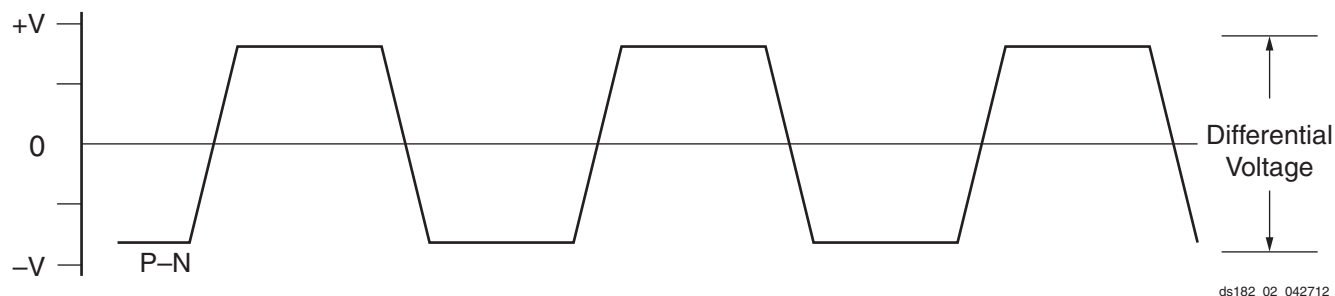


Figure 2: Differential Peak-to-Peak Voltage

Table 68: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Master/Slave Serial Mode Programming Switching						
T _{DCC} /T _{CCKD}	DIN Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCC} /T _{SMCCKD}	D[31:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{SMWCC} /T _{SMCCKW}	RDWR_B Setup/Hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T _{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F _{RBCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup/Hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F _{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] Setup/Hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T _{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
T _{SPICCF}	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

- To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 69 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 69: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	—	—	115	mA
t_j	Temperature range	15	—	125	$^{\circ}\text{C}$

Notes:

- The FPGA must not be configured during eFUSE programming.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials, or to advise you of any corrections or update. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.