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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	31775
Number of Logic Elements/Cells	406720
Total RAM Bits	29306880
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k410t-2fbg676i

Table 7 shows the minimum current, in addition to I_{CCQ} , that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

Table 7: Power-On Current for Kintex-7 Devices

Device	$I_{CCINTMIN}$ Typ ⁽¹⁾	$I_{CCAUXMIN}$ Typ ⁽¹⁾	I_{CCOMIN} Typ ⁽¹⁾	I_{CCAUX_IOMIN} Typ ⁽¹⁾	$I_{CCBRAMMIN}$ Typ ⁽¹⁾	Units
XC7K70T	$I_{CCINTQ} + 450$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K160T	$I_{CCINTQ} + 550$	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K325T	$I_{CCINTQ} + 600$	$I_{CCAUXQ} + 80$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K355T	$I_{CCINTQ} + 1450$	$I_{CCAUXQ} + 109$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 81$	mA
XC7K410T	$I_{CCINTQ} + 1500$	$I_{CCAUXQ} + 125$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 90$	mA
XC7K420T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA
XC7K480T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA

Notes:

- Typical values are specified at nominal voltage, 25°C.
- Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 8: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 12: LVDS_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		1.710	1.800	1.890	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.300	1.200	1.425	V

Table 17: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO}	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	2.0V	1866	1866	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	1066	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	800	800	800	Mb/s
RLDRAM III ⁽³⁾	HP	2.0V	800	667	667	533	MHz
	HP	1.8V	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+ ⁽⁴⁾	HP	2.0V	550	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
RLDRAM II	HP	2.0V	533	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
LPDDR2 ⁽³⁾	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), 7 Series FPGAs Memory Interface Solutions User Guide.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVDS	0.75	0.79	0.92	0.89	1.05	1.17	1.24	1.43	1.68	1.92	2.06	2.04	ns
HSUL_12	0.69	0.72	0.82	0.95	1.65	1.84	2.05	1.80	2.29	2.59	2.87	2.41	ns
DIFF_HSUL_12	0.69	0.72	0.82	0.92	1.65	1.84	2.05	1.47	2.29	2.59	2.87	2.08	ns
HSTL_I_S	0.68	0.72	0.82	0.84	1.15	1.28	1.38	1.46	1.79	2.03	2.20	2.07	ns
HSTL_II_S	0.68	0.72	0.82	0.84	1.05	1.17	1.26	1.44	1.69	1.93	2.08	2.05	ns
HSTL_I_18_S	0.70	0.72	0.82	0.86	1.12	1.24	1.34	1.41	1.75	2.00	2.16	2.02	ns
HSTL_II_18_S	0.70	0.72	0.82	0.86	1.06	1.18	1.26	1.44	1.70	1.94	2.08	2.05	ns
HSTL_I_12_S	0.68	0.72	0.82	0.94	1.14	1.27	1.37	1.43	1.78	2.02	2.20	2.04	ns
HSTL_I_DCI_S	0.68	0.72	0.82	0.78	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_S	0.68	0.72	0.82	0.78	1.05	1.17	1.26	1.33	1.69	1.93	2.08	1.94	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	0.76	1.15	1.28	1.38	1.40	1.78	2.03	2.20	2.01	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	0.76	1.05	1.16	1.24	1.32	1.69	1.92	2.06	1.93	ns
HSTL_II_T_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	0.89	1.15	1.28	1.38	1.47	1.79	2.03	2.20	2.08	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	0.89	1.05	1.17	1.26	1.47	1.69	1.93	2.08	2.08	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	0.76	1.15	1.28	1.38	1.47	1.78	2.03	2.20	2.08	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	0.76	1.05	1.17	1.26	1.40	1.69	1.93	2.08	2.01	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	0.89	1.12	1.24	1.34	1.46	1.75	2.00	2.16	2.07	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	0.89	1.06	1.18	1.26	1.47	1.70	1.94	2.08	2.08	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	0.75	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	0.75	1.05	1.16	1.24	1.41	1.69	1.92	2.06	2.02	ns
DIFF_HSTL_II_T_DCI_18_S	0.75	0.79	0.92	0.76	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
HSTL_I_F	0.68	0.72	0.82	0.84	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_II_F	0.68	0.72	0.82	0.84	0.97	1.08	1.15	1.29	1.61	1.84	1.97	1.90	ns
HSTL_I_18_F	0.70	0.72	0.82	0.86	1.04	1.16	1.24	1.32	1.68	1.91	2.06	1.93	ns
HSTL_II_18_F	0.70	0.72	0.82	0.86	0.98	1.09	1.16	1.35	1.62	1.85	1.98	1.96	ns
HSTL_I_12_F	0.68	0.72	0.82	0.94	1.02	1.13	1.21	1.26	1.65	1.88	2.03	1.87	ns
HSTL_I_DCI_F	0.68	0.72	0.82	0.78	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.78	0.97	1.08	1.15	1.22	1.61	1.84	1.97	1.83	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	0.76	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.76	0.98	1.09	1.16	1.27	1.61	1.85	1.98	1.88	ns
HSTL_II_T_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	0.89	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	0.89	0.97	1.08	1.15	1.35	1.61	1.84	1.97	1.96	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	0.76	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVC MOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVC MOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVC MOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVC MOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVC MOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVC MOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVC MOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVC MOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVC MOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVC MOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVC MOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVC MOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVC MOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVC MOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVC MOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVC MOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVC MOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVC MOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVC MOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVC MOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVC MOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVC MOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVC MOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVC MOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVC MOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVC MOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVC MOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVC MOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVC MOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVC MOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVC MOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS12_F8	0.64	0.67	0.78	0.95	1.27	1.42	1.55	1.41	1.91	2.18	2.37	2.02	ns
LVDCI_18	0.47	0.50	0.60	0.86	1.99	2.15	2.35	2.44	2.62	2.91	3.17	3.05	ns
LVDCI_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	2.40	2.62	2.99	3.40	3.01	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.87	1.99	2.15	2.34	1.86	2.62	2.90	3.17	2.48	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	1.83	2.62	2.99	3.40	2.44	ns
HSLVDCI_18	0.68	0.72	0.82	0.86	1.99	2.15	2.35	2.43	2.62	2.91	3.17	3.04	ns
HSLVDCI_15	0.68	0.72	0.82	0.84	1.98	2.23	2.58	2.27	2.62	2.99	3.40	2.88	ns
SSTL18_I_S	0.68	0.72	0.82	0.86	1.02	1.15	1.24	1.41	1.66	1.90	2.07	2.02	ns
SSTL18_II_S	0.68	0.72	0.82	0.87	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.76	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.78	0.88	0.98	1.08	1.26	1.51	1.74	1.90	1.87	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.78	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL15_S	0.68	0.72	0.82	0.81	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.78	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.80	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL135_S	0.69	0.72	0.82	0.89	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL12_S	0.69	0.72	0.82	0.95	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.89	1.02	1.15	1.24	1.43	1.66	1.90	2.07	2.04	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.89	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.75	0.88	0.98	1.08	1.33	1.51	1.74	1.90	1.94	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.89	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.75	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.76	0.94	1.06	1.15	1.38	1.57	1.82	1.97	1.99	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.91	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.43	1.60	1.85	2.01	2.04	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.91	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.78	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.80	1.03	1.17	1.27	1.41	1.66	1.92	2.09	2.02	ns

Input/Output Logic Switching Characteristics

Table 22: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	0.56/−0.16	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	0.88/−0.30	ns
T _{IDOCKE2} /T _{IOCKDE2}	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
T _{IDOCKDE2} /T _{IOCKDDE2}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
T _{IDOCKE3} /T _{IOCKDE3}	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
T _{IDOCKDE3} /T _{IOCKDDE3}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
Combinatorial						
T _{IDIE2}	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.09	0.10	0.12	0.14	ns
T _{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.15	ns
T _{IDIE3}	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.09	0.10	0.12	0.14	ns
T _{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.15	ns
Sequential Delays						
T _{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.36	0.39	0.45	0.54	ns
T _{IDLODE2}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.55	ns
T _{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.36	0.39	0.45	0.54	ns
T _{IDLODE3}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.55	ns
T _{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	0.71	ns
T _{RQ_ILOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.32	ns
T _{GSRQ_ILOGICE2}	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
T _{RQ_ILOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.32	ns
T _{GSRQ_ILOGICE3}	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_ILOGICE2}	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.68	ns, Min
T _{RPW_ILOGICE3}	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.68	ns, Min

Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/−0.13	0.50/−0.13	0.58/−0.13	0.79/−0.18	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/−0.10	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	0.62/−0.04	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.49/−0.16	0.56/−0.16	0.68/−0.16	0.67/−0.18	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/−0.10	ns
Combinatorial						
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	1.18	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	0.63	ns
T _{RQ_OLOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	1.12	ns
T _{GSRQ_OLOGICE2}	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
T _{RQ_OLOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	1.12	ns
T _{GSRQ_OLOGICE3}	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_OLOGICE2}	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	0.68	ns, Min
T _{RPW_OLOGICE3}	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	0.68	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.44/−0.24	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	0.67/−0.25	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input Setup/Hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	0.46/−0.25	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/−0.15	ns
T _{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.70	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/−0.15	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

CLB Switching Characteristics

Table 28: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	0.07	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	0.22	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	0.37	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	0.91	ns, Max
T _{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	0.62	ns, Max
T _{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	0.66	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	0.62	ns, Max
T _{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	0.67	ns, Max
T _{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	0.51	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	0.62	ns, Max
T _{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	0.43	ns, Max
T _{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	0.54	ns, Max
T _{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	0.52	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	0.40	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	0.46	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D Flip Flops	0.01/0.12	0.02/0.13	0.03/0.18	0.02/0.18	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D Flip Flops	0.04/0.14	0.04/0.14	0.05/0.20	0.05/0.21	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D Flip Flops	0.36/0.10	0.37/0.11	0.46/0.16	0.56/0.15	ns, Min
T _{CECK_CLB} /T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.19/0.05	0.20/0.05	0.25/0.05	0.24/0.04	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.30/0.05	0.31/0.07	0.37/0.09	0.48/0.05	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	0.59	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	0.54	ns, Max
F _{TOG}	Toggle frequency (for export control)	1818	1818	1818	1286	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{SHCKO}	Clock to A – B outputs	0.68	0.70	0.85	1.08	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	1.44	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	0.69/0.33	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	0.21/0.63	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	0.63/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	0.46/0.10	ns, Min
T _{CECK_LRAM} / T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	0.47/0.10	ns, Min
Clock CLK						
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	1.11	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	2.22	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	1.35	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	1.72	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	1.25	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	0.41/0.10	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	0.42/0.10	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	0.41/0.36	ns, Min
Clock CLK						
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.91	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Block RAM and FIFO Switching Characteristics

Table 31: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.57	1.80	2.08	2.44	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.54	0.63	0.75	0.86	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.35	2.58	3.26	4.49	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.62	0.69	0.80	0.94	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.21	2.45	2.80	3.19	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	0.98	1.08	1.24	1.32	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.65	0.74	0.89	0.97	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.79	0.87	0.98	1.10	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.93	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	4.15	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.89	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.98	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKCK_ADDRA} /T _{RCKC_ADDRA}	ADDR inputs ⁽⁸⁾	0.38/0.27	0.42/0.28	0.48/0.31	0.65/0.38	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.49/0.51	0.55/0.53	0.63/0.57	0.78/0.64	ns, Min
T _{RDCK_DI_RF} /T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.17/0.25	0.19/0.29	0.21/0.35	0.25/0.32	ns, Min
T _{RDCK_DI_ECC} / T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.42/0.37	0.47/0.39	0.53/0.43	0.66/0.46	ns, Min
T _{RDCK_DI_ECCW} / T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.79/0.37	0.87/0.39	0.99/0.43	1.17/0.41	ns, Min
T _{RDCK_DI_ECC_FIFO} / T _{RCKD_DI_ECC_FIFO}	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.89/0.47	0.98/0.50	1.12/0.54	1.32/0.65	ns, Min
T _{RCKCK_INJECTBITERR} / T _{RCKC_INJECTBITERR}	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	0.78/0.41	ns, Min
T _{RCKCK_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	0.48/0.22	ns, Min
T _{RCKCK_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	0.34/0.16	ns, Min
T _{RCKCK_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	0.35/0.06	ns, Min

DSP48E1 Switching Characteristics

Table 32: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
T _{DSPDCK_A_AREG} /T _{DSPCKD_A_AREG}	A input to A register CLK	0.24/ 0.12	0.27/ 0.14	0.31/ 0.16	0.38/ 0.12	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.28/ 0.13	0.32/ 0.14	0.39/ 0.15	0.51/ 0.16	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.15/ 0.15	0.17/ 0.17	0.20/ 0.20	0.31/ 0.21	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.21/ 0.19	0.27/ 0.22	0.35/ 0.26	0.46/ 0.20	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.21/ 0.12	0.24/ 0.14	0.27/ 0.16	0.31/ 0.12	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.22/ 0.13	0.25/ 0.14	0.30/ 0.15	0.34/ 0.16	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
T _{DSPDCK_{A, B}_MREG_MULT} / T _{DSPCKD_B_MREG_MULT}	{A, B,} input to M register CLK using multiplier	2.04/ −0.01	2.34/ −0.01	2.79/ −0.01	3.66/ −0.06	ns
T _{DSPDCK_{A, B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.09/ −0.02	1.25/ −0.02	1.49/ −0.02	1.94/ −0.23	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
T _{DSPDCK_{A, B}_PREG_MULT} / T _{DSPCKD_{A, B}_PREG_MULT}	{A, B,} input to P register CLK using multiplier	3.41/ −0.24	3.90/ −0.24	4.64/ −0.24	5.89/ −0.41	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.33/ −0.62	3.81/ −0.62	4.53/ −0.62	5.70/ −1.42	ns
T _{DSPDCK_{A, B}_PREG} / T _{DSPCKD_{A, B}_PREG}	A or B input to P register CLK not using multiplier	1.47/ −0.24	1.68/ −0.24	2.00/ −0.24	2.37/ −0.41	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.30/ −0.22	1.49/ −0.22	1.78/ −0.22	2.11/ −0.36	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.12/ −0.13	1.28/ −0.13	1.52/ −0.13	1.81/ −0.21	ns
Setup and Hold Times of the CE Pins						
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.30/ 0.05	0.36/ 0.06	0.44/ 0.09	0.55/ 0.09	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.24/ 0.08	0.29/ 0.09	0.36/ 0.11	0.43/ 0.11	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.31/ −0.02	0.36/ −0.02	0.44/ −0.02	0.58/ 0.12	ns
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.26/ 0.15	0.29/ 0.17	0.33/ 0.20	0.39/ 0.25	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.31/ 0.01	0.36/ 0.01	0.45/ 0.01	0.54/ 0.00	ns

Table 42: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7K70T	0.95	0.95	0.95	1.74	ns
		XC7K160T	0.96	0.96	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 43: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFPLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7K70T	0.84	0.84	0.84	1.45	ns
		XC7K160T	0.89	0.89	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 44: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> BUFIO.						
T _{ICKOFCS}	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.90	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 45: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7K70T	2.83/−0.29	2.95/−0.29	3.15/−0.29	4.96/−0.33	ns
		XC7K160T	3.17/−0.35	3.29/−0.35	3.55/−0.35	5.54/−0.49	ns
		XC7K325T	2.83/−0.06	2.94/−0.06	3.15/−0.06	5.18/−0.14	ns
		XC7K355T	3.26/−0.32	3.41/−0.32	3.67/−0.32	5.84/−0.49	ns
		XC7K410T	3.43/−0.34	3.59/−0.34	3.88/−0.34	6.21/−0.54	ns
		XC7K420T	3.37/−0.27	3.48/−0.27	3.76/−0.27	6.00/−0.52	ns
		XC7K480T	3.37/−0.27	3.48/−0.27	3.76/−0.27	6.00/−0.52	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 46: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7K70T	2.39/−0.22	2.65/−0.22	2.94/−0.22	2.21/−0.44	ns
		XC7K160T	2.49/−0.20	2.77/−0.20	3.07/−0.20	2.38/−0.47	ns
		XC7K325T	2.55/−0.16	2.85/−0.16	3.14/−0.16	2.60/−0.47	ns
		XC7K355T	2.43/−0.16	2.73/−0.16	3.00/−0.16	2.47/−0.43	ns
		XC7K410T	2.55/−0.16	2.84/−0.16	3.14/−0.16	2.58/−0.47	ns
		XC7K420T	2.47/−0.09	2.73/−0.09	3.02/−0.09	2.40/−0.41	ns
		XC7K480T	2.47/−0.09	2.73/−0.09	3.02/−0.09	2.40/−0.41	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

Table 50: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC7K70T	FBG484	108	ps
			FBG676	135	ps
		XC7K160T	FBG484	118	ps
			FBG676	136	ps
			FFG676	161	ps
		XC7K325T	FBG676	146	ps
			FFG676	154	ps
			FBG900	163	ps
			FFG900	161	ps
		XC7K355T	FFG901	149	ps
		XC7K410T	FBG676	165	ps
			FFG676	168	ps
			FBG900	151	ps
			FFG900	146	ps
		XC7K420T	FFG901	149	ps
			FFG1156	145	ps
		XC7K480T	FFG901	149	ps
			FFG1156	145	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) for further details.

Table 52: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) for further information.

Table 53: GTX Transceiver Performance

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1 ⁽¹⁾		-2L ⁽²⁾		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F _{GTXMAX} ⁽³⁾	Maximum GTX transceiver data rate		12.5	6.6	10.3125	6.6	8.0	6.6	6.6	6.6	Gb/s
F _{GTXMIN} ⁽³⁾	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
F _{GTXCRANGE}	CPLL line rate range	1	3.2–6.6								Gb/s
		2	1.6–3.3								Gb/s
		4	0.8–1.65								Gb/s
		8	0.5–0.825								Gb/s
		16	N/A								Gb/s
F _{GTXQRANGE1}	QPLL line rate range 1	1	5.93– 8.0	5.93– 6.6	5.93– 8.0	5.93– 6.6	5.93– 8.0	5.93– 6.6	5.93–6.6		Gb/s
		2	2.965–4.0		2.965–4.0		2.965–4.0		2.965–3.3		Gb/s
		4	1.4825–2.0		1.4825–2.0		1.4825–2.0		1.4825–1.65		Gb/s
		8	0.74125–1.0		0.74125–1.0		0.74125–1.0		0.74125–0.825		Gb/s
		16	N/A		N/A		N/A		N/A		Gb/s
F _{GTXQRANGE2}	QPLL line rate range 2 ⁽⁴⁾	1	9.8– 12.5	N/A	9.8– 10.3125	N/A	N/A		N/A		Gb/s
		2	4.9–6.25		4.9–5.15625		N/A		N/A		Gb/s
		4	2.45–3.125		2.45–2.578125		N/A		N/A		Gb/s
		8	1.225–1.5625		1.225–1.2890625		N/A		N/A		Gb/s
		16	0.6125–0.78125		0.6125– 0.64453125		N/A		N/A		Gb/s
F _{GCPLL} RANGE	GTX transceiver CPLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz
F _{GQPLL} RANGE1	GTX transceiver QPLL frequency range 1		5.93–8.0		5.93–8.0		5.93–8.0		5.93–6.6		GHz

Table 65: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 64.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 66: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

Revision History

The following table shows the revision history for this document:

Date	Version	Description
03/01/11	1.0	Initial Xilinx release.
04/01/11	1.1	Added the XC7K355T, XC7K420T, and XC7K480T devices throughout data sheet. Added the extended temperature range discussion to page 1 . Updated V_{CCAUX_IO} in Table 2 . Edits to clarify Power-On/Off Power Supply Sequencing power sequencing discussion. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7 . Updated $MMCM_F_{INDUTY}$ and added $F_{INJITTER}$, $T_{OUTJITTER}$, $T_{EXTFVAR}$, and Note 3 to Table 38 . Removed the SBG324 package from Table 50 . Updated the Notice of Disclaimer .
10/04/11	1.2	Replaced -1L with -2L throughout this data sheet. Updated Min/Max values and removed Note 5 from Table 2 . Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8 . Updated V_{ICM} in Table 12 and Table 13 . Added Note 1 to Table 12 . Updated Table 69 including adding Note 1 . Added <i>Absolute Maximum Ratings for GTX Transceivers</i> . Revised the reference clock maximum frequency (F_{GCLK}) in Table 55 . Added Table 57 . Added LVTTTL and removed SSTL135_II and SSTL15_II specifications from Table 19 . Removed HSTL_III from Table 20 . Removed the <i>I/O Standard Adjustment Measurement Methodology</i> section. Use IBIS for more accurate information and measurements. Updated $T_{DELAYPAT_JIT}$ in Table 26 . Added T_{AS}/T_{AH} to Table 28 . Added $T_{RDCK_DI_WF_NC}/T_{RCKD_DI_WF_NC}$ and $T_{RDCK_DI_RF}/T_{RCKD_DI_RF}$ to Table 31 . Completely updated Table 68 . Updated the AC Switching Characteristics in Table 19 , Table 20 , Table 21 , Table 22 , Table 23 , Table 24 , Table 26 through Table 38 , Table 40 through Table 37 , and Table 67 .
11/03/11	1.3	Revised the V_{OCM} specification in Table 12 . Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20 . Added $MMCM_T_{FBDELAY}$ while adding $MMCM_$ to the symbol names of a few specifications in Table 38 and PLL to the symbol names in Table 39 . In Table 40 through Table 47 , updated the pin-to-pin descriptions with the SSTL15 standard. Updated units in Table 49 .
02/13/12	1.4	Updated summary description on page 1 . In Table 2 , revised V_{CCO} for the 3.3V HR I/O banks and updated T_j . Added typical values to Table 3 . Updated the notes in Table 6 . Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8 . Rearranged Table 9 , added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11 . Revised the specifications in Table 12 and Table 13 . Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 67 . Revised DDR LVDS transmitter data width in Table 16 . Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 28 as they are no longer applicable. Updated specifications in Table 68 . Updated Note 1 in Table 37 . In the GTX Transceiver DC Input and Output Levels section: Revised V_{IN} , and added I_{DCIN} and I_{DCOUT} to Table 51 . Added Note 4 to Table 53 . In Table 55 , revised F_{GCLK} , removed T_{PHASE} , and added T_{DLOCK} . Revised specifications and added Note 2 to Table 57 . Added Table 58 and Table 59 along with GTX Transceiver Protocol Jitter Characteristics in Table 60 through Table 65 .
05/23/12	1.5	Reorganized entire data sheet including adding Table 44 and Table 48 . Updated T_{SOL} in Table 1 . Updated I_{BATT} and added R_{IN_TERM} to Table 3 . Added values to Table 6 and Table 7 . Updated Power-On/Off Power Supply Sequencing , page 6 with regards to GTX transceivers. Updated many parameters in Table 9 including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11 . Updated V_{OL} in Table 12 . Updated Table 16 and removed notes 2 and 3. Updated Table 17 . Updated the AC Switching Characteristics based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and -2L (0.9V) speed specifications throughout the document. In Table 31 , updated Reset Delays section including Note 10 and Note 11 . Added data for T_{LOCK} and T_{DLOCK} in Table 55 . Updated many of the XADC specifications in Table 67 and added Note 2 . Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 68 to Table 38 and Table 39 .

Date	Version	Description
07/25/12	1.6	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 9. Updated parameters in Table 3. Added Table 4 and Table 5. Changed the typical values for many of the devices in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated speed specification to v1.06 (-3, -2, -2L(1.0V), -1) and v1.05 (-2L(0.9V)) with appropriate changes to Table 14 and Table 15 including production release of the XC7K325T and the XC7K410T in the -2, -2L(1.0V), and -1 speed designations. Added notes and specifications to Table 17 and Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 51 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 67 updated Note 1 and added Note 4. In Table 68, updated T_{POR} and F_{EMCCK}.
09/04/12	1.7	Updated Table 14 and Table 15 for production release of the XC7K160T in the -2, -2L(1.0V), and -1 speed designations.
09/26/12	1.8	In Table 2 , revised V_{CCINT} and V_{CCBRAM} and added Note 2 . Updated Table 14 and Table 15 for production release of the XC7K480T in the -2, -2L(1.0V), and -1 speed designations and the XC7K325T and XC7K410T in the -3 speed designation.
10/10/12	1.9	Updated the $I_{CCINTMIN}$ value for the XC7K355T in Table 7 . Updated Table 14 and Table 15 for production release of the XC7K420T in the -2, -2L(1.0V), and -1 speed designations.
10/25/12	2.0	Updated the AC Switching Characteristics based upon ISE 14.3 v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and ISE 14.3 v1.06 for the -2L (0.9V) speed specifications throughout the document. Updated Table 14 and Table 15 for production release of the XC7K355T in the -2, -2L(1.0V), and -1 speed designations. Also updated Table 14 and Table 15 for production release of the XC7K325T and XC7K410T in the -2L (0.9V). Added values for Table 16 -2L (0.9V). Added package skew values to Table 50. In Table 53, increased -1 speed grade (FF package) F_{GTMAX} value from 6.6 Gb/s to 8.0 Gb/s.
10/31/12	2.1	Updated Table 14 and Table 15 for production release of the XC7K70T in the -2, -2L(1.0V), and -1 speed designations.
11/26/12	2.2	Updated Table 14 and Table 15 for production release of -3 speed designation for XC7K70T, XC7K160T, XC7K355T, XC7K420T, and XC7K480T. Removed Note 4 from Table 67 .
12/05/12	2.3	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K160T, XC7K420T, and XC7K480T. Updated Note 1 in Table 50 .
12/12/12	2.4	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K70T and XC7K355T. Added Internal Configuration Access Port section to Table 68 .