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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	31775
Number of Logic Elements/Cells	406720
Total RAM Bits	29306880
Number of I/O	500
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k410t-2fbg900c

Table 1: Absolute Maximum Ratings ⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
I_{DCIN}	DC input current for receiver input pins DC coupled $V_{MGTAVTT} = 1.2V$	–	14	mA
I_{DCOUT}	DC output current for transmitter pins DC coupled $V_{MGTAVTT} = 1.2V$	–	14	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies ⁽⁶⁾	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies ⁽⁶⁾	–	+260	°C
T_j	Maximum junction temperature ⁽⁶⁾	–	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to [UG471: 7 Series FPGAs SelectIO Resources User Guide](#).
- The maximum limit applied to DC and AC signals.
- For maximum undershoot and overshoot AC specifications, see [Table 4](#) and [Table 5](#).
- For soldering guidelines and thermal considerations, see [UG475: 7 Series FPGA Packaging and Pinout Specification](#).

Table 2: Recommended Operating Conditions ⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
$V_{CCINT}^{(2)}$	Internal supply voltage	0.97	1.00	1.03	V
	For -2L (0.9V) devices: internal supply voltage	0.87	0.90	0.93	V
$V_{CCBRAM}^{(2)}$	Block RAM supply voltage	0.97	1.00	1.03	V
	For -2L (0.9V) devices: block RAM supply voltage	0.87	0.90	1.03	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
$V_{CCO}^{(3)(4)}$	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
	Supply voltage for 1.8V HP I/O banks	1.14	–	1.89	V
V_{CCAUX_IO}	Auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	Auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
$V_{IN}^{(5)}$	I/O input voltage	–0.20	–	$V_{CCO} + 0.2$	V
	I/O input voltage for V_{REF} and differential I/O standards	–0.20	–	2.625	V
$I_{IN}^{(6)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
$V_{CCBATT}^{(7)}$	Battery voltage	1.0	–	1.89	V
GTX Transceiver					
$V_{MGTAVCC}^{(8)}$	Analog supply voltage for the GTX transceiver QPLL frequency range ≤ 10.3125 GHz ⁽⁹⁾⁽¹⁰⁾	0.97	1.0	1.08	V
	Analog supply voltage for the GTX transceiver QPLL frequency range > 10.3125 GHz	1.02	1.05	1.08	V
$V_{MGTAVTT}^{(8)}$	Analog supply voltage for the GTX transmitter and receiver termination circuits	1.17	1.2	1.23	V
$V_{MGTVCCAUX}^{(8)}$	Auxiliary analog QPLL voltage supply for the transceivers	1.75	1.80	1.85	V

Table 2: Recommended Operating Conditions ⁽¹⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
$V_{MGTAVTTRCAL}$ ⁽⁸⁾	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

- All voltages are relative to ground.
- V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .
- Each voltage listed requires the filter circuit described in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#).
- For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be $1.0V \pm 3\%$ for lower power consumption.
- For lower power consumption, $V_{MGTAVCC}$ should be $1.0V \pm 3\%$ over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	μA
C_{IN} ⁽²⁾	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$	90	–	330	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$	68	–	250	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	34	–	220	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	23	–	150	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	12	–	120	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3V$	68	–	330	μA
	Pad pull-down (when selected) @ $V_{IN} = 1.8V$	45	–	180	μA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT} ⁽³⁾	Battery supply current	–	–	150	nA

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
$R_{IN_TERM}^{(4)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	—	1.010	—	—
r	Temperature diode series resistance	—	2	—	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	61.7
$V_{CCO} + 0.50$	100	–0.50	25.8
$V_{CCO} + 0.55$	100	–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	100
$V_{CCO} + 0.50$	100	–0.50	100
$V_{CCO} + 0.55$	100	–0.55	100
$V_{CCO} + 0.60$	50.0	–0.60	50.0
$V_{CCO} + 0.65$	50.0	–0.65	50.0
$V_{CCO} + 0.70$	47.0	–0.70	50.0
$V_{CCO} + 0.75$	21.2	–0.75	50.0

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than T_{VCCO2VCCAUX} for each power-on/off cycle to maintain device reliability levels.
- The T_{VCCO2VCCAUX} time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTVCCAUX}. Both V_{MGTAVCC} and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

- When V_{MGTAVTT} is powered before V_{MGTAVCC} and V_{MGTAVTT} - V_{MGTAVCC} > 150 mV and V_{MGTAVCC} < 0.7V, the V_{MGTAVTT} current draw can increase by 460 mA per transceiver during V_{MGTAVCC} ramp up. The duration of the current draw can be up to 0.3 x T_{MGTAVCC} (ramp time from GND to 90% of V_{MGTAVCC}). The reverse is true for power-down.
- When V_{MGTAVTT} is powered before V_{CCINT} and V_{MGTAVTT} - V_{CCINT} > 150 mV and V_{CCINT} < 0.7V, the V_{MGTAVTT} current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTTL_S4	1.31	1.42	1.64	1.51	5.27	5.63	6.05	4.13	6.03	6.49	7.04	4.64	ns
LVTTTL_S8	1.31	1.42	1.64	1.51	4.45	4.83	5.30	3.86	5.21	5.69	6.29	4.38	ns
LVTTTL_S12	1.31	1.42	1.64	1.51	4.45	4.83	5.29	3.84	5.21	5.69	6.28	4.36	ns
LVTTTL_S16	1.31	1.42	1.64	1.51	3.47	3.88	4.40	3.39	4.23	4.74	5.39	3.91	ns
LVTTTL_S24	1.31	1.42	1.64	1.51	3.58	3.99	4.51	3.61	4.34	4.85	5.50	4.13	ns
LVTTTL_F4	1.31	1.42	1.64	1.51	4.70	4.98	5.29	3.58	5.46	5.84	6.28	4.09	ns
LVTTTL_F8	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.06	4.42	4.92	5.55	3.58	ns
LVTTTL_F12	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.05	4.42	4.92	5.55	3.56	ns
LVTTTL_F16	1.31	1.42	1.64	1.51	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVTTTL_F24	1.31	1.42	1.64	1.51	2.41	2.64	2.89	2.94	3.17	3.50	3.88	3.45	ns
LVDS_25 ⁽¹⁾	0.64	0.68	0.80	0.83	1.36	1.47	1.55	1.58	2.12	2.33	2.54	2.09	ns
MINI_LVDS_25	0.68	0.70	0.79	0.83	1.36	1.47	1.55	1.59	2.12	2.33	2.54	2.11	ns
BLVDS_25 ⁽¹⁾	0.65	0.69	0.80	0.83	1.83	2.02	2.20	2.16	2.59	2.88	3.19	2.67	ns
RSDS_25 (point to point) ⁽¹⁾	0.63	0.68	0.79	0.83	1.36	1.48	1.55	1.59	2.12	2.34	2.54	2.11	ns
PPDS_25 ⁽¹⁾	0.65	0.69	0.80	0.83	1.36	1.49	1.58	1.59	2.12	2.35	2.57	2.11	ns
TMDS_33 ⁽¹⁾	0.72	0.76	0.86	0.83	1.43	1.54	1.60	1.70	2.19	2.40	2.59	2.22	ns
PCI33_3 ⁽¹⁾	1.28	1.41	1.65	1.50	2.71	3.08	3.52	3.42	3.47	3.94	4.51	3.94	ns
HSUL_12	0.63	0.64	0.71	0.79	2.06	2.31	2.59	2.13	2.82	3.17	3.58	2.64	ns
DIFF_HSUL_12	0.58	0.61	0.70	0.81	1.83	2.04	2.26	1.92	2.59	2.90	3.25	2.44	ns
HSTL_I_S	0.61	0.64	0.73	0.79	1.55	1.69	1.80	1.91	2.31	2.55	2.79	2.42	ns
HSTL_II_S	0.61	0.64	0.73	0.78	1.21	1.34	1.43	1.70	1.97	2.20	2.42	2.22	ns
HSTL_I_18_S	0.64	0.67	0.76	0.79	1.28	1.39	1.45	1.58	2.04	2.25	2.44	2.09	ns
HSTL_II_18_S	0.64	0.67	0.76	0.79	1.18	1.31	1.40	1.69	1.94	2.17	2.39	2.20	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.78	1.42	1.54	1.61	1.84	2.18	2.40	2.60	2.36	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.79	1.15	1.24	1.27	1.78	1.91	2.10	2.26	2.30	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	0.79	1.27	1.38	1.43	1.67	2.03	2.24	2.42	2.19	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	0.81	1.14	1.23	1.26	1.72	1.90	2.09	2.25	2.23	ns

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPi}				T _{IOPp}				T _{IOTp}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS15_S16	0.66	0.69	0.81	0.90	1.76	1.95	2.13	1.91	2.52	2.81	3.12	2.42	ns
LVC MOS15_F4	0.66	0.69	0.81	0.90	3.39	3.60	3.80	1.98	4.15	4.46	4.79	2.50	ns
LVC MOS15_F8	0.66	0.69	0.81	0.90	1.79	1.99	2.18	1.92	2.55	2.85	3.17	2.44	ns
LVC MOS15_F12	0.66	0.69	0.81	0.90	1.40	1.54	1.65	1.67	2.16	2.40	2.64	2.19	ns
LVC MOS15_F16	0.66	0.69	0.81	0.90	1.37	1.51	1.61	1.66	2.13	2.37	2.60	2.17	ns
LVC MOS12_S4	0.88	0.91	1.00	1.01	3.85	4.22	4.69	2.89	4.61	5.08	5.68	3.41	ns
LVC MOS12_S8	0.88	0.91	1.00	1.01	2.52	2.96	3.52	2.41	3.28	3.82	4.51	2.92	ns
LVC MOS12_S12 ⁽¹⁾	0.88	0.91	1.00	1.01	2.06	2.31	2.59	2.11	2.82	3.17	3.58	2.63	ns
LVC MOS12_F4	0.88	0.91	1.00	1.01	3.44	3.73	4.06	2.30	4.20	4.59	5.05	2.81	ns
LVC MOS12_F8	0.88	0.91	1.00	1.01	1.72	2.04	2.40	1.86	2.48	2.90	3.39	2.38	ns
LVC MOS12_F12 ⁽¹⁾	0.88	0.91	1.00	1.01	1.54	1.71	1.87	1.69	2.30	2.57	2.86	2.20	ns
SSTL135_S	0.61	0.64	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
SSTL15_S	0.61	0.64	0.73	0.73	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
SSTL18_I_S	0.64	0.67	0.76	0.79	1.59	1.74	1.85	1.95	2.35	2.60	2.84	2.47	ns
SSTL18_II_S	0.64	0.67	0.76	0.78	1.27	1.40	1.50	1.63	2.03	2.26	2.49	2.14	ns
DIFF_SSTL135_S	0.59	0.61	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
DIFF_SSTL15_S	0.63	0.67	0.77	0.79	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	0.79	1.50	1.63	1.72	1.95	2.26	2.49	2.71	2.47	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	0.79	1.13	1.22	1.25	1.66	1.89	2.08	2.24	2.17	ns
SSTL135_F	0.61	0.64	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
SSTL15_F	0.61	0.64	0.73	0.73	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
SSTL18_I_F	0.64	0.67	0.76	0.79	1.12	1.22	1.26	1.44	1.88	2.08	2.25	1.95	ns
SSTL18_II_F	0.64	0.67	0.76	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
DIFF_SSTL135_F	0.59	0.61	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
DIFF_SSTL15_F	0.63	0.67	0.77	0.79	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	0.79	1.10	1.19	1.23	1.52	1.86	2.05	2.22	2.03	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	0.79	1.02	1.10	1.14	1.50	1.78	1.96	2.13	2.02	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVC MOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVC MOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVC MOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVC MOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVC MOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVC MOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVC MOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVC MOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVC MOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVC MOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVC MOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVC MOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVC MOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVC MOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVC MOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVC MOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVC MOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVC MOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVC MOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVC MOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVC MOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVC MOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVC MOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVC MOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVC MOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVC MOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVC MOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVC MOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVC MOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVC MOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVC MOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
T _{ISCK_BITSLIP} / T _{ISCKC_BITSLIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	0.02/0.21	ns
T _{ISCK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	0.51/−0.22	ns
T _{ISCK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	−0.17/0.40	ns
Setup/Hold for Data Lines						
T _{ISDCK_D} /T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.03/0.19	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	0.19/0.19	ns
Sequential Delays						
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	0.67	ns
Propagation Delays						
T _{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	0.14	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.44/−0.24	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	0.67/−0.25	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input Setup/Hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	0.46/−0.25	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/−0.15	ns
T _{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.70	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/−0.15	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	0.81	ns
T _{CKO_FLAGS}	Clock to IO_FIFO Flags	0.59	0.62	0.81	0.77	ns
Setup/Hold						
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	0.76/−0.05	ns
T _{IFFCKC_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	0.70/−0.05	ns
T _{OFFCKC_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	0.79/−0.02	ns
Minimum Pulse Width						
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
Maximum Frequency						
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	333.33	MHz

CLB Switching Characteristics

Table 28: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	0.07	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	0.22	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	0.37	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	0.91	ns, Max
T _{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	0.62	ns, Max
T _{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	0.66	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	0.62	ns, Max
T _{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	0.67	ns, Max
T _{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	0.51	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	0.62	ns, Max
T _{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	0.43	ns, Max
T _{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	0.54	ns, Max
T _{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	0.52	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	0.40	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	0.46	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D Flip Flops	0.01/0.12	0.02/0.13	0.03/0.18	0.02/0.18	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D Flip Flops	0.04/0.14	0.04/0.14	0.05/0.20	0.05/0.21	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D Flip Flops	0.36/0.10	0.37/0.11	0.46/0.16	0.56/0.15	ns, Min
T _{CECK_CLB} /T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.19/0.05	0.20/0.05	0.25/0.05	0.24/0.04	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.30/0.05	0.31/0.07	0.37/0.09	0.48/0.05	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	0.59	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	0.54	ns, Max
F _{TOG}	Toggle frequency (for export control)	1818	1818	1818	1286	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{SHCKO}	Clock to A – B outputs	0.68	0.70	0.85	1.08	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	1.44	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	0.69/0.33	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	0.21/0.63	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	0.63/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	0.46/0.10	ns, Min
T _{CECK_LRAM} / T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	0.47/0.10	ns, Min
Clock CLK						
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	1.11	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	2.22	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	1.35	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	1.72	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	1.25	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	0.41/0.10	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	0.42/0.10	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	0.41/0.36	ns, Min
Clock CLK						
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.91	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 31: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCKK_RSTRAM}/T_{RCKC_RSTRAM}$	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	0.34/0.40	ns, Min
$T_{RCKK_WEA}/T_{RCKC_WEA}$	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	0.54/0.19	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	0.65/0.37	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	0.60/0.38	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers ⁽¹⁰⁾	0.76	0.83	0.93	1.06	ns, Max
$T_{RREC_RST}/T_{RREM_RST}$	FIFO reset recovery and removal timing ⁽¹¹⁾	1.59/–0.68	1.76/–0.68	2.01/–0.68	2.07/–0.60	ns, Max
Maximum Frequency						
$F_{MAX_BRAM_WF_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	372.44	MHz
$F_{MAX_BRAM_RF_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	372.44	MHz
$F_{MAX_BRAM_RF_DELAYED_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	317.36	MHz
$F_{MAX_CAS_WF_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	322.48	MHz
$F_{MAX_CAS_RF_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	322.48	MHz
$F_{MAX_CAS_RF_DELAYED_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.27	427.35	350.88	267.38	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	372.44	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	254.13	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- These parameters include both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 39: PLL Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550.00	500.00	450.00	450.00	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300.00	300.00	300.00	300.00	MHz
PLL_F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLCKC_DADDR} / T _{PLLCKC_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKC_DI} / T _{PLLCKC_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKC_DEN} / T _{PLLCKC_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLCKC_DWE} / T _{PLLCKC_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Table 42: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7K70T	0.95	0.95	0.95	1.74	ns
		XC7K160T	0.96	0.96	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 43: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFPLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7K70T	0.84	0.84	0.84	1.45	ns
		XC7K160T	0.89	0.89	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 44: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> BUFIO.						
T _{ICKOFCS}	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.90	ns

Table 47: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSPLLCC} / T _{PHPLLCC}	No Delay clock-capable clock input and IFF ⁽²⁾ with PLL	XC7K70T	2.75/−0.32	3.04/−0.32	3.33/−0.32	2.42/−0.54	ns
		XC7K160T	2.85/−0.31	3.16/−0.31	3.46/−0.31	2.59/−0.56	ns
		XC7K325T	2.91/−0.27	3.24/−0.27	3.54/−0.27	2.80/−0.56	ns
		XC7K355T	2.79/−0.27	3.12/−0.27	3.40/−0.27	2.67/−0.52	ns
		XC7K410T	2.91/−0.27	3.24/−0.27	3.53/−0.27	2.78/−0.56	ns
		XC7K420T	2.83/−0.20	3.12/−0.20	3.41/−0.20	2.61/−0.50	ns
		XC7K480T	2.83/−0.20	3.12/−0.20	3.41/−0.20	2.61/−0.50	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T _{PSCS} /T _{PHCS}	Setup/Hold of I/O clock for HR I/O banks	−0.36/1.36	−0.36/1.50	−0.36/1.70	−0.44/1.87	ns
	Setup/Hold of I/O clock for HP I/O banks	−0.34/1.39	−0.34/1.53	−0.34/1.73	−0.44/1.87	ns

Table 49: Sample Window

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T _{SAMP}	Sampling Error at Receiver Pins ⁽¹⁾	0.51	0.56	0.61	0.56	ns
T _{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO ⁽²⁾	0.30	0.35	0.40	0.35	ns

Notes:

- This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

Table 50: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC7K70T	FBG484	108	ps
			FBG676	135	ps
		XC7K160T	FBG484	118	ps
			FBG676	136	ps
			FFG676	161	ps
		XC7K325T	FBG676	146	ps
			FFG676	154	ps
			FBG900	163	ps
			FFG900	161	ps
		XC7K355T	FFG901	149	ps
		XC7K410T	FBG676	165	ps
			FFG676	168	ps
			FBG900	151	ps
			FFG900	146	ps
		XC7K420T	FFG901	149	ps
			FFG1156	145	ps
		XC7K480T	FFG901	149	ps
			FFG1156	145	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 58: GTX Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{10.3125}	Total Jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
DJ _{10.3125}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.953}	Total Jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
DJ _{9.953}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.8}	Total Jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	–	–	0.28	UI
DJ _{9.8}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{8.0}	Total Jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–	0.30	UI
DJ _{8.0}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.15	UI
TJ _{6.6_QPLL}	Total Jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	–	–	0.28	UI
DJ _{6.6_QPLL}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{6.6_CPLL}	Total Jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6_CPLL}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{5.0}	Total Jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{4.25}	Total Jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.75}	Total Jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.2}	Total Jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.2	UI
DJ _{3.2}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.1	UI
TJ _{3.2L}	Total Jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–	0.32	UI
DJ _{3.2L}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
TJ _{2.5}	Total Jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
TJ _{1.25}	Total Jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
TJ ₅₀₀	Total Jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.1	UI
DJ ₅₀₀	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of $1e^{-12}$.
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

XADC Specifications

Table 67: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C.	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 67: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference⁽⁵⁾						
External Reference	V _{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V _{REFP} pin to AGND, T _j = -40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for new BitGen option XADCEnhancedLinearity = ON.
- See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 68: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency	5	5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width	250	250	250	250	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay	150	150	150	150	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F _{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T _{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F _{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
Internal Configuration Access Port						
F _{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	70.00	MHz, Max