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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	31775
Number of Logic Elements/Cells	406720
Total RAM Bits	29306880
Number of I/O	500
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k410t-2ffg900c

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than T_{VCCO2VCCAUX} for each power-on/off cycle to maintain device reliability levels.
- The T_{VCCO2VCCAUX} time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, V_{MGTAVCC}, V_{MGTAVTT} OR V_{MGTAVCC}, V_{CCINT}, V_{MGTAVTT}. There is no recommended sequencing for V_{MGTVCCAUX}. Both V_{MGTAVCC} and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from V_{MGTAVTT} can be higher than specifications during power-up and power-down.

- When V_{MGTAVTT} is powered before V_{MGTAVCC} and V_{MGTAVTT} - V_{MGTAVCC} > 150 mV and V_{MGTAVCC} < 0.7V, the V_{MGTAVTT} current draw can increase by 460 mA per transceiver during V_{MGTAVCC} ramp up. The duration of the current draw can be up to 0.3 x T_{MGTAVCC} (ramp time from GND to 90% of V_{MGTAVCC}). The reverse is true for power-down.
- When V_{MGTAVTT} is powered before V_{CCINT} and V_{MGTAVTT} - V_{CCINT} > 150 mV and V_{CCINT} < 0.7V, the V_{MGTAVTT} current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 15](#) lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 15: Kintex-7 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7K70T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K160T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K325T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K355T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K410T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K420T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K480T	ISE 14.2 v1.06			ISE 14.3 v1.06

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 11](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 16: Networking Applications Interface Performances

Description	I/O Bank Type	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS receiver (SFI-4.2) ⁽¹⁾	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO} ⁽³⁾	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III ⁽⁴⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+ ⁽⁵⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2 ⁽⁴⁾	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDR II+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS15_S16	0.66	0.69	0.81	0.90	1.76	1.95	2.13	1.91	2.52	2.81	3.12	2.42	ns
LVC MOS15_F4	0.66	0.69	0.81	0.90	3.39	3.60	3.80	1.98	4.15	4.46	4.79	2.50	ns
LVC MOS15_F8	0.66	0.69	0.81	0.90	1.79	1.99	2.18	1.92	2.55	2.85	3.17	2.44	ns
LVC MOS15_F12	0.66	0.69	0.81	0.90	1.40	1.54	1.65	1.67	2.16	2.40	2.64	2.19	ns
LVC MOS15_F16	0.66	0.69	0.81	0.90	1.37	1.51	1.61	1.66	2.13	2.37	2.60	2.17	ns
LVC MOS12_S4	0.88	0.91	1.00	1.01	3.85	4.22	4.69	2.89	4.61	5.08	5.68	3.41	ns
LVC MOS12_S8	0.88	0.91	1.00	1.01	2.52	2.96	3.52	2.41	3.28	3.82	4.51	2.92	ns
LVC MOS12_S12 ⁽¹⁾	0.88	0.91	1.00	1.01	2.06	2.31	2.59	2.11	2.82	3.17	3.58	2.63	ns
LVC MOS12_F4	0.88	0.91	1.00	1.01	3.44	3.73	4.06	2.30	4.20	4.59	5.05	2.81	ns
LVC MOS12_F8	0.88	0.91	1.00	1.01	1.72	2.04	2.40	1.86	2.48	2.90	3.39	2.38	ns
LVC MOS12_F12 ⁽¹⁾	0.88	0.91	1.00	1.01	1.54	1.71	1.87	1.69	2.30	2.57	2.86	2.20	ns
SSTL135_S	0.61	0.64	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
SSTL15_S	0.61	0.64	0.73	0.73	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
SSTL18_I_S	0.64	0.67	0.76	0.79	1.59	1.74	1.85	1.95	2.35	2.60	2.84	2.47	ns
SSTL18_II_S	0.64	0.67	0.76	0.78	1.27	1.40	1.50	1.63	2.03	2.26	2.49	2.14	ns
DIFF_SSTL135_S	0.59	0.61	0.73	0.79	1.27	1.40	1.50	1.64	2.03	2.26	2.49	2.16	ns
DIFF_SSTL15_S	0.63	0.67	0.77	0.79	1.24	1.37	1.47	1.59	2.00	2.23	2.46	2.11	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	0.79	1.50	1.63	1.72	1.95	2.26	2.49	2.71	2.47	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	0.79	1.13	1.22	1.25	1.66	1.89	2.08	2.24	2.17	ns
SSTL135_F	0.61	0.64	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
SSTL15_F	0.61	0.64	0.73	0.73	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
SSTL18_I_F	0.64	0.67	0.76	0.79	1.12	1.22	1.26	1.44	1.88	2.08	2.25	1.95	ns
SSTL18_II_F	0.64	0.67	0.76	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
DIFF_SSTL135_F	0.59	0.61	0.73	0.79	1.04	1.17	1.26	1.42	1.80	2.03	2.25	1.94	ns
DIFF_SSTL15_F	0.63	0.67	0.77	0.79	1.04	1.17	1.26	1.39	1.80	2.03	2.25	1.91	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	0.79	1.10	1.19	1.23	1.52	1.86	2.05	2.22	2.03	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	0.79	1.02	1.10	1.14	1.50	1.78	1.96	2.13	2.02	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVDS	0.75	0.79	0.92	0.89	1.05	1.17	1.24	1.43	1.68	1.92	2.06	2.04	ns
HSUL_12	0.69	0.72	0.82	0.95	1.65	1.84	2.05	1.80	2.29	2.59	2.87	2.41	ns
DIFF_HSUL_12	0.69	0.72	0.82	0.92	1.65	1.84	2.05	1.47	2.29	2.59	2.87	2.08	ns
HSTL_I_S	0.68	0.72	0.82	0.84	1.15	1.28	1.38	1.46	1.79	2.03	2.20	2.07	ns
HSTL_II_S	0.68	0.72	0.82	0.84	1.05	1.17	1.26	1.44	1.69	1.93	2.08	2.05	ns
HSTL_I_18_S	0.70	0.72	0.82	0.86	1.12	1.24	1.34	1.41	1.75	2.00	2.16	2.02	ns
HSTL_II_18_S	0.70	0.72	0.82	0.86	1.06	1.18	1.26	1.44	1.70	1.94	2.08	2.05	ns
HSTL_I_12_S	0.68	0.72	0.82	0.94	1.14	1.27	1.37	1.43	1.78	2.02	2.20	2.04	ns
HSTL_I_DCI_S	0.68	0.72	0.82	0.78	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_S	0.68	0.72	0.82	0.78	1.05	1.17	1.26	1.33	1.69	1.93	2.08	1.94	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	0.76	1.15	1.28	1.38	1.40	1.78	2.03	2.20	2.01	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	0.76	1.05	1.16	1.24	1.32	1.69	1.92	2.06	1.93	ns
HSTL_II_T_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	0.89	1.15	1.28	1.38	1.47	1.79	2.03	2.20	2.08	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	0.89	1.05	1.17	1.26	1.47	1.69	1.93	2.08	2.08	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	0.76	1.15	1.28	1.38	1.47	1.78	2.03	2.20	2.08	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	0.76	1.05	1.17	1.26	1.40	1.69	1.93	2.08	2.01	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	0.89	1.12	1.24	1.34	1.46	1.75	2.00	2.16	2.07	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	0.89	1.06	1.18	1.26	1.47	1.70	1.94	2.08	2.08	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	0.75	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	0.75	1.05	1.16	1.24	1.41	1.69	1.92	2.06	2.02	ns
DIFF_HSTL_II_T_DCI_18_S	0.75	0.79	0.92	0.76	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
HSTL_I_F	0.68	0.72	0.82	0.84	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_II_F	0.68	0.72	0.82	0.84	0.97	1.08	1.15	1.29	1.61	1.84	1.97	1.90	ns
HSTL_I_18_F	0.70	0.72	0.82	0.86	1.04	1.16	1.24	1.32	1.68	1.91	2.06	1.93	ns
HSTL_II_18_F	0.70	0.72	0.82	0.86	0.98	1.09	1.16	1.35	1.62	1.85	1.98	1.96	ns
HSTL_I_12_F	0.68	0.72	0.82	0.94	1.02	1.13	1.21	1.26	1.65	1.88	2.03	1.87	ns
HSTL_I_DCI_F	0.68	0.72	0.82	0.78	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.78	0.97	1.08	1.15	1.22	1.61	1.84	1.97	1.83	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	0.76	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.76	0.98	1.09	1.16	1.27	1.61	1.85	1.98	1.88	ns
HSTL_II_T_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	0.89	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	0.89	0.97	1.08	1.15	1.35	1.61	1.84	1.97	1.96	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	0.76	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVC MOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVC MOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVC MOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVC MOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVC MOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVC MOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVC MOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVC MOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVC MOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVC MOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVC MOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVC MOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVC MOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVC MOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVC MOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVC MOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVC MOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVC MOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVC MOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVC MOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVC MOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVC MOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVC MOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVC MOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVC MOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVC MOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVC MOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVC MOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVC MOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVC MOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVC MOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS12_F8	0.64	0.67	0.78	0.95	1.27	1.42	1.55	1.41	1.91	2.18	2.37	2.02	ns
LVDCI_18	0.47	0.50	0.60	0.86	1.99	2.15	2.35	2.44	2.62	2.91	3.17	3.05	ns
LVDCI_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	2.40	2.62	2.99	3.40	3.01	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.87	1.99	2.15	2.34	1.86	2.62	2.90	3.17	2.48	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	1.83	2.62	2.99	3.40	2.44	ns
HSLVDCI_18	0.68	0.72	0.82	0.86	1.99	2.15	2.35	2.43	2.62	2.91	3.17	3.04	ns
HSLVDCI_15	0.68	0.72	0.82	0.84	1.98	2.23	2.58	2.27	2.62	2.99	3.40	2.88	ns
SSTL18_I_S	0.68	0.72	0.82	0.86	1.02	1.15	1.24	1.41	1.66	1.90	2.07	2.02	ns
SSTL18_II_S	0.68	0.72	0.82	0.87	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.76	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.78	0.88	0.98	1.08	1.26	1.51	1.74	1.90	1.87	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.78	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL15_S	0.68	0.72	0.82	0.81	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.78	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.80	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL135_S	0.69	0.72	0.82	0.89	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL12_S	0.69	0.72	0.82	0.95	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.89	1.02	1.15	1.24	1.43	1.66	1.90	2.07	2.04	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.89	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.75	0.88	0.98	1.08	1.33	1.51	1.74	1.90	1.94	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.89	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.75	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.76	0.94	1.06	1.15	1.38	1.57	1.82	1.97	1.99	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.91	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.43	1.60	1.85	2.01	2.04	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.91	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.78	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.80	1.03	1.17	1.27	1.41	1.66	1.92	2.09	2.02	ns

Input/Output Logic Switching Characteristics

Table 22: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ICE1CK} /T _{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	0.56/−0.16	ns
T _{ISRCK} /T _{ICKSR}	SR pin Setup/Hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	0.88/−0.30	ns
T _{IDOCKE2} /T _{IOCKDE2}	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
T _{IDOCKDE2} /T _{IOCKDDE2}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
T _{IDOCKE3} /T _{IOCKDE3}	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
T _{IDOCKDE3} /T _{IOCKDDE3}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
Combinatorial						
T _{IDIE2}	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.09	0.10	0.12	0.14	ns
T _{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.15	ns
T _{IDIE3}	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.09	0.10	0.12	0.14	ns
T _{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.15	ns
Sequential Delays						
T _{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.36	0.39	0.45	0.54	ns
T _{IDLODE2}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.55	ns
T _{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.36	0.39	0.45	0.54	ns
T _{IDLODE3}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.55	ns
T _{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	0.71	ns
T _{RQ_ILOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.32	ns
T _{GSRQ_ILOGICE2}	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
T _{RQ_ILOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.32	ns
T _{GSRQ_ILOGICE3}	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_ILOGICE2}	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.68	ns, Min
T _{RPW_ILOGICE3}	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.68	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
T _{ISCKK_BITSLIP} / T _{ISCKC_BITSLIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	0.02/0.21	ns
T _{ISCKK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	0.51/−0.22	ns
T _{ISCKK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	−0.17/0.40	ns
Setup/Hold for Data Lines						
T _{ISDCK_D} /T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.03/0.19	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	0.19/0.19	ns
Sequential Delays						
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	0.67	ns
Propagation Delays						
T _{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	0.14	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.44/−0.24	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	0.67/−0.25	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input Setup/Hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	0.46/−0.25	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/−0.15	ns
T _{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.70	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/−0.15	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{SHCKO}	Clock to A – B outputs	0.68	0.70	0.85	1.08	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	1.44	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	0.69/0.33	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	0.21/0.63	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	0.63/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	0.46/0.10	ns, Min
T _{CECK_LRAM} / T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	0.47/0.10	ns, Min
Clock CLK						
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	1.11	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	2.22	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	1.35	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	1.72	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	1.25	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	0.41/0.10	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	0.42/0.10	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	0.41/0.36	ns, Min
Clock CLK						
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.91	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.

Table 31: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCKK_RSTRAM}/T_{RCKC_RSTRAM}$	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	0.34/0.40	ns, Min
$T_{RCKK_WEA}/T_{RCKC_WEA}$	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	0.54/0.19	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	0.65/0.37	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	0.60/0.38	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers ⁽¹⁰⁾	0.76	0.83	0.93	1.06	ns, Max
$T_{RREC_RST}/T_{RREM_RST}$	FIFO reset recovery and removal timing ⁽¹¹⁾	1.59/–0.68	1.76/–0.68	2.01/–0.68	2.07/–0.60	ns, Max
Maximum Frequency						
$F_{MAX_BRAM_WF_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	372.44	MHz
$F_{MAX_BRAM_RF_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	372.44	MHz
$F_{MAX_BRAM_RF_DELAYED_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	317.36	MHz
$F_{MAX_CAS_WF_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	322.48	MHz
$F_{MAX_CAS_RF_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	322.48	MHz
$F_{MAX_CAS_RF_DELAYED_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.27	427.35	350.88	267.38	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	372.44	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	254.13	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO} .
- T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with $DO_REG = 0$.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
- $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- These parameters include both A and B inputs as well as the parity inputs of A and B.
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
- RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Clock Buffers and Networks

Table 33: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK_CE}/T_{BCKKC_CE}^{(1)}$	CE pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
$T_{BCCCK_S}/T_{BCKKC_S}^{(1)}$	S pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
$T_{BCKKO_O}^{(2)}$	BUFGCTRL delay from I0/I1 to O	0.08	0.10	0.12	0.10	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	560.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCKKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKKO_O} values.

Table 34: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	1.48	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	710.00	MHz

Table 35: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	1.06	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	0.57	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	0.93	ns
Maximum Frequency						
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	600.00	540.00	450.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 36: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.12	ns
T_{BHCK_CE}/T_{BHCKC_CE}	CE pin Setup and Hold	0.20/0.16	0.23/0.20	0.38/0.21	0.28/0.09	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	560.00	MHz

Table 37: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC7K70T	0.29	0.40	0.40	0.47	ns
		XC7K160T	0.42	0.53	0.57	0.59	ns
		XC7K325T	0.59	0.74	0.79	0.91	ns
		XC7K355T	0.45	0.57	0.59	0.69	ns
		XC7K410T	0.60	0.74	0.79	0.91	ns
		XC7K420T	0.60	0.74	0.79	0.91	ns
		XC7K480T	0.60	0.74	0.79	0.91	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	0.12	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

Table 39: PLL Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550.00	500.00	450.00	450.00	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300.00	300.00	300.00	300.00	MHz
PLL_F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLCKC_DADDR} / T _{PLLCKC_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKC_DI} / T _{PLLCKC_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKC_DEN} / T _{PLLCKC_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLCKC_DWE} / T _{PLLCKC_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7K70T	4.98	5.49	6.17	7.04	ns
		XC7K160T	5.23	5.77	6.48	7.38	ns
		XC7K325T	5.72	6.31	7.09	8.07	ns
		XC7K355T	5.34	5.87	6.57	7.51	ns
		XC7K410T	5.84	6.44	7.22	8.21	ns
		XC7K420T	5.50	6.04	6.77	7.73	ns
		XC7K480T	5.50	6.04	6.77	7.73	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7K70T	5.29	5.83	6.55	7.47	ns
		XC7K160T	5.84	6.45	7.24	8.24	ns
		XC7K325T	6.33	6.99	7.84	8.92	ns
		XC7K355T	5.95	6.55	7.32	8.36	ns
		XC7K410T	6.45	7.12	7.97	9.07	ns
		XC7K420T	6.41	7.06	7.90	9.01	ns
		XC7K480T	6.41	7.06	7.90	9.01	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 53: GTX Transceiver Performance (Cont'd)

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1 ⁽¹⁾		-2L ⁽²⁾		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F _{GQPLL} RANGE2	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	125.00	MHz

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

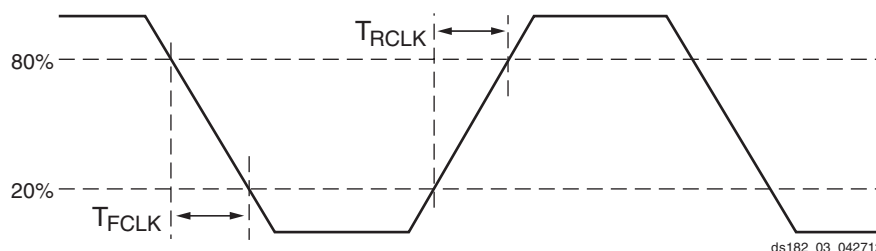


Figure 3: Reference Clock Timing Parameters

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: PCI Express Protocol Characteristics⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 68: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Master/Slave Serial Mode Programming Switching						
T _{DCC} /T _{CCKD}	DIN Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCC} /T _{SMCCKD}	D[31:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T _{SMWCC} /T _{SMCCKW}	RDWR_B Setup/Hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T _{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F _{RBCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI Setup/Hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F _{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] Setup/Hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T _{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
T _{SPICCF}	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

- To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 69 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 69: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	—	—	115	mA
t_j	Temperature range	15	—	125	°C

Notes:

- The FPGA must not be configured during eFUSE programming.

Date	Version	Description
07/25/12	1.6	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 9. Updated parameters in Table 3. Added Table 4 and Table 5. Changed the typical values for many of the devices in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated speed specification to v1.06 (-3, -2, -2L(1.0V), -1) and v1.05 (-2L(0.9V)) with appropriate changes to Table 14 and Table 15 including production release of the XC7K325T and the XC7K410T in the -2, -2L(1.0V), and -1 speed designations. Added notes and specifications to Table 17 and Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 51 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 67 updated Note 1 and added Note 4. In Table 68, updated T_{POR} and F_{EMCCK}.
09/04/12	1.7	Updated Table 14 and Table 15 for production release of the XC7K160T in the -2, -2L(1.0V), and -1 speed designations.
09/26/12	1.8	In Table 2 , revised V_{CCINT} and V_{CCBRAM} and added Note 2 . Updated Table 14 and Table 15 for production release of the XC7K480T in the -2, -2L(1.0V), and -1 speed designations and the XC7K325T and XC7K410T in the -3 speed designation.
10/10/12	1.9	Updated the $I_{CCINTMIN}$ value for the XC7K355T in Table 7 . Updated Table 14 and Table 15 for production release of the XC7K420T in the -2, -2L(1.0V), and -1 speed designations.
10/25/12	2.0	Updated the AC Switching Characteristics based upon ISE 14.3 v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and ISE 14.3 v1.06 for the -2L (0.9V) speed specifications throughout the document. Updated Table 14 and Table 15 for production release of the XC7K355T in the -2, -2L(1.0V), and -1 speed designations. Also updated Table 14 and Table 15 for production release of the XC7K325T and XC7K410T in the -2L (0.9V). Added values for Table 16 -2L (0.9V). Added package skew values to Table 50. In Table 53, increased -1 speed grade (FF package) F_{GTMAX} value from 6.6 Gb/s to 8.0 Gb/s.
10/31/12	2.1	Updated Table 14 and Table 15 for production release of the XC7K70T in the -2, -2L(1.0V), and -1 speed designations.
11/26/12	2.2	Updated Table 14 and Table 15 for production release of -3 speed designation for XC7K70T, XC7K160T, XC7K355T, XC7K420T, and XC7K480T. Removed Note 4 from Table 67 .
12/05/12	2.3	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K160T, XC7K420T, and XC7K480T. Updated Note 1 in Table 50 .
12/12/12	2.4	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K70T and XC7K355T. Added Internal Configuration Access Port section to Table 68 .